STUDIES ON Ⅲ-Ⅴ COMPOUND SEMICONDUCTORS ON Si SUBSTRATES GROWN BY MOCVD

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STUDIES ON III-V COMPOUND SEMICONDUCTORS ON Si SUBSTRATES GROWN BY MOCVD

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CONTENTS

Chapter 1. Introduction

1.1 Heteroepitaxy of III-V compound semiconductors on Si

Semiconductor materials are roughly classified into two types; one is an elemental semiconductor (Si, Ge) and the other is a compound semiconductor (GaAs, InP, InAs •••).

The Si technology has been developed aiming at the electronic devices with the large integration. But the Si material has some essential limitations, i.e., light emitting devices cannot be fabricated and the signal processing speed is not high.

On the other hand, the epitaxial growth technique of III-V compound semiconductors has been developed recently and high-performance devices such as optical devices, high speed devices and microwave devices have been fabricated by LPE (liquid phase epitaxy), MOCVD (metalorganic chemical vapor deposition), MBE (molecular beam epitaxy), etc. Comparing with the elemental semiconductors, III-V compound semiconductors are promising materials because they have a direct band gap, a high mobility and a high drift velocity. Moreover, alloy semiconductors can be obtained by mixing some compound semiconductors, varying the lattice constant and the band gap energy gradually, and they can easily fabricate heterojunctions. Taking these advantages, various devices such as double heterostructure lasers, high efficiency solar cells, wide gap emitter transistors and HEMT's (high

electron mobility transistors) can be fabricated.

But, until now, these devices have been almost fabricated on the lattice matched substrates, such as AlGaAs/GaAs, InGaAsP/InP and InGaAlP/GaAs.

If III-V compound semiconductors can be grown on Si substrates, new devices would be realized. Especially, GaAs on a Si substrate enables us to combine GaAs and Si devices[1-3].

The advantages of growing GaAs on Si substrates are as follows.

(1) The GaAs band structure is direct and a laser diode can be easily obtained by fabricating the double heterostructure.

(2) The GaAs drift velocity is high, and high speed devices and microwave devices can be obtained. The electron drift velocity of GaAs is about 5 times larger than that of Si.

(3) Si substrates are mechanically strong, light and cheap.

(4) The heat conductivity of Si is about 3 times larger than that of GaAs and the Si substrate itself can take the place of a heat sink of a power device such as a laser and a power FET (field effect transistor).

(5) Si substrates are larger than GaAs substrates. High quality Si wafers with the diameter of 6-8 inch can be available, while the maximum diameter of a GaAs wafer is about 3 inch. The control of dislocation, impurity and stoichiometry of the large GaAs wafer is difficult now.

The comparison between Si and GaAs is summarized in Table 1.1[2].

The examples of the device application of this technology

Table 1.1 Comparison between GaAs and Si[2)]

	Si	GaAs
mobility ($cm^2/V \cdot s$)	1500	8600
electron arrival velocity (cm/s)	1×10^7	3×10^7
band gap energy (eV)	1.11	1.42
thermal conductivity (W/K•cm)	1.45	0.46
thermal expansion coefficient ($^oC^{-1}$)	2.6×10^{-6}	5.9×10^{-6}
specific gravity (g/cc)	2.33	5.32
lattice constant (nm)	0.5431	0.5653
band structure	indirect	direct
crystal structure	diamond	zincblend
mechanical strength	strong	fragile
heterojunction	difficult	easy (AlGaAs)
wafer size (inch)	6-8	2-3
price	cheap	expensive

are as follows.

(1) Monolithic optoelectronic IC's that contain GaAs optical and Si electronic devices, e.g. OEIC's (opto electronic integrated circuits)

(2) High efficiency tandem structure solar cells on cheap and light weight substrates

(3) High speed GaAs IC's on large area Si substrates

(4) GaAs/Si hybrid IC's

However, there are three large problems to grow high quality GaAs on Si substrates, i.e.,

(1) The lattice mismatch between Si and GaAs is about 4.1% and a lot of misfit dislocations generate.

(2) The thermal expansion coefficient of GaAs is about 2.5 times larger than that of Si and the large tensile stress would be applied to the GaAs layer when the grown wafer is cooled down from the growth temperature to the room temperature. Moreover, there appear cracks on the epilayer when the epilayer thickness increases.

(3) When a polar semiconductor is grown on a nonpolar semiconductor, the formation of an antiphase domain structure take place[4] where the grown layer is separated by the antiphase boundaries, in which the two regions are crystallographically reversed as the Ga atoms and As atoms reverse positions.

As mentioned above, although the heteroepitaxy of III-V compounds on Si substrates is a promising technology, there exist problems. To overcome these difficulties, an intermediate layer

between III-V compound semiconductors and Si must be grown. Until recently, some attempts have been made and some compound semiconductors were grown on Si substrates. In the next section, successfully grown compound semiconductors and fabricated devices on Si substrates and the intermediate layer structures are reviewed.

1.2 Growth of compound semiconductors on Si substrates

1.2.1 GaAs on Si substrates

GaAs was first grown on Si substrate using Ge as the intermediate layer[5]. Figure 1.1 shows the lattice constant and the thermal expansion coefficients of semiconductors. Since the lattice constant and the thermal expansion coefficient of Ge is almost the same as those of GaAs, GaAs can be relatively easily grown on Ge substrates[6-10]. After Ge was formed on a Si substrate by a vacuum evaporation or an ion cluster beam (ICB)[11-13], GaAs is grown on it[14]. But this method will meet difficulty that GaAs is contaminated by Ge because of its high vapor pressure and the Ge diffusion into the epi-layer. Moreover, the GaAs crystallinity is greatly affected by the Ge condition and a new growth technique to form Ge on Si is indispensable. Although solar cells[15-17], FET's[18,19], LED's[20,21] and lasers[22,23] have been fabricated using Ge as the intermediate layer, these chracteristics are not satisfactory. This method will not be the

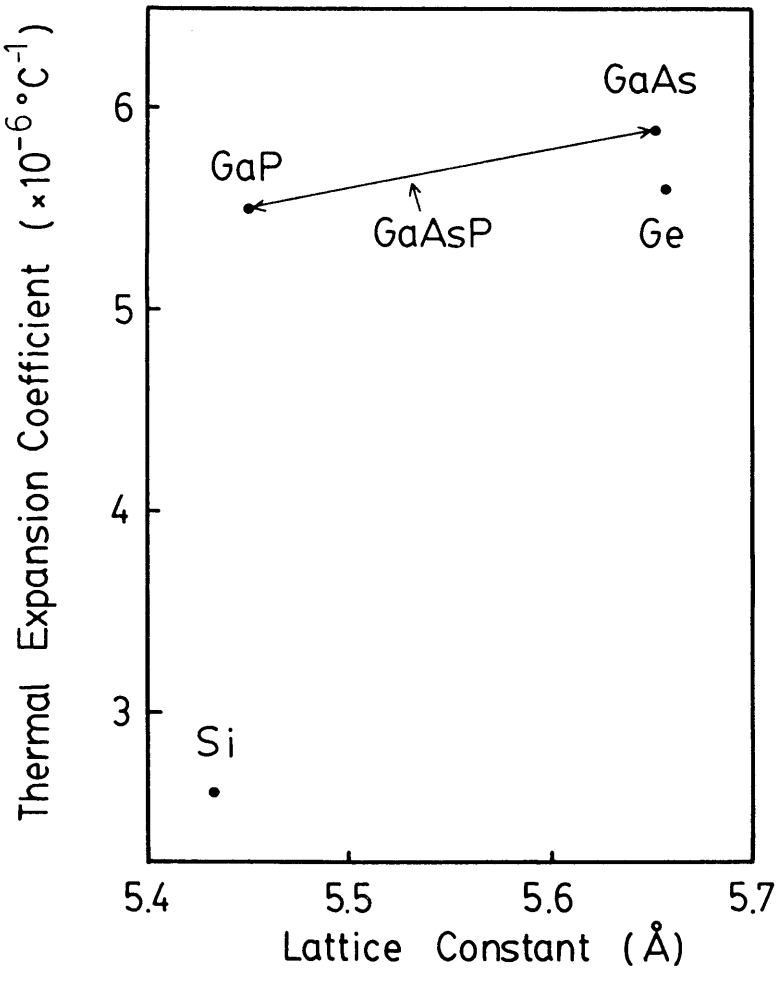

Fig.1.1 Lattice constants and thermal expansion coefficients of semiconductors.

hopeful method.

The most popular technique to grow GaAs on Si substrate recently is so-called two-step growth method[24-26]. In this method, first thin GaAs amorphous film (aboot 20nm) is deposited on a high-temperature annealed Si at the relatively low temperature (450-500^{o}C), next heat it up to crystallize, and continue to grow GaAs at the normal temperature (650-700^{o}C). The grown layer on Si using this method is high quality, i.e., the high electron mobility of 5200cm^{2}/V•s and the low etch pit density less than 3000cm^{-2}. MESFET's[27] and LED's[28] were fabricated by using this method. However, still there remain problems, that the cracks appear on more than 3μm-thick GaAs layer on Si[24], and that it is still in question whether this method can be applicable to the growth of all the compound semiconductors on Si.

Attempts to grow GaAs on Si directly[29-31] or using the intermediate layers of Ge/W/SiO_2[32], CaF_2[33] or AlGaAs/GaAs superlattice[34] have also been made. Although LED's[32], solar cells[35], lasers[36,37], FET's[38,39], bipolar transistors[40] and HEMT's[34] have been fabricated, still the most suitable technique has not ever been found.

1.2.2 Other semiconductors on Si substrates

(A) GaP

The lattice constant of GaP is almost the same as Si and attempts to grow GaP on Si have been made for a long time[41,42].

Single crystalline GaP has been obtained on a Si substrate by VPE (vapor phase epitaxy)[43-45], MBE[46,47] and MOCVD[48-50]. The characteristic of p-n junction, photoluminescence and deep levels have been obtained. The relationship between growth conditions and the primitive properties of the epitaxial layer is also presented.

(B) GaSb

GaSb was first grown on Si by MBE[51]. Optically pumped lasers emitting at 1.7μm[52] and photoconductive detectors[53] were fabricated although the lattice mismatch is about 12%. But properties of the grown layer have not been obtained.

(C) InP

InP was grown on Si by MOCVD[54]. The single domain crystal is obtained although the lattice mismatch is about 8%. The etch pit density and the X-ray diffraction of InP/Si were obtained. InP/Si is expected to be a promising material for the future optoelectronic devices.

(D) AlP

AlP is almost lattice matched to Si and was grown on it by a transport reaction, utilizing the disproportionation of AlCl[55]. The primitive optical properties were obtained. But the crystal quality is poor because the compound including Al is sensitive to the residual O_2 and H_2O in the growth system.

(E) AlGaN

AlGaN has been usually grown on Al_2O_3. But it was successfully grown on Si by MOCVD[56]. The crystal growth is not easy because the crystal structure is different and it is difficult to form a uniform nucleus at the hetero-interface. The detailed properties of the grown layers have not been clarified.

(F) II-VI compound semiconductors

ZnS[57], ZnSe[58] and CdTe[59] have been grown on Si recently. The conditions to grow single crystals on Si have been obtained. But the optimization of the conditions at the initial stage of the growth is the problem at present.

1.3 Purpose and scope of this dissertation

The studies on the growth of GaAs on Si were started for establishing the growth technique, for characterizing the GaAs layers grown on Si and for fabricating the AlGaAs/GaAs lasers on Si. Although GaAs/Si is a promising material, there still remain many problems to grow GaAs on Si substrates as described in this chapter. To overcome these difficulties, a new method for growing GaAs on Si is proposed in this study.

In this thesis, GaAs is grown on Si substrates with the intermediate layer of strained layer superlattices (SLS's)[60-62], which will hopefully eliminate the threading dislocations[63,64] and relax the mismatch between GaAs and Si. A strained layer

superlattice is an alternating multilayer structure of thin layers whose lattice constants are different. GaAs grown using SLS's is characterized by some measurements because the properties of the grown layer have not been clarified yet.

The MOCVD growth technique is used for the epitaxial growth. For growing GaAs on Si, this technique has advantages compared with other growth techniques, i.e.,

(1) The thin multi films such as superlattices can be easily grown by alternating the gas flow.

(2) The growth is performed under the thermal nonequilibrium condition compared with LPE, enabling the heteroepitaxy.

(3) Very thin layers are obtained over a large area.

GaAs is grown on Si by changing the intermediate layer structure and the growth conditions because the epitaxial layer is greatly affected by these parameters. Next, grown layers are characterized by some measurements, comparing with the GaAs layer grown on GaAs substrate, and lasers are fabricated. Finally, GaAsP is grown on Si and $GaAs_{0.6}P_{0.4}$ LED is fabricated.

This dissertation is composed of six chapters. The summary is as follows.

Chapter 1 is the introduction of this dissertation and describes the development of III-V compound semiconductors on Si.

In chapter 2, GaAs is grown on Si with the intermediate layers of AlP, AlGaP, GaAs/GaAsP SLS and GaAsP/GaAs SLS by MOCVD and crystallinity and electrical properties are given. The optimization of the structure and the growth condition is

performed.

In chapter 3, the effect of the substrate orientation on the crystallographic properties and the conditions to obtain a single domain structure are given. The GaAs layer grown on Si is characterized by photoluminescence, electroreflectance, deep level transient spectroscopy etc.

In chapter 4, AlGaAs/GaAs double heterostructure lasers are fabricated on Si. The fabrication process and lasing characteristics are given.

In chapter 5, $GaAs_{1-x}P_x$ (x=0-1) is grown on Si with the intermediate layers of GaP and SLS's. $GaAs_{0.6}P_{0.4}$ LED's emitting at 655nm are fabricated on Si.

Chapter 6 is the summary of this dissertation. The scope for the future work is also given.

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Chapter 2. MOCVD growth of GaAs on Si substrate with strained layer superlattices

2.1 Introduction

The heteroepitaxial growth of GaAs on Si has been attracting much attention because this technique enables us to realize new devices as described in chapter 1. However, the technique to grow GaAs on Si has not so much been established and the device performance is typically inferior to that grown homoepitaxially on the GaAs substrate since the crystal quality of GaAs on Si is still poor at present. This would be due to the difference in the lattice constant on the one hand and the difference in the thermal expansion coefficient on the other hand, and thus more directly, due to the improper choice of the intermediate layer.

To overcome these difficulties, new complex structures of III-V compounds are proposed as an intermediate layer to give a high quality GaAs surface layer[1-4] on Si.

Among many III-V compound semiconductors, GaP and AlP have nearly the same lattice constant as Si. In view of an inference that the interface between Si and the bottom III-V compound semiconductor should most effectively affect the crystallinity of the surface GaAs layer, GaP or AlP is first grown on Si. But there exists the large lattice mismatch between GaAs and GaP or AlP. There are two methods to relax the lattice mismatch. One is to use the compositional graded layer[5], i.e. the content of P

in GaAsP is varied gradually from 1 to 0 to reach GaAs. But the thickness of the graded layer must be very thick to obtain a high quality GaAs free of dislocation[6]. The other method which is used in this study is the use of a strained layer superlattice[7-9]. A strained layer superlattice is a multilayer structure of thin films whose lattice constants are different. When the thickness is thinner than the critical thickness, the misfit dislocation does not generate, distorting the lattice[10]. Practically, dislocation-reduced GaAsP has been grown on the lattice mismatched GaAs substrate with a SLS buffer layer[10] and the reduction of the dislocation by the use of SLS has been confirmed by TEM (transmission electron microscope)[11].

After all, GaAs is grown on Si substrates using the following two intermediate structures, and the optimization of the structure and the growth condition is performed.

(A) GaAs/SLS/AlP/Si

(B) GaAs/SLS/GaP/Si

The crystal is grown by the MOCVD technique. This technique is suitable for growing superlattices easily and suitable for the heteroepitaxy because the crystal is grown under thermal nonequillibrium.

In this chapter, at first, the MOCVD growth apparatus used in this study is described. GaAs is grown on Si using the two kinds of intermediate layer ((A) and (B)) having the strained layer superlattices structure. There involved are a lot of growth parameters for obtaining a high quality epitaxial GaAs

layer such as the superlattice thickness, the layer number and the growth temperature of the respective layer. The effect of growth parameters on the optical, electrical and crystallographical properties is described. The optimized structure and growth conditions are given.

2.2 MOCVD growth apparatus and crystal growth

Figure 2.1 shows the schematic illustration of the detailed gas lines used in this study. The MOCVD growth apparatus is composed of three parts, i.e., source materials and the transport gas whose gas flow is controlled by mass flow controllers, the reactor and the exhaust of gases. The reacting part consists of a horizontal square (4.5 x 5.5 cm) reactor and an inductively heated graphite susceptor at atmospheric pressure. To increase the flow speed and to smooth the gas flow, a block of SiO_2 is inserted into the reactor as shown in Fig. 2.2.

H_2 is a high purity Pd-diffused gas. TMG (trimethylgallium), TMA (trimethylalluminum), AsH_3 (10% in H_2) and PH_3 (10% in H_2) are used as the source materials. DEZ (diethylzinc) and H_2Se (100ppm in H_2) are used for p or n type dopant, respectrively. No precracking of PH_3 or AsH_3 is performed. The flow rates of hydride materials are precisely controlled by the mass flow controllers and those of metal organic compounds are controlled by the H_2 flow rate bubbled into the materials. These gases are all poisonous and they must be treated carefully. The burned-off

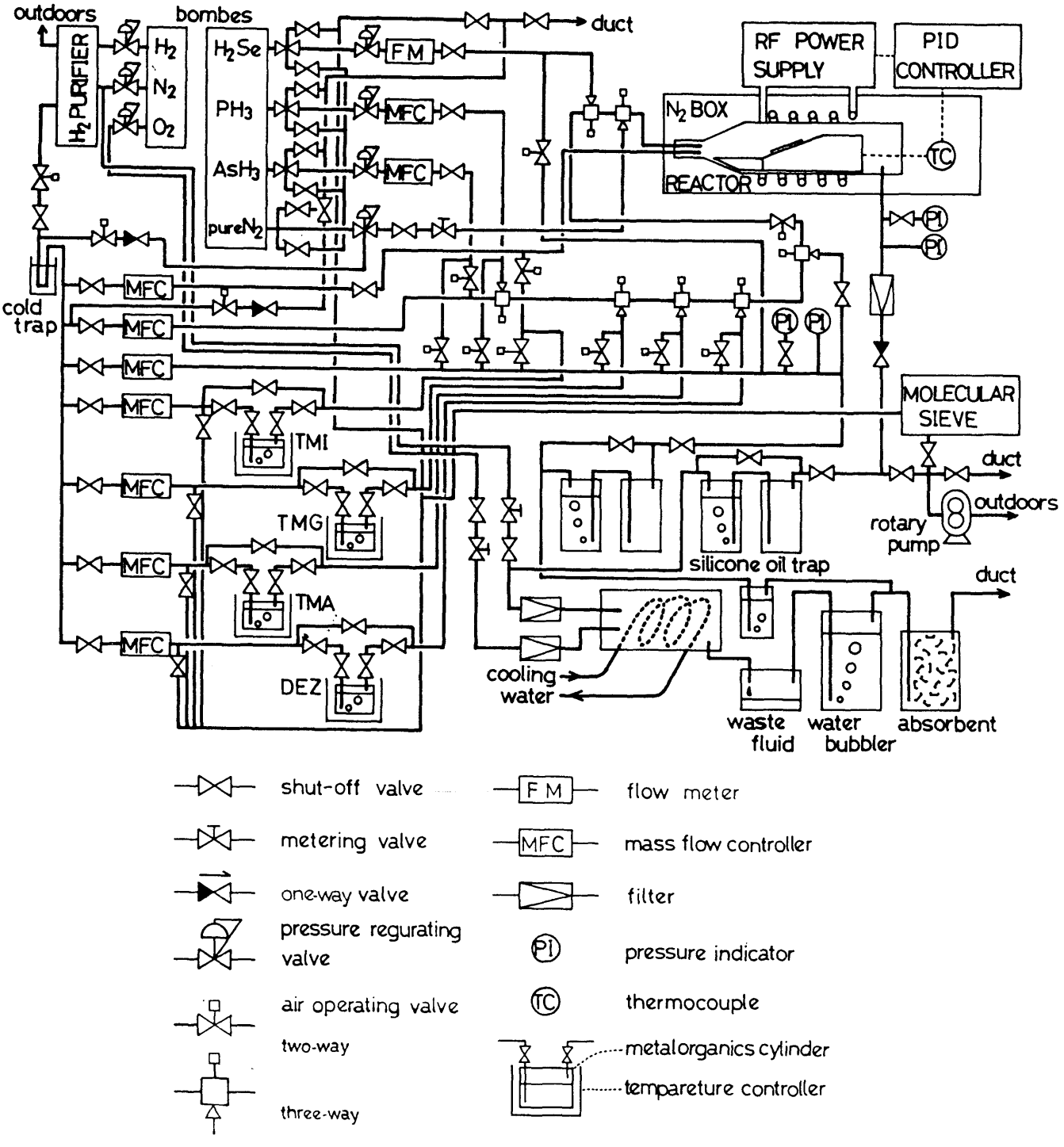

Fig. 2.1 Gas lines of the MOCVD growth apparatus.

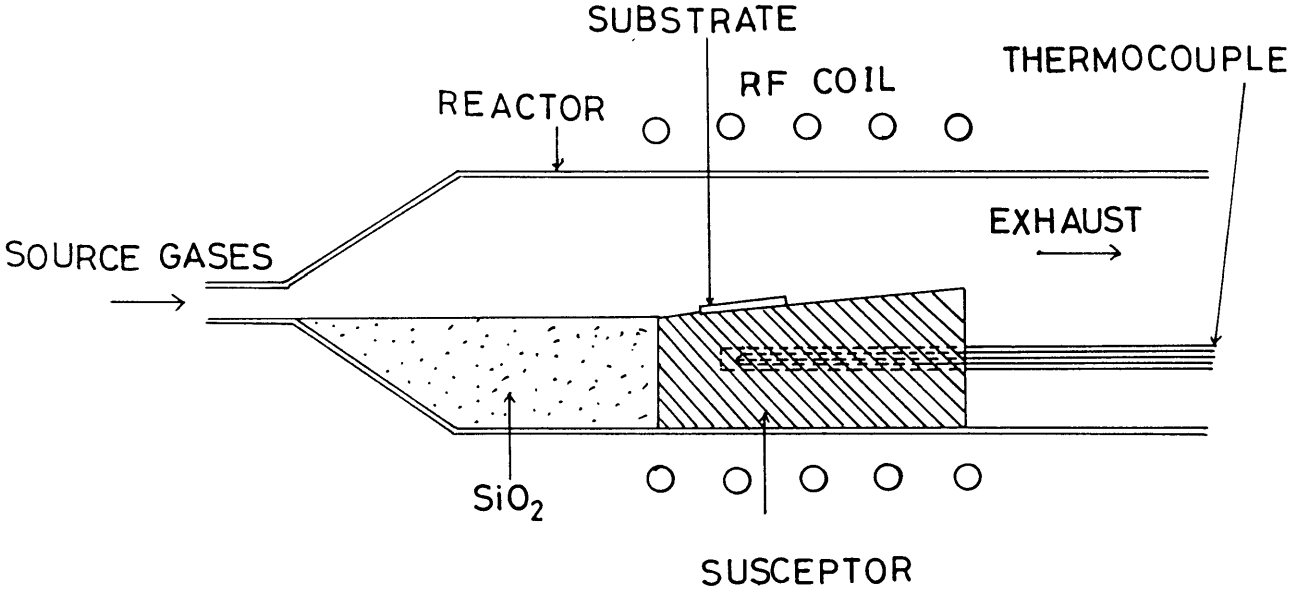

Fig. 2.2 Schematic view of the MOCVD reactor.

exhausted gases pass through the absorbent and the toxicities are perfectly removed.

The Si substrate are 320μm-thick polished wafer cut from n- or p-type Czochralski-grown single crystal. The tested orientations are (100)just, (100)2° off, (110) and (111).

Before carrying out the growth, substrates are carefully cleaned and etched. Substrates are cleaned by the ultrasonic cleaner in methylalcohol, trichloroethane and methylalcohol for 5, 10 and 5 minutes, respectively. In the early stage of this study, $HF:HNO_3:H_2O$ = 1:2:4 solution at room temperature is used as the etchant. But since the surface sometimes becomes rough after etching, the etchant is changed to $HF:H_2O$ = 1:1 solution. Substrates are etched for 2 minutes at room temperature, followed by the rinse by the deionized water. Next, they are blown by N_2 in N_2 box just prior to loading into the reactor. After loading, the reactor tube is evacuated and flashed with a purified hydrogen gas for 20 minutes before growth.

2.3 Growth of GaAs on Si substrate with AlP and strained layer superlattices[1-3)]

GaAs is grown on Si substrates with III-V compound intermediate layers by MOCVD. Among III-V compound semiconductors, fortunately GaP and AlP have nearly the same lattice constant as Si. The growth of high quality GaP on Si is very difficult, on the other hand, AlP is easily grown on Si uniformly because of

the strong bond between Al and Si atoms. GaP can be successfully grown on an AlP layer using an intermediate layer of $Al_{0.5}Ga_{0.5}P$. The lattice mismatch of GaP and GaAs can be relaxed by the strained layer superlattice. However, the lattice mismatch is too large to be relaxed only by one kind of superlattice layer, and thus, two stages of superlattice layers of $GaP/GaAs_{0.5}P_{0.5}$ and $GaAs_{0.5}P_{0.5}$ /GaAs are used. The proposed structure is schematically shown in Fig. 2.3.

The possible alternative structure such as GaAs/(AlGaAsP/GaAs SLS)/(AlP/AlGaAsP SLS)/AlP/Si etc. may be considered, but these structures are expected to be inferior to the present structure because these structures contain many Al content layers in the intermediate layers. AlP and compounds including high Al content are not stable in an atmosphere, and the crystal quality of these materials becomes very sensitive to the residual water/oxgen vapor in the growth system.

In this structure, there are many growth parameters to be optimized for obtaining a high quality epitaxial GaAs layer on Si. In this section, the effects of the SLS's, AlP+AlGaP layers and the thickness of GaAs layer on the crystallinity, the PL (photoluminescence) intensity and the carrier concentration are described. Next, these results are compared with GaAs grown on GaAs and Ge-coated Si substrate prepared by ICB.

The growth condition is briefly mentioned below. The mole fractions of TMG and TMA to hydrogen in growing the intermediate layers are kept constant at 3.6×10^{-5} and 3.1×10^{-5},

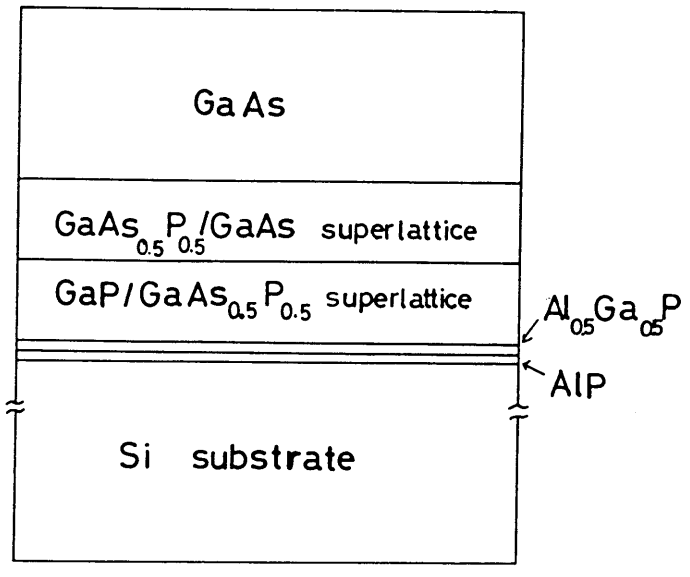

Fig. 2.3 Structure to grow GaAs on Si substrate

respectively and the V/III ratio (the ratio of group V atoms to group III atoms introduced into the reactor) is 84. The growth temperature is 950°C for AlP and AlGaP and 830°C for the superlattice layers. The total hydrogen flow rate is 3.8 l/min. The growth rate is 20 nm/min for the superlattice growth. The growth conditions of the surface undoped GaAs layer are the following; the growth temperature is 730°C, the V/III ratio is 40, the total hydrogen flow rate is 3.8 l/min, the mole fraction of TMG to hydrogen is 1.2×10^{-4} and the growth rate is about 75 nm/min. The etched Si substrates are annealed at 1000°C in hydrogen atmosphere for 10 minutes to remove the oxidized layer at the surface[12] and to reconstract the surface[13] and growth starts.

2.3.1 Crystallinity

The effects of the intermediate layer structure on the crystallinity and the surface morphology are investigated for various structures. Figure 2.4 shows the X-ray diffraction curves from the (400) Bragg lines of GaAs for the following three samples; (A) GaAs(2μm)/SLS's(350nm)/Si, (B) GaAs(2μm)/GaP (100nm)/AlGaP(13nm)/AlP(7nm)/Si, (C) GaAs(2μm)/SLS's(350nm)/AlGaP (13nm)/AlP(7nm)/Si, where there are 10 layers in one superlattice and the respective layer thickness is 17.5nm. The intermediate layers of AlP+AlGaP+GaP bring about the narrow peak in the X-ray diffraction curve (sample (B)) compared to the sample with only

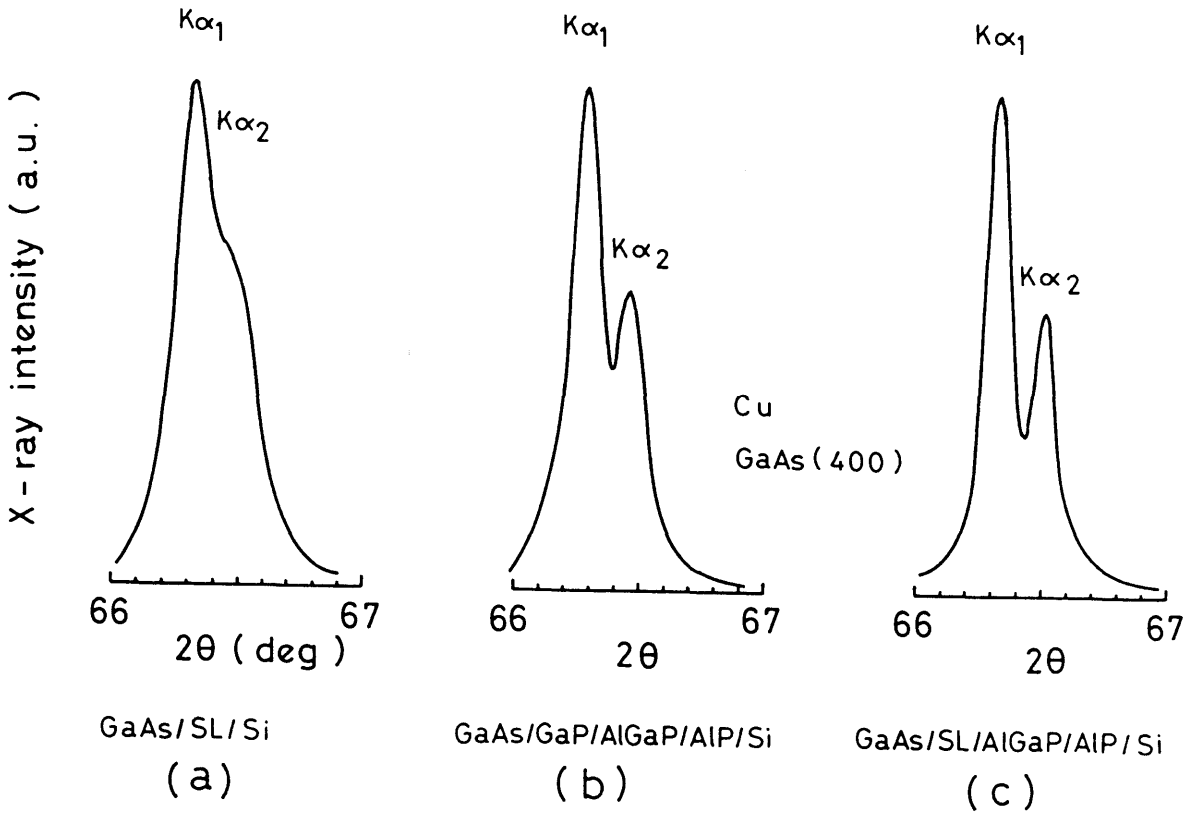

Fig. 2.4 X-ray diffraction patterns for various structures.

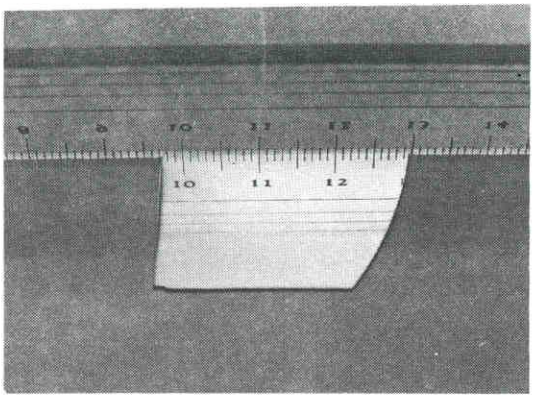

Fig. 2.5 Photograph of GaAs surface on Si.

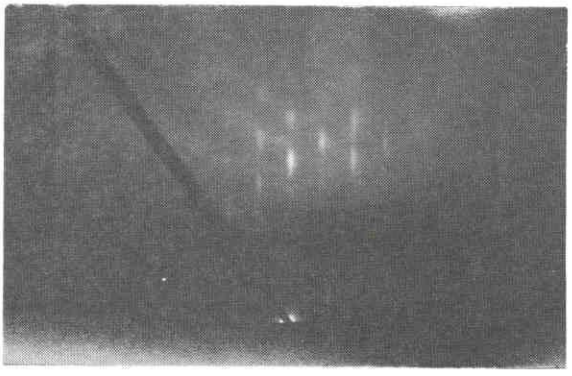

Fig. 2.6 RHEED pattern of GaAs on Si.

superlattice (sample (A)). Moreover, the insertion of superlattice between GaAs and GaP together with AlP and AlGaP brings about the narrower peak of the rocking curve. Figure 2.5 shows the photograph of the surface for sample (C), presenting a mirror-like surface. This means that the large lattice mismatch between GaAs and Si can be relaxed by two stages of strained layer superlattices. An example of the reflection electron diffraction pattern for sample (C) is shown in Fig. 2.6, indicating the spot pattern with Kikuchi lines. This photograph shows that the good crystalline single crystal of GaAs could be obtained with AlP, AlGaP and the strained layer superlattices.

2.3.2 Optical and electrical properties

To investigate the effects of the intermediate layers on the PL intensity and the carrier concentration of the surface GaAs, the thickness of AlP+AlGaP, the layer number in SLS layer, the thickness in SLS and the GaAs layer thickness are changed while keeping the growth conditions same. All the grown layer are n-type and the thickness is 2μm unless otherwise mentioned.

Figure 2.7 shows the carrier concentration n determined by C-V method and normalized PL intensity by the carrier concentration PL/n as a function of the total layer thickness of AlP+AlGaP. The photoluminescence is measured at room temperature using 514.5nm line of an argon ion laser with an excitation intensity of 2.4W/cm^2. Both the carrier concentration and the

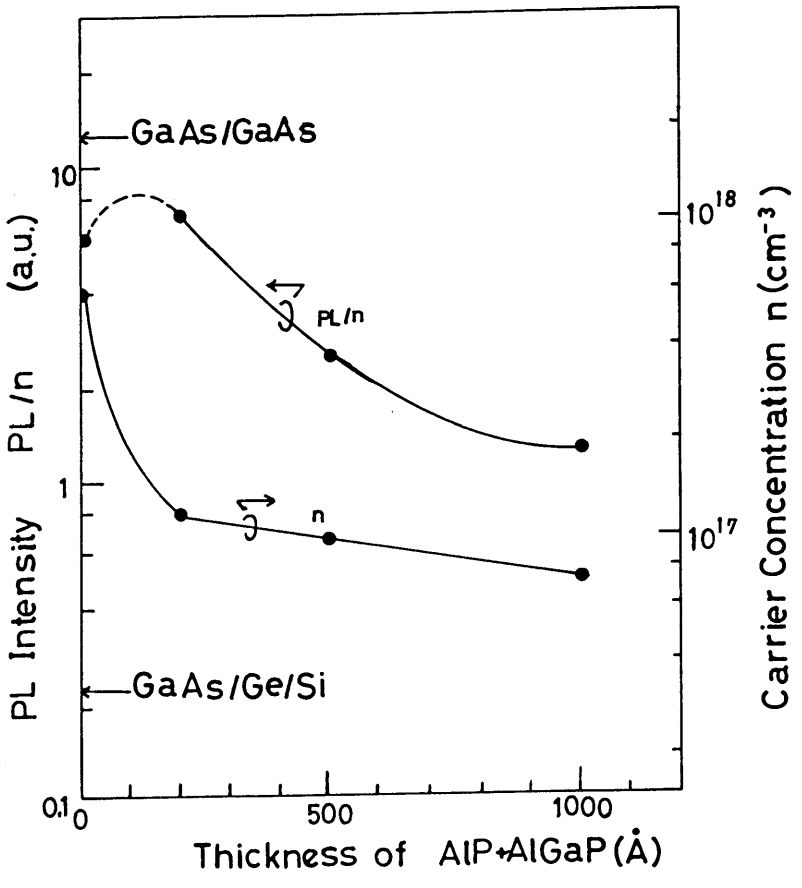

Fig. 2.7 PL intensity and carrier concentration vs. the thickness of AlP + AlGaP.

normalized PL intensity decrease with increasing the thickness of AlP and AlGaP. But when there is no AlP and AlGaP layers, PL/n decreases and carrier concentration increases rapidly, and the surface becomes rough. Thus there must be a maximum of PL/n at small thickness of AlP and AlGaP layers. The PL intensity is about one order of magnitude higher than that grown on a Ge-coated Si substrate.

Figure 2.8 shows the PL intensity normalized by carrier concentration determined by van der Pauw method and PL/n as a function of layers in one superlattice when the thickness of AlP+ AlGaP is 20nm. The numbers of layers in two superlattice layers are same. When there is no superlattice, PL/n is about one order of magnitude smaller than that with superlattice layers. PL/n has a small maximum at about ten layers. On the other hand, the carrier concentration slightly increases with increasing the layer number. The total intermediate layer thickness is less than 0.7μm. Figure 2.9 shows PL/n and the carrier concentration vs. each layer thickness in the superlattice. The layer number in one superlattice is 10. PL/n has a maximum at about 20 nm for each layer thickness while the carrier concentration is un-changed.

Figure 2.10 shows PL/n and the carrier concentration as a function of the surface GaAs layer thickness. The PL/n increases with increasing the thickness of GaAs and saturates over 3μm. The increase in PL intensity with increasing the layer thickness is not caused by the increased absorption of the exciting light

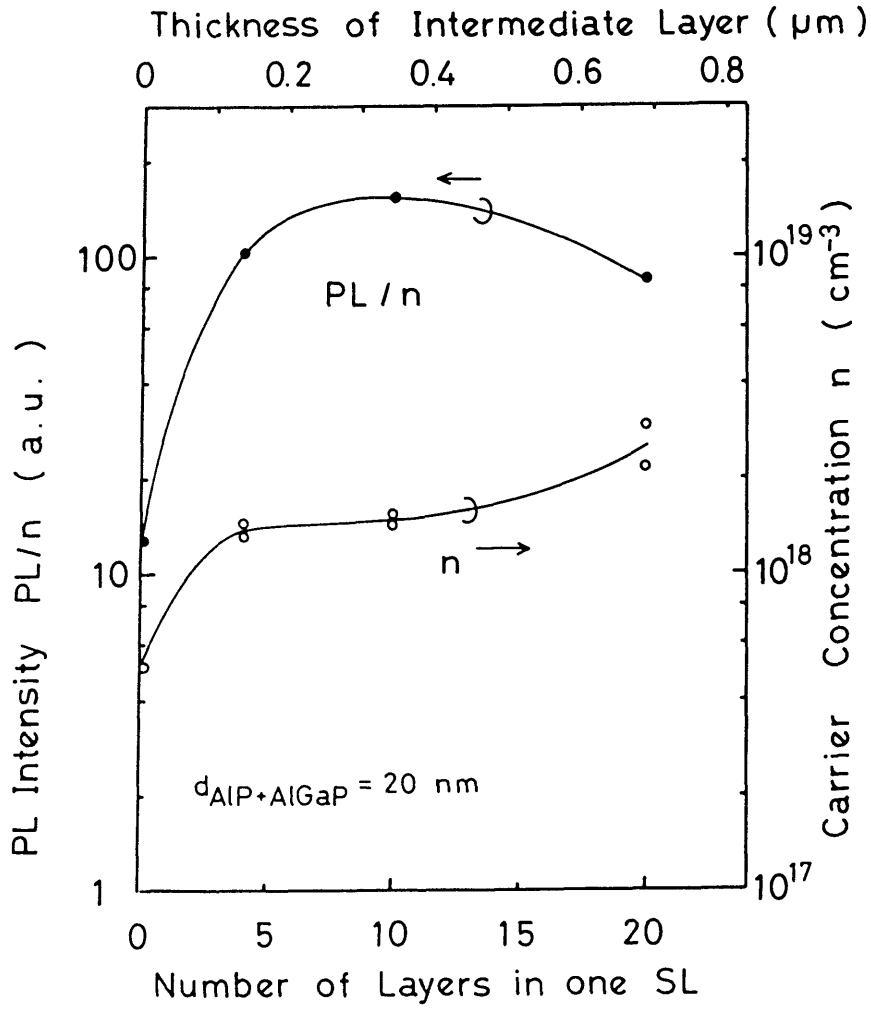

Fig. 2.8 PL intensity and carrier concentration vs. layer number in one superlattice.

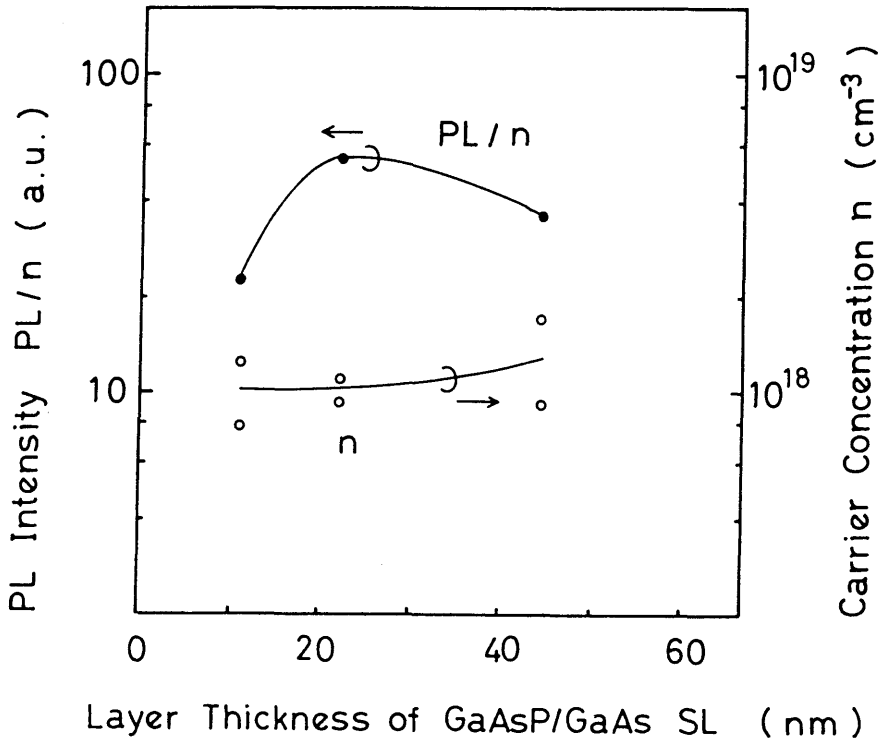

Fig. 2.9 PL intensity and carrier concentration vs. layer thickness in the superlattice.

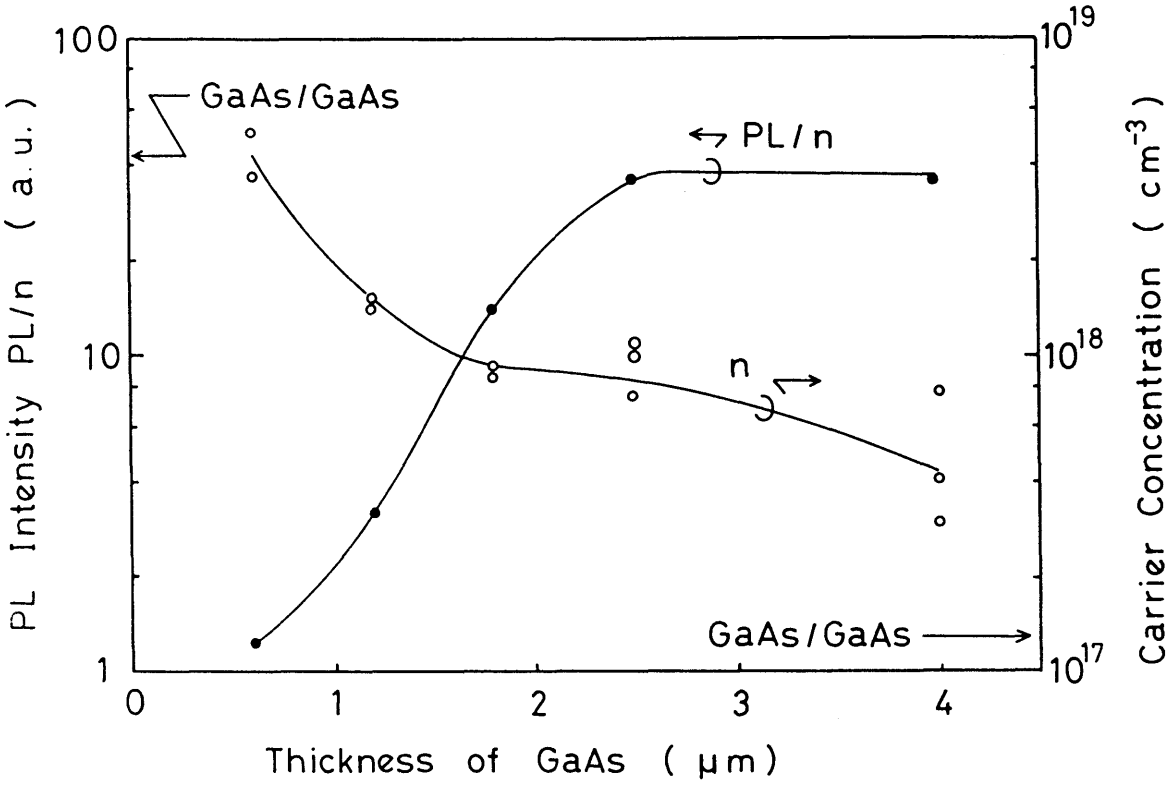

Fig. 2.10 PL intensity and carrier concentration vs. surface GaAs thickness. PL/n and n values for GaAs/GaAs epitaxial growth sample are shown by arrows.

because the minimum GaAs layer thickness (0.6μm) is much larger than the absorption length of the exciting light (about 0.1μm). The saturated value of PL intensity is about 80% of that of GaAs grown on GaAs substrate. Figure 2.11 shows the in-depth profile of the carrier concentration measured by the C-V method using the electrochemical cell. The carrier concentration increases drastically with approaching toward the intermediate layer, and n^+-Si layer is formed by the diffusion of P or As into Si substrate. The slightly larger carrier concentration near the top surface compared to that on GaAs substrate seems to be caused by the auto doping of Si during the growth and will be improved by the SiO_2 coating to the back side of the Si substrate. These results indicate that GaAs grown thicker than 3μm on Si substrate is hardly affected by the Si substrate and the intermediate layers, and the optical and electrical properties are comparable to that grown on GaAs substrate.

Table 2.1 shows the PL half width at 150K for various structure. Adding the AlP and AlGaP layers, the half width becomes 11meV narrower than that without these layers but still 8meV broader than that grown on GaAs substrate. The peak energy for GaAs grown on Si shifts 16meV toward lower energy side compared to GaAs/GaAs by the effect of lattice strain.

2.4 Optimization to grow GaAs on Si

In the previous section, GaAs was grown on Si with AlP,

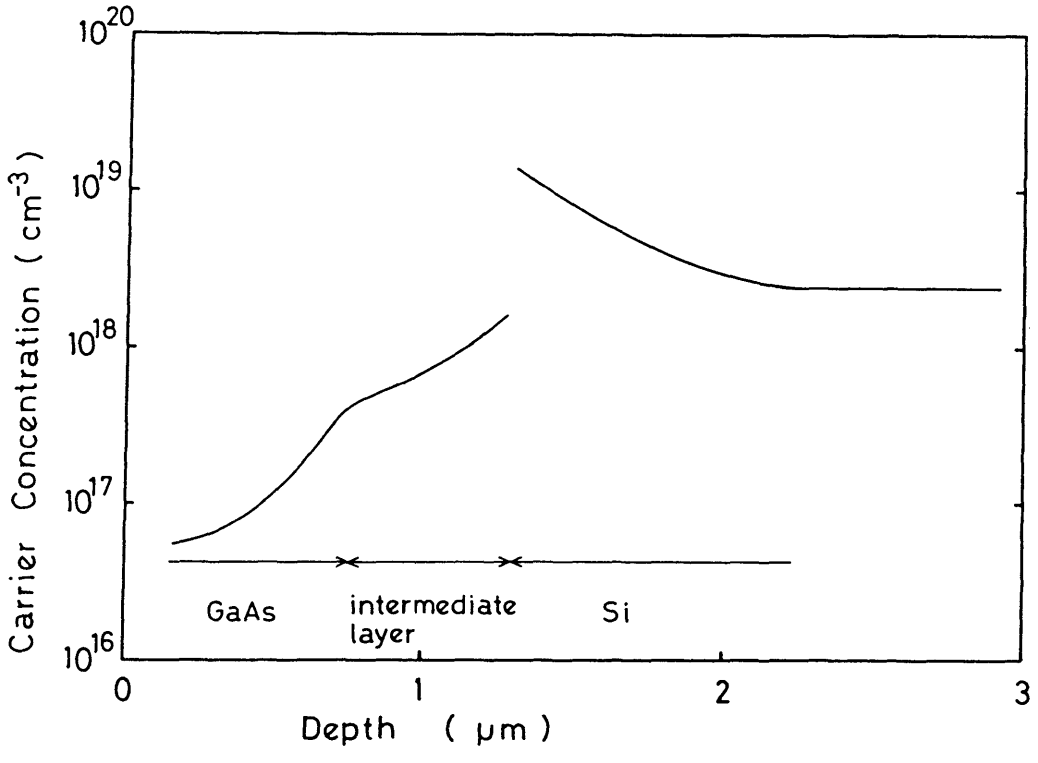

Fig. 2.11 In-depth carrier profile of GaAs on Si.

Table 2.1 PL half width at 150K for various structures.

Sample	Half width (meV)
GaAs/SLS's/AlGaP/ AlP/Si	41
GaAs/SLS's/Si	52
GaAs/Ge/Si	62
GaAs/GaAs	33

AlGaP and SLS's. But this structure is not the most suitable structure because the crystallinity of the intermediate layer including high Al content is poor, producing the barrier between GaAs snd Si.

The growth of GaAs on Si without using AlP and AlGaP is performed to obtain a high quality GaAs by changing the growth sequence and the growth conditions.

The growth procedure is as follows[14]. Figure 2.12 shows the temperature program to grow GaAs on Si. Before inserting the substrate into the reactor, the substrate susceptor is annealed in H_2 ambient at 950°C to bake out As or P deposited to the susceptor during the previous growth run as it possibly contaminates the Si substrate[15].

The etched substrate is then loaded and annealed at 950°C for 10 minutes in H_2+PH_3 atmosphere to remove the oxidized layer, to reconstract the surface and to coat it with very thin P[16]. These heat treatments are followed by the sequential growth of GaP (50nm), GaP/$GaAs_{0.5}P_{0.5}$ SLS ((20nm+20nm) x 5), $GaAs_{0.5}P_{0.5}$/GaAs SLS ((20nm+20nm) x 5) and GaAs (2μm). The growth temperatures of GaP, SLS's and GaAs are changed in the range T_{GaP}=850-950°C, T_{SLS} =680-900°C and T_{GaAs}=620-780°C, respectively. The total gas flow rate is 3.8 l/min. The mole fraction of TMG to hydrogen in growing the intermediate layer is kept constant at 3.6×10^{-5} and that for the surface GaAs layer is 1.2×10^{-4}. Under these conditions, the growth rates for the superlattice and the surface GaAs layer are 20 and 75 nm/min,

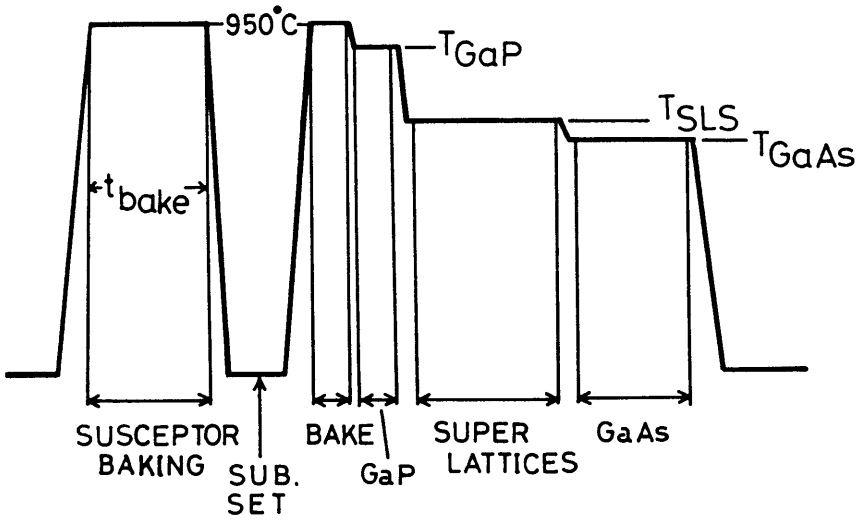

Fig. 2.12 Temperature program to grow GaAs on Si.

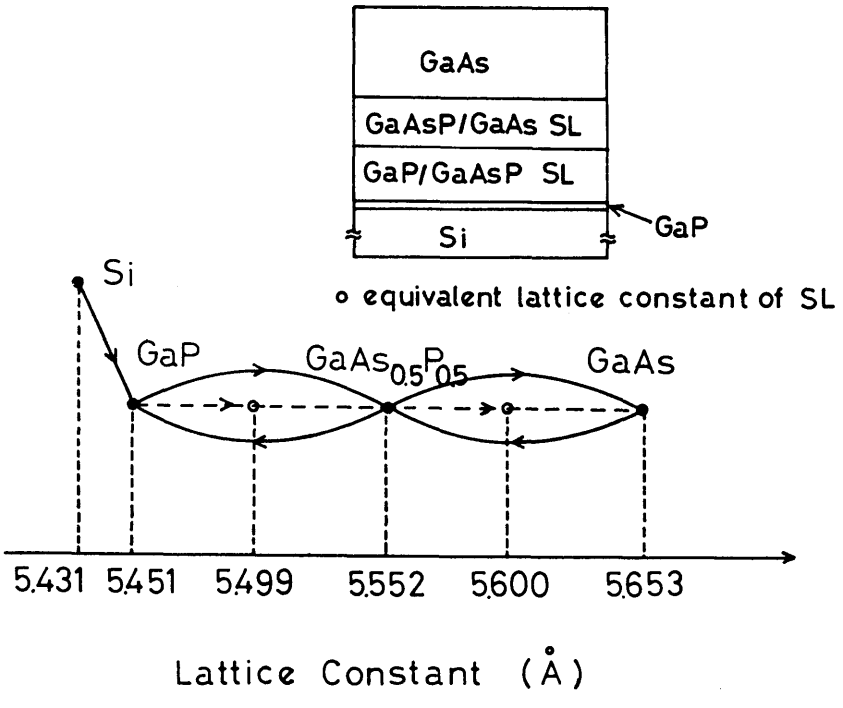

Fig. 2.13 Optimized structure to grow GaAs on Si and lattice constant of semiconductors used in this structure.

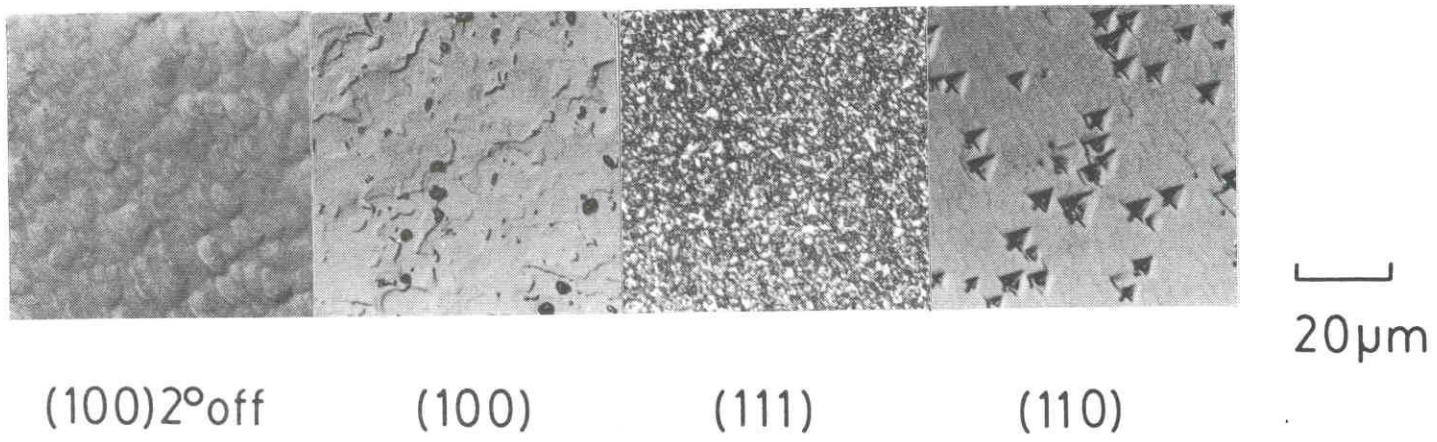

Fig. 2.14 Surface Nomarski micro photographs of GaAs grown at various Si substrate orientations.

respectively.

The structure to grow GaAs on Si and the lattice constants of the materials used in this structure are shown in Fig.2.13. The equivalent lattice constants of two SLS's are calculated using the formula in ref.17.

Figure 2.14 represents the Nomarski surface microphotographs of GaAs layers grown on various Si substrate orientations of (100)2^{o} off toward [011]+15^{o}, (100)just, (111) and (110). T_{GaP}, T_{SLS} and T_{GaAs} are 900, 680 and 650^{o}C, respectively. The surface morphology is the best on (100)2^{o} off orientation and has a single domain structure, while that grown on (100) has an anti-phase domain structure[18]. The surfaces grown on (111) and (110)Si are rough. So the following results are concentrated only on the growth on (100)2^{o} off substrate.

The room temperature PL half width of the GaAs layer grown on Si is shown in Figure 2.15 as a function of the susceptor annealing time, t_{bake}. The PL half width decreases with increasing the annealing time and saturates over 10 hours. This may be due to the perfect vaporization of attached As and P. Unless the two step annealings before the growth are performed, the surface becomes clouded. When the annealing temperature of the substrate is lower than 950^{o}C, the surface becomes clouded, demonstrating that the cleaning temperature more than 950^{o}C is necessary to reconstruct the surface and to vaporize the oxidized layer.

Figure 2.16 shows the PL spectra at 4.2K and the room

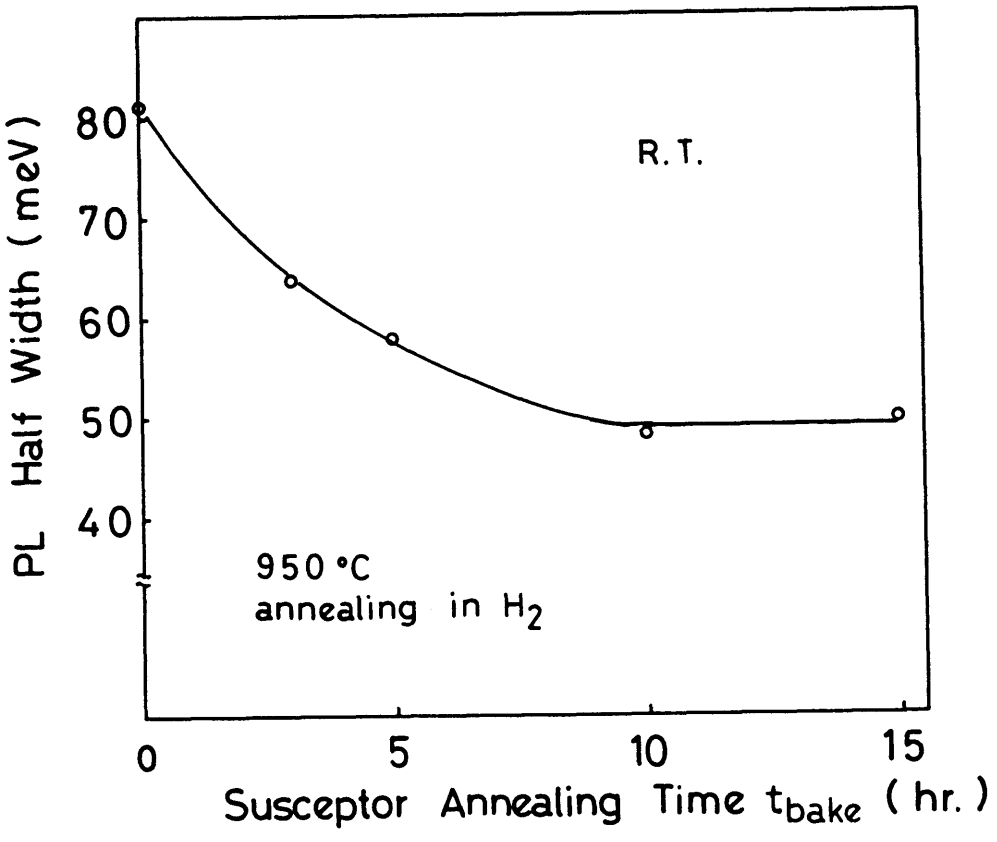

Fig. 2.15 Room temperature PL half width vs. annealing time of the susceptor.

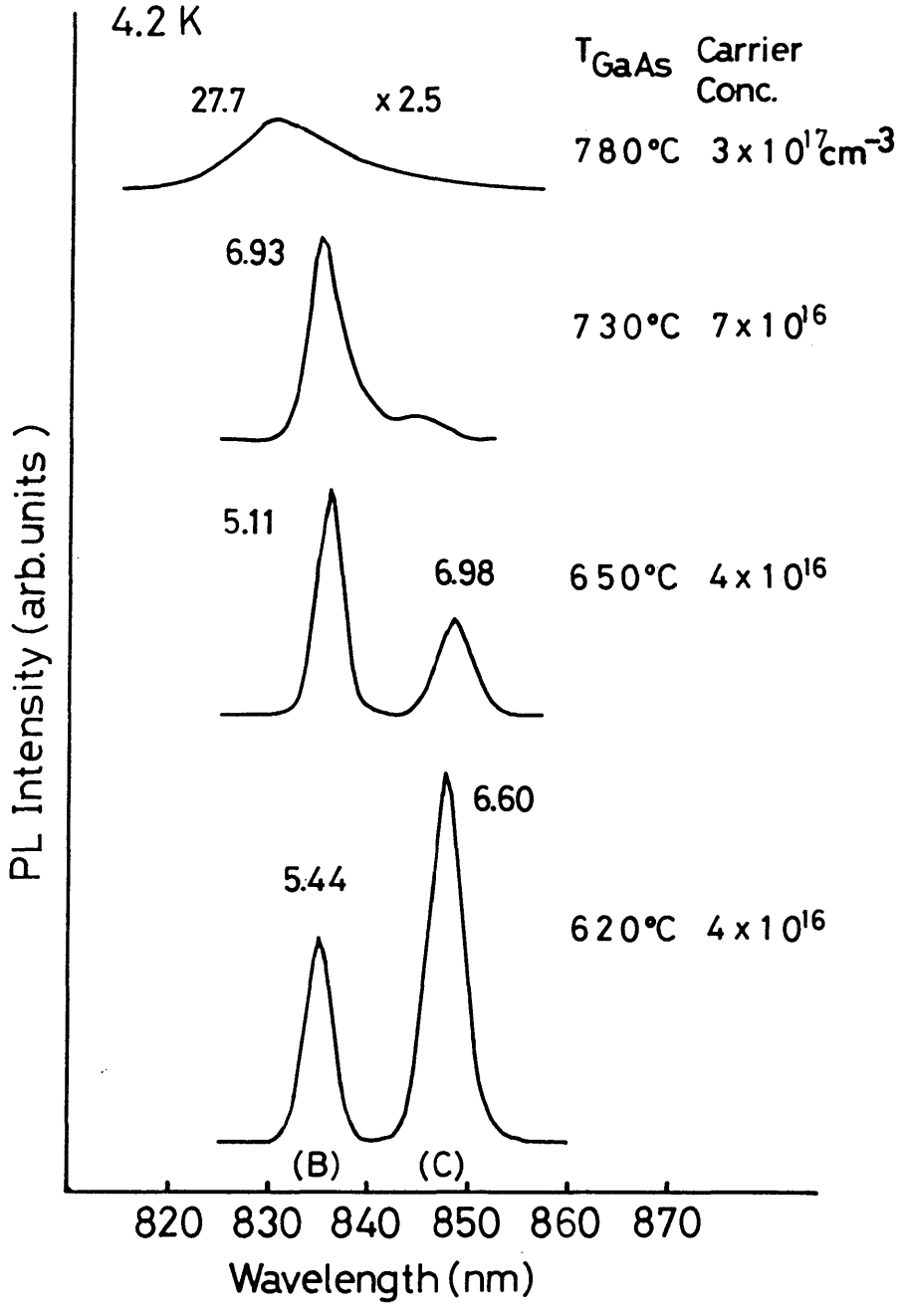

Fig. 2.16 4.2K PL spectra and room temperature carrier concentration at various growth temperature of GaAs. PL half width is indicated at the top of the peaks.

temperature carrier concentration at various growth temperature of GaAs, T_{GaAs}. The carrier concentration is measured by the C-V method. The PL half width of the respective peak is indicated in this figure. T_{GaP} and T_{SLS} are kept constant at 950 and 680°C, respectively. The PL intensity of the peak (B) at 1.4838eV is unchanged but that of the peak(C) at 1.4611eV decreases with increasing the growth temperature. The PL intensity is small at 780°C. The PL half width of the peak(B) has the minimum at 650°C. The carrier concentration decreases with decreasing the growth temperature and is about 4×10^{16} cm^{-3} at 650°C. The good surface is obtained in the temperature range of 650-730°C.

Figure 2.17 shows the PL spectra at 4.2K and the room temperature carrier concentration with changing the growth temperature of GaP, T_{GaP}. T_{GaAs} and T_{SLS} are 650 and 680°C, respectively. The sample becomes rough when the growth temperature is lower than 850°C and higher than 950°C. The half width has a minimum and the surface is the best at 900°C. The half width of the peak(B) is about 3.9 meV and that of peak(C) is 5.7 meV. The carrier concentration is not affected by the growth temperature of GaP and about $4 \times 10^{16} cm^{-3}$.

Figure 2.18 shows the PL half width at room temperature as a function of the growth temperature of the strained layer superlattice, T_{SLS}. The half width decreases with decreasing the growth temperature and is about 46meV at 680°C. The surface becomes rough when the growth temperature is lower than 680°C. When the strained layer superlattices are not grown between GaP

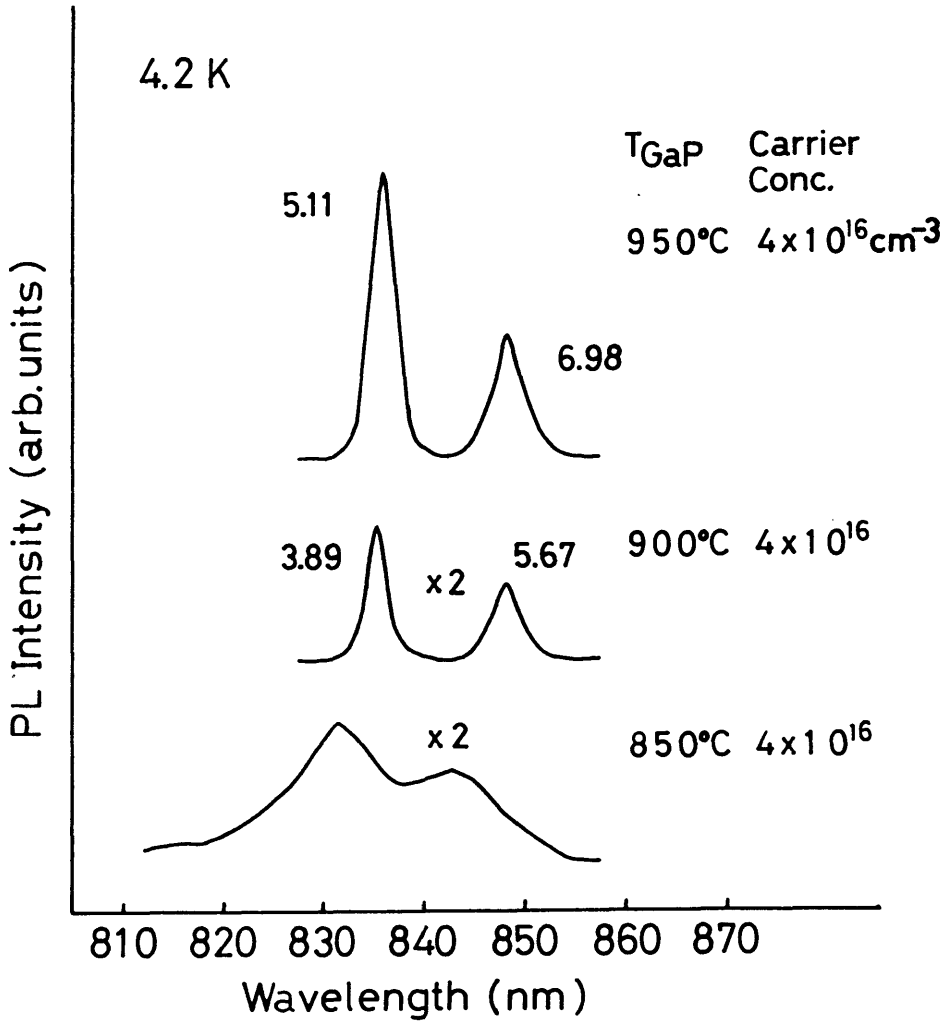

Fig. 2.17 4.2K PL spectra and room temperature carrier concentration at various growth temperature of GaP. PL half width is indicated at the top of the peaks.

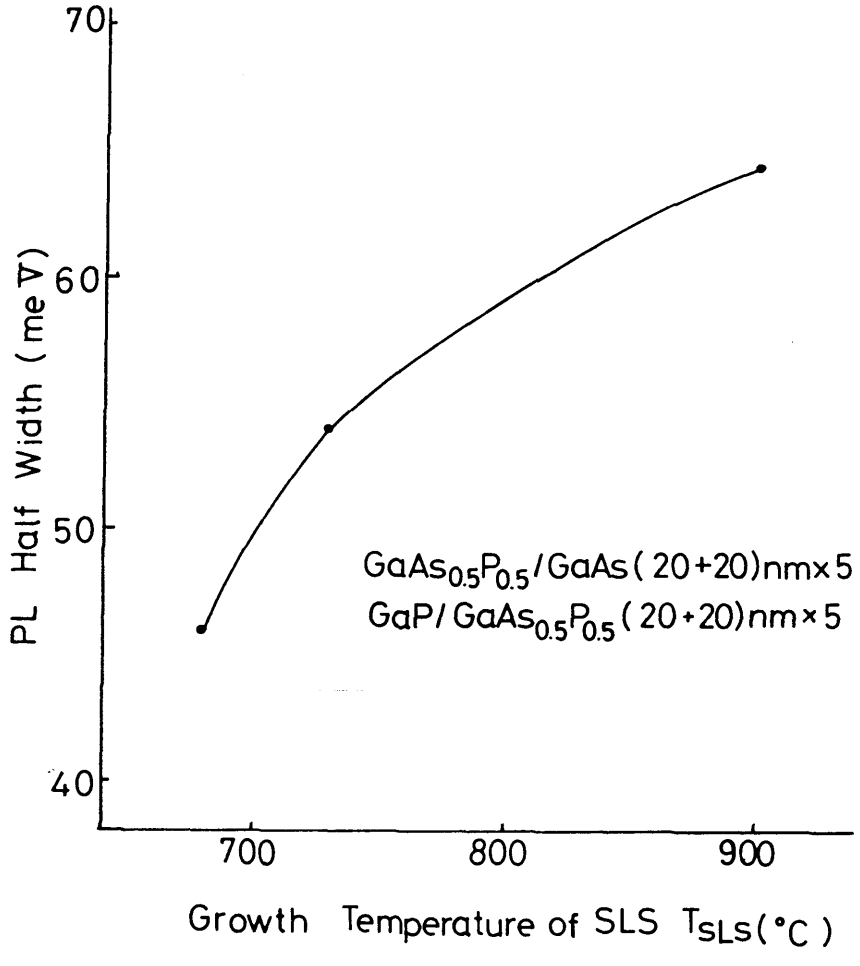

Fig. 2.18 Room temperature PL half width vs. growth temperature of SLS.

Table 2.2 Optimum growth conditions to grow GaAs on Si.

		($\times 10^{-5}$)	($\times 10^{-4}$)	($\times 10^{-3}$)		(nm/min)
	T_g(^{o}C)	TMG	AsH_3	PH_3	V/III	GROWTH RATE
SUSCEPTOR	950	-	-	-	-	-
SUBSTRATE	950	-	-	2.6	-	-
GaP	900	3.6	-	2.6	72	5
SLS's	680	3.6	8.4	2.6	94,72	20
GaAs	650	12	53	-	44	75

and GaAs, the PL intensity is about one order of magnitude smaller and the PL half width becomes broader to 88meV. The room temperature PL intensity from the best wafer is comparable to that grown on GaAs, but that at 4.2K is about one order of magnitude smaller than that grown homoepitaxially.

The optimum growth conditions, the growth temperature, the mole ratio of source gases to hydrogen, the mole ratio of group V to group III and the growth rate are summarized in Table 2.2.

2.5 Conclusion

A new intermediate layer structure to grow GaAs on Si substrates is proposed and demonstrated. The relationship between the intermediate layer structure and the electrical, optical and crystallographical properties of GaAs on Si is investigated. The optimum intermediate layers are composed of GaP, GaP/GaAsP SLS and GaAsP/GaAs SLS and the optimum growth conditions of the each layers are made clear. A single domain GaAs with a superior morphology is obtained on (100)2^{o} off Si substrates with the annealing of the susceptor in hydrogen and the annealing of the substrate in H_2 +PH_3 before the growth demonstrating the importance of the Si-compound semiconductor interface conditions. The optimization of the intermediate layer with AlP and AlGaP was performed in detail in this study. A more detailed optimization of the intermediate layer with GaP is the future work.

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Chapter 3. Characterization of GaAs on Si substrates

3.1 Introduction

Some AlGaAs/GaAs devices have been fabricated on Si substrates until now[1]. These device performances are still far inferior to those on GaAs substrates probably due to the difference in the lattice constant and/or the thermal expansion coefficient between Si and GaAs. But the properties of defects, dislocations, deep levels and the stress of GaAs on Si caused by these mismatches have not almost been investigated yet although these properties greatly affect the device performances.

In this chapter, GaAs grown on Si with the intermediate layers of GaP, GaP/GaAsP SLS and GaAsP/GaAs SLS optimized in chapter 2 is characterized by photoluminescence, electroreflectance, deep level transient spectroscopy, electron beem induced current etc. to evaluate the stress, deep levels and the characteristics of p-n junction. The conditions to obtain a single domain structure is also made clear.

3.2 Substrate orientation and crystal orientation

The crystal orientation of the Si substrate is a very important factor to obtain a single domain GaAs on Si. Some authors proposed the preference of (110) or (211) planes for polar on non-polar epitaxy[2-4]. However, the most important plane for

device application is (100). It has already been described in chapter 2 that the single domain GaAs can be grown on (100)2° off substrate. More important point is found to be the direction of off angle as described below[5].

Figure 3.1 shows the orientation of the GaAs grown on (100) 2° off toward [011]Si determined by etching the GaAs in $C_3H_4(OH)(COOH)_3 \cdot H_2O$-$H_2O_2$-$H_2O$ solution[6] and observing the cross section. The GaAs orientation is influenced by the direction of off angle and the GaAs [0$\bar{1}$1] direction coincides with the direction of off angle. Figure 3.2 shows the angle between the Si[011] and GaAs[0$\bar{1}$1] directions as a function of the direction of off angle θ shown in the inset. The Si[011] direction is always the GaAs[0$\bar{1}$1] direction except at θ = 45° where the surface becomes very bad and the GaAs has an antiphase domain (APD) structure[7]. As the [011] and [0$\bar{1}$1] directions of Si are equivalent, Fig.3.2 shows all the direction of the off angle. The result indicates that the atomic step along Si[011] plays an essential roles in growing single domain GaAs on Si. This behavior is explained as follows.

The schematic illustration of (100) plane having off angle toward [011]+θ is shown in Fig.3.3. There are atomic steps going two directions. It should be noted that these atomic steps are equivalent as Si in non-polar. At very early stage of the growth, the two kind of nuclears different in phase compete with each other. But, since the lengths of the terraces along two directions are different, one phase continues more earlier than

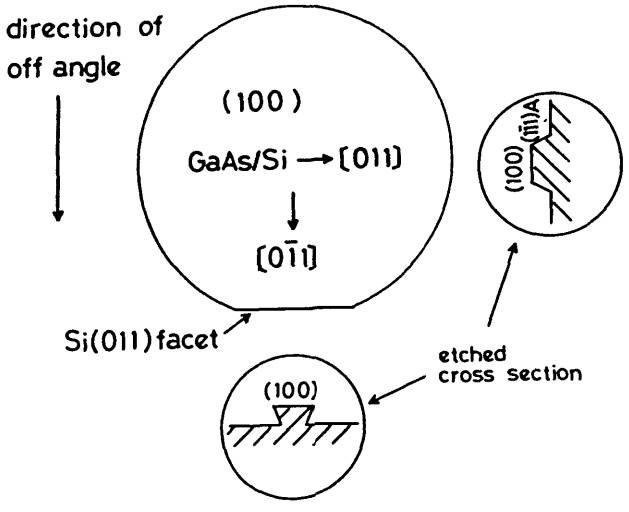

Fig. 3.1 Crystal orientation of GaAs on Si.

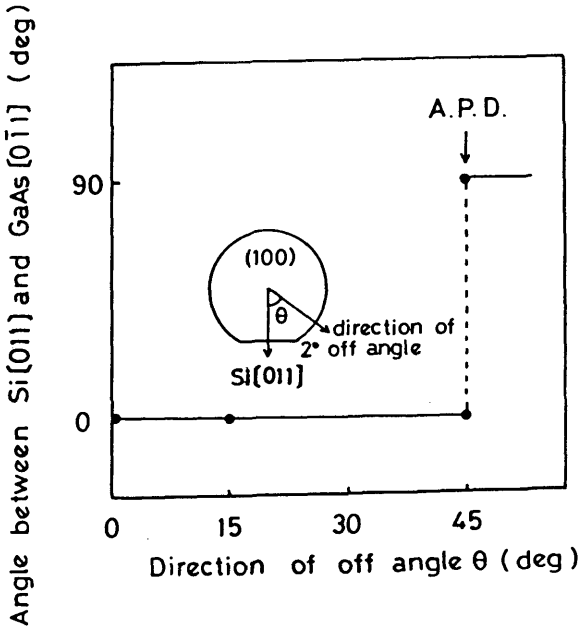

Fig. 3.2 Angle between Si[011] and GaAs[0$\bar{1}$1] vs. direction of off angle.

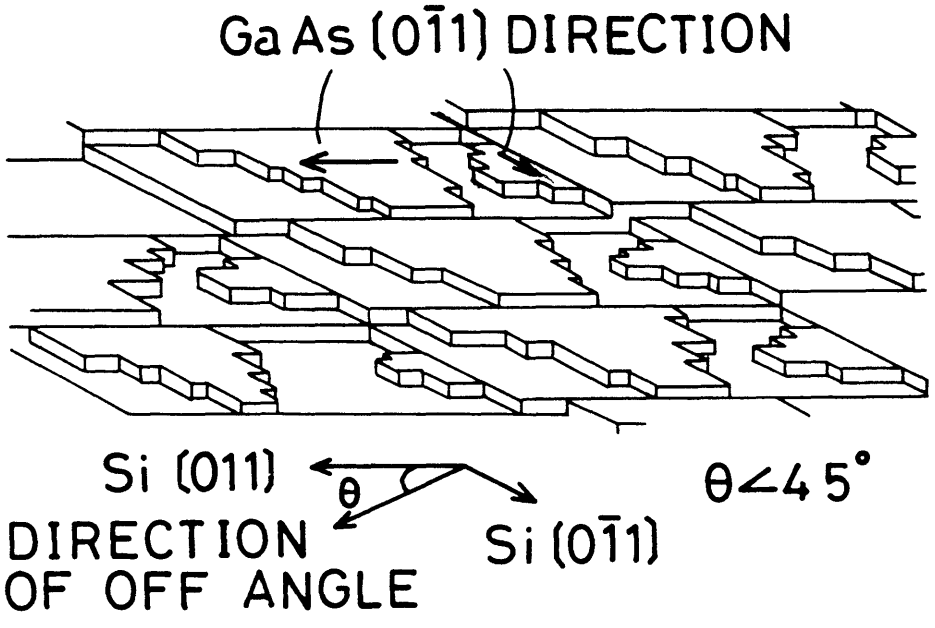

Fig. 3.3 Schematic illustration of GaAs growth on inclined (100) Si surface.

the other and dominates the succeeding growth unless θ is 45^{o} where the length of both terraces are equal resulting in the formation of an antiphase domain structure.

Let α and β to be [011] and its perpendicular directions. The terrace lengths L_{α} and L_{β} along α and β directions on (100) plane ϕ degree off from α are expressed as

$$L_{\alpha} = a_0/2\cos(\theta)/\tan(\phi)$$

$$L_{\beta} = a_0/2\sin(\theta)/\tan(\phi)$$

assuming two atomic steps, where a_0 is a lattice constant of Si. The overgrown GaAs crystal orientation is determined by the shorter terrace length as mentioned. The interesting situation occurs at $\theta = 0$ which gives $L_{\beta} = 0$. This means no atomic steps along β direction, and GaAs orientation is determined by L_{α}. But once θ deviates very small angle from 0, L_{β} is no longer 0 and dominates the growth. Thus the crystal orientation of GaAs on exactly $\theta = 0$ and θ (small angle deviation from 0) must be different, but in practical, the realization of θ to be exactly 0 is impossible.

3.3 Measurement of stress

The stress generation in the grown layer cannot be avoided as far as GaAs is rigidly connected to Si because there is about 2.5 times difference in thermal expansion coefficients between GaAs and Si, and the grown layer is cooled more than 600K from growth temperature to room temperature, resulting in the concave

bending of the wafer which produces the tensile stress in GaAs. This stress makes the lattice constant of GaAs parallel and perpendicular to the surface different, and also effects another electronic properties such as effective mass or band gap energy.

This section gives the experimental estimation of the stress by photoluminescence (PL), electroreflectance (ER), X-ray diffraction etc. when the GaAs thickness is changed.

Figure 3.4 shows the Nomarski surface microphotographs for different GaAs layers of 1, 2, 4 and 8 μm, respectively. These samples have single domain structures and mirror-like surfaces. A variation of surface morphology is observed. Figure 3.5 shows the surface fluctuation divided by the thickness of GaAs as a function of the GaAs thickness. The surface structure becomes larger with increasing thickness and the surface roughness becomes better. No crack appears on the surface even on the 8μm-thick GaAs, while cracks appear on 3μm-thick GaAs grown by the two-step growth method[8].

Figure 3.6 shows the etch pit density (EPD), revealed by molten KOH[9,10], as a function of the GaAs layer thickness. The EPD drastically decreases with increasing the thickness from 0.8 to 1.6μm and further decreases gradually with thickness. The EPD of an 8μm-thick sample is about $4000cm^{-2}$, which is about the same as the commercially available GaAs wafer. In some part of the wafer, the EPD is lower than these values and it is almost zero on an 8μm-thick layer. This figure shows that the defect density reduces with increasing GaAs thickness. These results fit into a

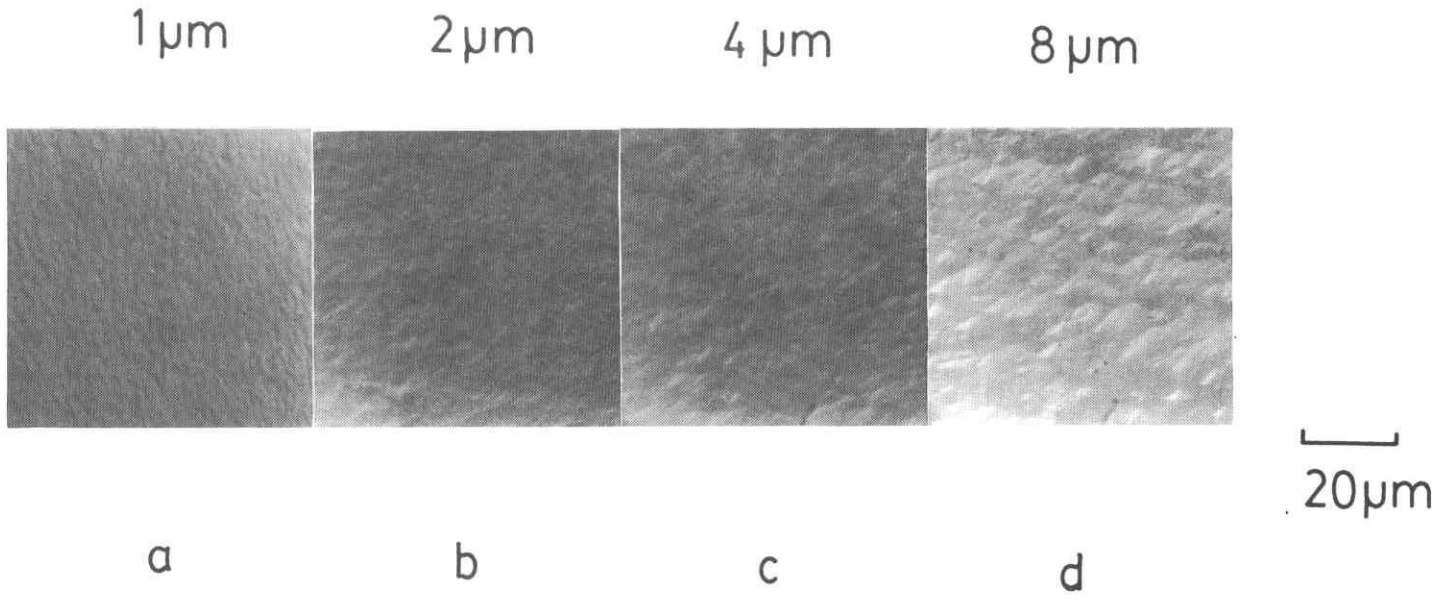

Fig. 3.4 Nomarski surface microphotographs of GaAs grown on Si. GaAs thicknesses (in μm) are (a)1, (b)2, (c)4 and (d)8.

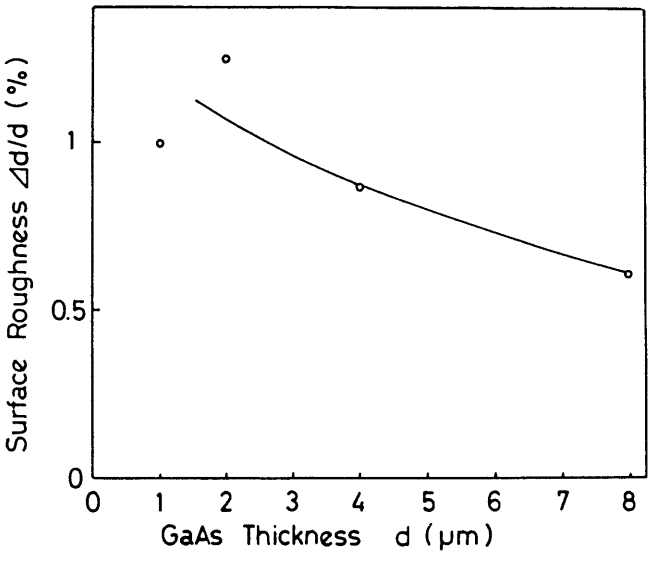

Fig. 3.5 Surface roughness of GaAs as a function on GaAs thickness.

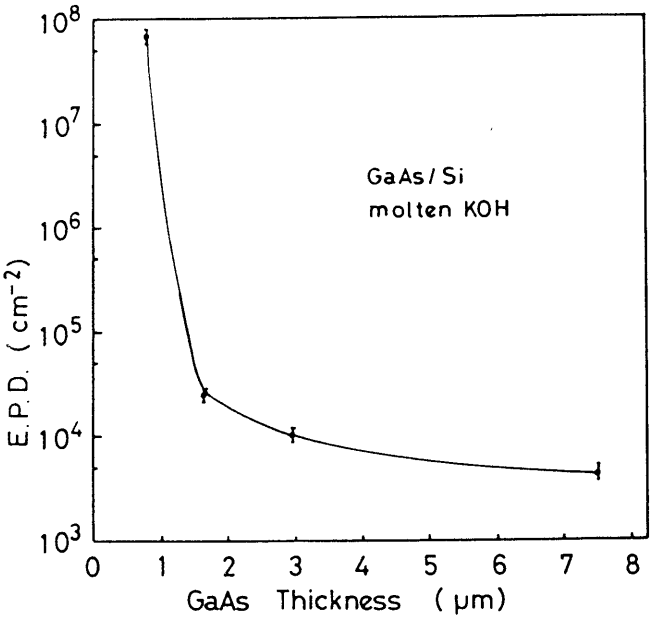

Fig. 3.6 EPD as a function of GaAs thickness.

picture with similar results, that the reduction of defects with GaAs layer thickness investigated by TEM, formerly reported for GaAs grown on Si by the two-step growth method[11]. Cracks appear only on the surface of the 8μm-thick sample after etching.

3.3.1 Photoluminescence measurement[12]

Figure 3.7 shows the typical PL spectrum at 4.2K grown on Si substrate (upper), and GaAs substrate (lower). The sample grown on GaAs has three peaks; (a), (b) and (c). The origin of these peaks has already been clarified by many authors[13-16]. The peak (a) at 1.5133eV is a bound exciton (BE) and the peak (b) at 1.4873eV is band to acceptor (BA) and donor to acceptor (DA) recombination lines from the residual impurities. The peak (c) at 1.4509eV is attributed to the LO phonon replica of the peak (b). The energy difference between (b) and (c) is 36.4meV.

On the other hand, the GaAs layer grown on Si substrate has five peaks of (A), (B), (C), (D) and (E). The PL peak wave length and the shape are almost the same as the result for GaAs grow on Si directly[17] or by the two-step growth method[18,19]. The origins of these peaks are identified as follows.

The peak (A) at 1.5022eV is due to bound excitons.

Peaks (B) and (C) are related to band to acceptor or donor to acceptor transitions. It is already known that the biaxial stress splits the degeneracy of light and heavy hole bands[20], and thus the acceptor level also splits into two levels. Peak

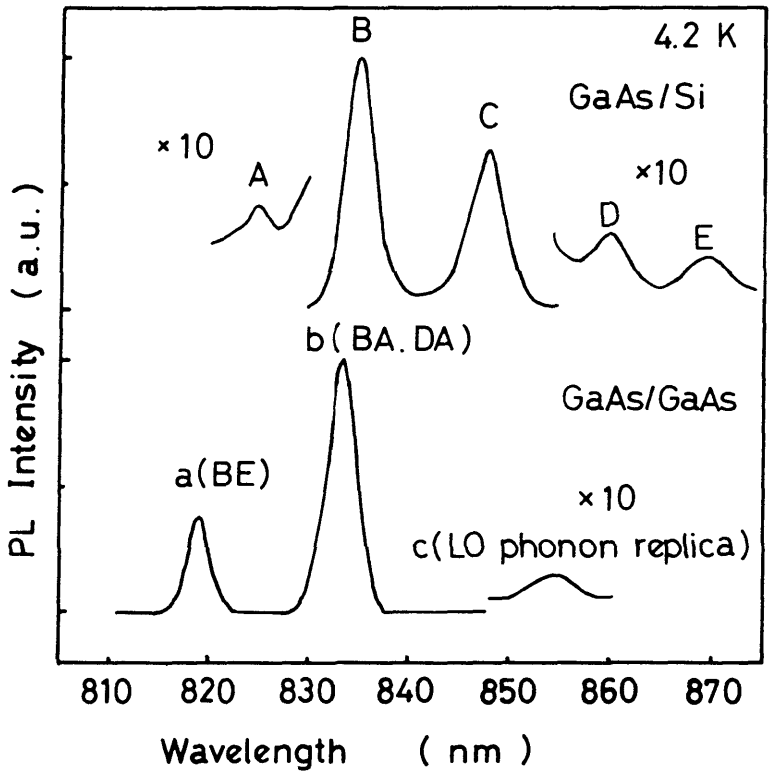

Fig. 3.7 PL spectra at 4.2K grown on Si (upper) and GaAs (lower).

(B) and (C) at 1.4838eV and 1.4611eV respectively are transition from band or donor to acceptors bound to light and heavy hole valence bands, respectively[18]. The pressure coefficients of light and heavy hole bands of GaAs are not well established but are about 7.11×10^{-9} and 0.95×10^{-9} meV/(dyn/cm^2) for uniaxial compressive stress along (100) measured by electroreflectance. Thus the energy difference is 6.16×10^{-9} meV/(dyn/cm^2)[21]. The strain in the epitaxial layer parallel and perpendicular to the surface $e_{\parallel}$ and $e_{\perp}$ respectively are measured by the Bond method to be $e_{\parallel} = 5.84 \times 10^{-4}$ and $e_{\perp} = -1.13 \times 10^{-3}$. The strain at 4.2K can be estimated to be $e_{\parallel} = 8.49 \times 10^{-4}$ and $e_{\perp} = -1.66 \times 10^{-3}$ from this result. Using these values the tensile stress applied to GaAs parallel to the surface at 4.2K is calculated to be 2.36×10^9 dyn/cm^2. Thus the estimated splitting energy of light and heavy hole bands is 14.5 meV which is a little smaller than the measured 22.7 meV energy difference of peak (B) and (C) because the applied stress is tensile.

The peak (D) at 1.4420 and the peak (E) at 1.4251 eV are due to the LO phonon replica of the peaks (B) and (C). The energy differences of the peaks (B) and (D) and peaks (C) and (E) are 41.8 meV and 36 meV, respectively. This difference may be due attributed to the tension applied to the epi-layer.

3.3.2 Curvature radius and lattice constant

Figure 3.8 shows the curvature radius of the wafer, r, and

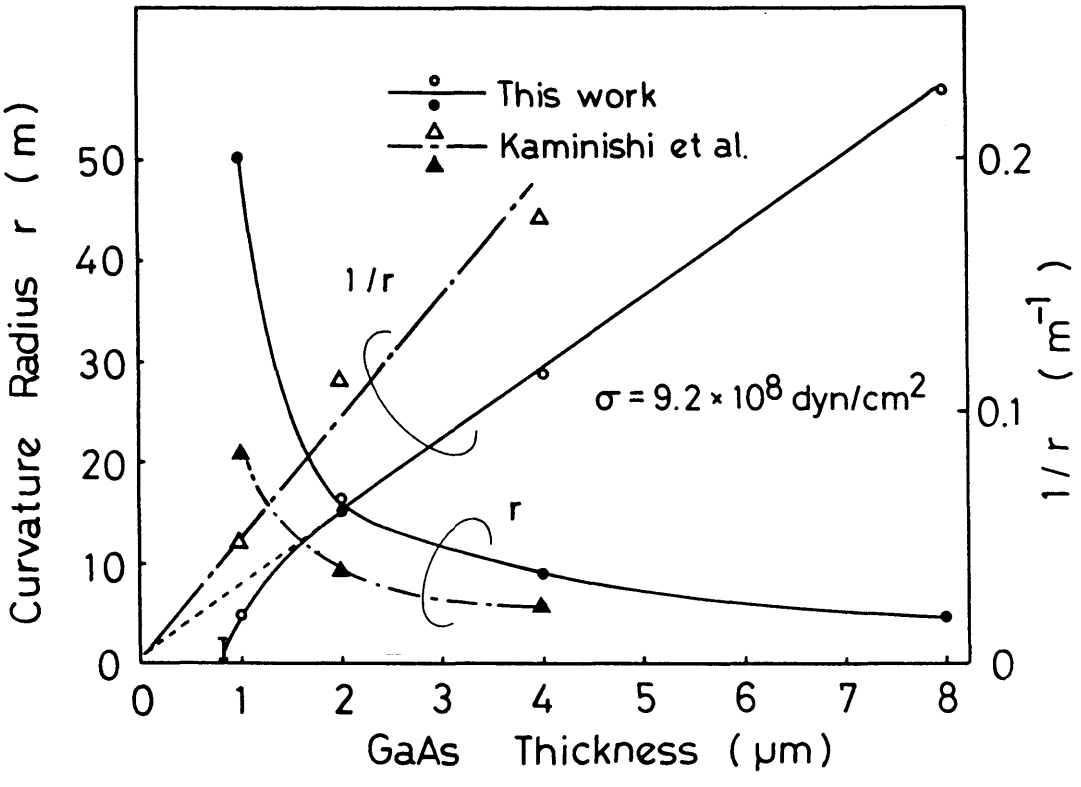

Fig. 3.8 Curvature radius of the wafer and its reciprocal as a function of GaAs thickness.

its reciplocal 1/r as a function of the thickness of GaAs. The results obtained by Kaminishi and Akiyama[22], grown using the two-step growth method, are also shown in this figure. The curvature radius r decreases and 1/r increases monotonically with increasing GaAs thickness. As the stress σ in the GaAs layer is expressed as[23]:

$$\sigma = \frac{E_{Si} b^2}{6(1-\gamma_{Si})rd} ,$$

the straight line of 1/r versus GaAs layer thickness d gives the constant stress σ of 9.2×10^8 dyn/cm^2 using E_{Si} (Young modulus of Si)= 1.3×10^{12} dyn/cm^2, b (Si substrate thickness) = 320μm and γ_{Si} (Poisson ratio of Si) = 0.3. This value of stress is about one half of the caluculated thermal stress of 1.8×10^9 dyn/cm^2, using the next equation:

$$\sigma_T = E_{GaAs}(\alpha_{GaAs} - \alpha_{Si})\Delta T,$$

where α is the thermal expansion coefficient and ΔT is the difference between growth temperature and room temperature. It is interesting to note that our data points apparently depart from a straight line when the GaAs is thinner than 1 μm, while they are on a straight line for GaAs grown on Si by the two-step growth method. Figure 3.9 shows the GaAs thickness dependence of the applied stress calculated from the curvature radius. It

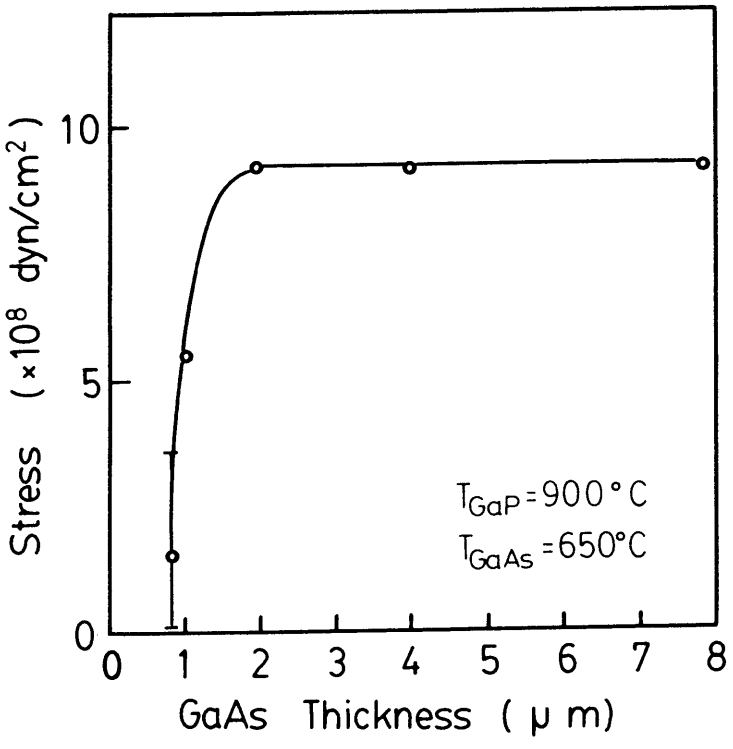

Fig. 3.9 Stress calculated from the curvature radius as a function of GaAs thickness.

increases with increasing the thickness and saturates over 2 μm.

The lattice constant of GaAs is measured by X-ray diffraction. The lattice constant parallel $a_{\parallel}$ and perpendicular $a_{\perp}$ to the surface are expanded and compressed, respectively. Figure 3.10 shows the lattice constant $a_{\perp}$ determined by X-ray (400) Bragg reflection as a function of the GaAs thickness. The lattice constant decreases with increasing thickness and saturates. The saturated value is almost coincident with the calculated value, using the following equation and taking account only the thermal stress[23]:

$$a_{\perp} = a_{GaAs}\,[1-2(\alpha_{GaAs} - \alpha_{Si})\Delta T \cdot \gamma_{GaAs}],$$

where a_{GaAs} is the lattice constant without the stress.

The photoluminescence at 4.2K is measured for different GaAs thickness. Two strong and three weak peaks are observed at the 4.2K PL spectrum, as described in the previous section. Figure 3.11 shows the PL peak energy of the two strong peaks as a function of GaAs thickness. The peak energy for a GaAs layer grown on GaAs is also indicated in this figure. The PL energy shifts toward smaller energy and saturates over 2 μm.

The experimental observations with decreasing GaAs thickness are summarized as: (1) the etch pit density drastically increases, (2) the stress calculated from curvature radius decreases, (3) the lattice constant comes near to the GaAs original value, and (4) the energy gap also approaches the originals.

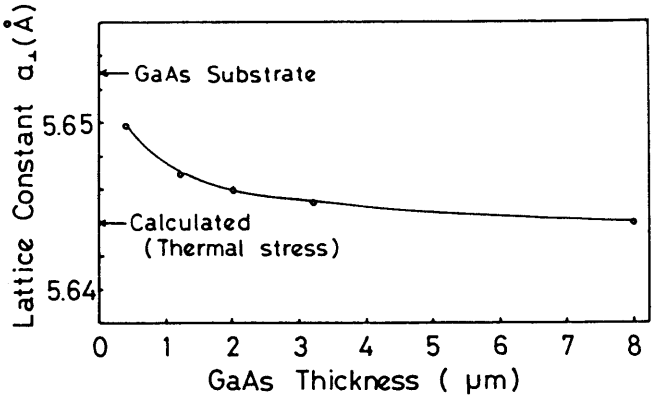

Fig. 3.10 Lattice constant perpendicular to the surface as a function of GaAs thickness.

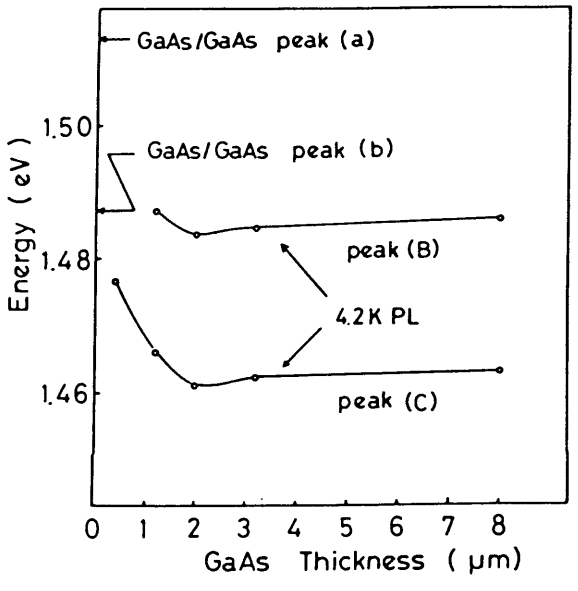

Fig. 3.11 PL peak energy as a function of GaAs thickness.

These results all suggest that the stress is relaxed by the dislocations when GaAs is thin and that the GaAs layer gradually becomes perfect with increasing thickness. But the reduction of dislocations with GaAs thickness, in turn, produces the stress of the order of 9×10^8 dyn/cm^2. This value of the stress is about one half of the caluculated thermal stress and seems smaller than the sample grown by the two-step growth method. This difference may be due to the effect of the superlattice layer used here, but the mechanism to relax the stress by superlattice layers is still in question.

3.3.3 Electroreflectance measurement[24)]

The electroreflectance (ER) spectroscopy is known as an easy and accurate technique to measure the band gap energy of the semiconductors[25)]. The electroreflectance measurement system is schematically shown in Fig. 3.12.

The electroreflectance spectra are taken using 1 mol KOH/ semiconductor contact which is electrically modulated at 100 Hz while measuring the reflectivity of the epitaxial surfaces. All the measurements are done at room temperature. The modulation voltage is low enough to give the low field spectra which is checked by the linear relation of $\Delta R/R$ versus applied voltage, where ΔR is the 100 Hz component of the reflectivity R. The band gap energy E_g and broadening parameter Γ are calculated following the method of Aspnes[25)]. The difference in E_g from the original

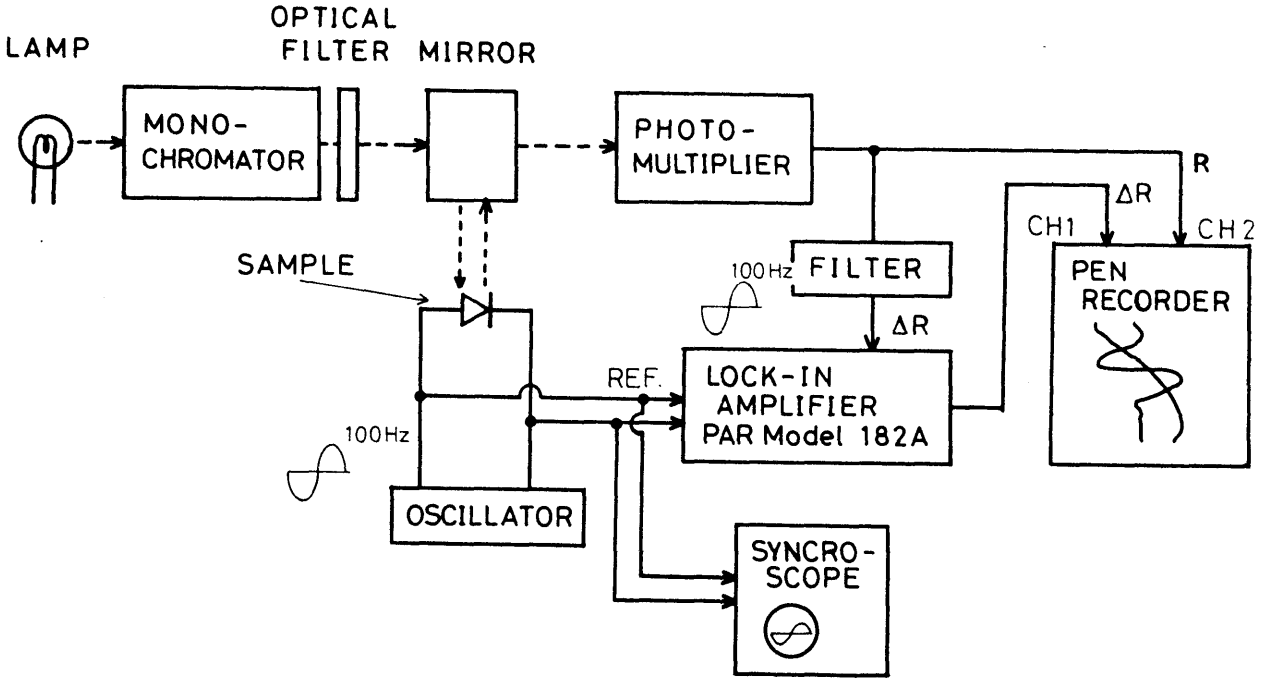

Fig. 3.12 Electroreflectance measurement system.

value of GaAs gives the stress applied to the layer assuming the constant and sufficiently low value of Γ , and Γ itself shows the crystal perfection.

The two groups of peaks are observed at around 1.45 and 1.75 eV which are due to transitions from conduction band minima to light hole valence band maxima and to split off band, respectively. But, only 1.45 eV peaks are measured here as the peak at 1.75 eV is too small to discuss the small change in its energy and broadening.

One example of ER spectra of GaAs grown on GaAs and Si substrates under the same conditions is shown in Fig. 3.13. There is no essential difference in the spectra except the slight shift in energy. It is known that the uniaxial stress applied to semiconductors splits the light and heavy hole valence bands. But, this split is responsible to the ER spectrum only when the incident-light electric field is polarized perpendicular to the stress direction (not the present situation), resulting in the same spectra of GaAs/Si as on GaAs. It is quite clear that the shift in energy is produced by the stress applied to the GaAs layer grown on Si as the peak is moved to the lower energy side by the substrate polishing which increases the stress in the epi-layer.

The band gap energy E_g and broadening parameter Γ are shown in Fig.3.14 as a function of the GaAs layer thickness. E_g gradually decreases with thickness untill about 4 μm and saturates while Γ is almost unchanged.

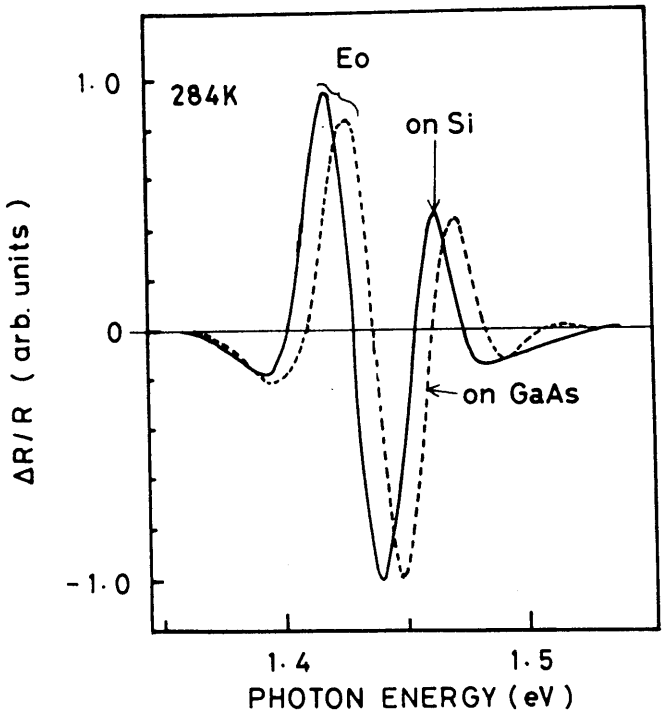

Fig. 3.13 Typical ER epectra of GaAs on Si and GaAs.

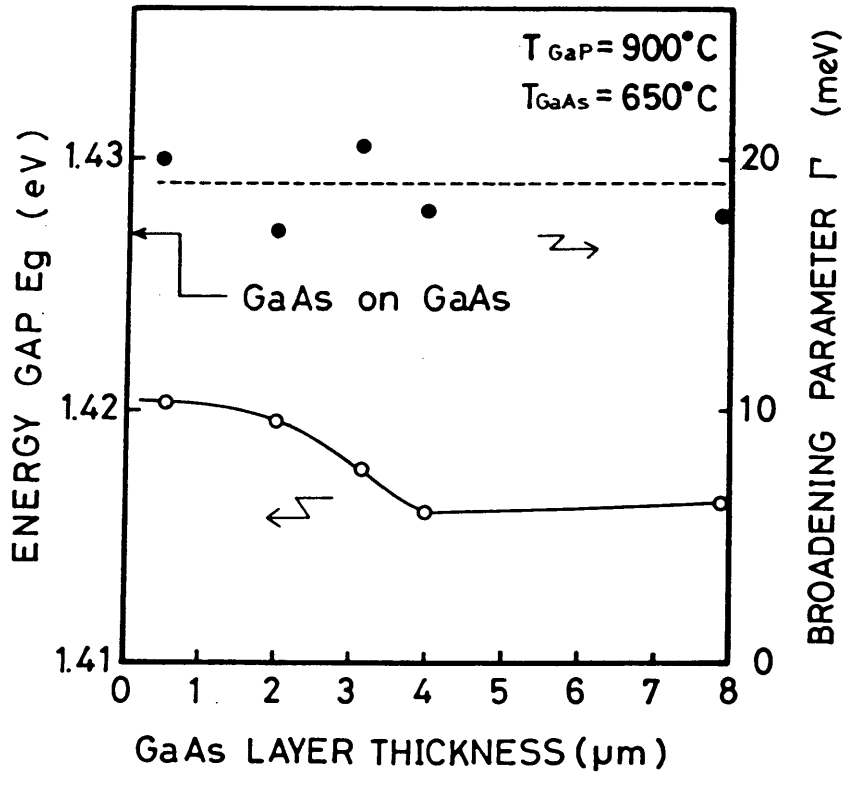

Fig. 3.14 Band gap energy and broadening parameter as a function of GaAs thickness.

The shift in band gap energy from the original value of GaAs shows the stress applied to the layer assuming a sufficiently low value of Γ. The random lattice deformation also changes energy gap, but Γ becomes large in this case. The Γ values shown in Fig. 3.14 are almost the same as on GaAs substrates (16-23meV), thus the band gap change from that of GaAs on GaAs reflects the stress applied to the layer. It should be noted that the measured stress effecting on the band gap energy shift is the stress inside the small regions when the layer is separated by the dislocations or stacking faults. It is interesting to note that the change in E_g from the original value of GaAs (even at 0.8 μm) is fairly large in spite that the measured stress from the curvature radius is very weak (Fig.3.9), and also E_g saturates at about 4 μm, while the stress saturates at 2 μm.

These observations are explained as shown in Fig.3.15[26]. If the GaAs layer is thinner than 1 μm, the high density of dislocations or stacking faults separate the layer in many small regions, resulting in a small warpage. This high density of dislocations relax some of the stress, but the stress is still kept applied to a small region and produces the shift in the band gap energy. In the medium thickness region (about 2 μm), the surface becomes connected and the stress effecting on the warpage saturates, but there are still some dislocations which relax the stress. When the thickness exceeds 4 μm, the dislocation almost disappears and stress saturates at a value determined by the difference in thermal expansion coefficients of Si and GaAs, and

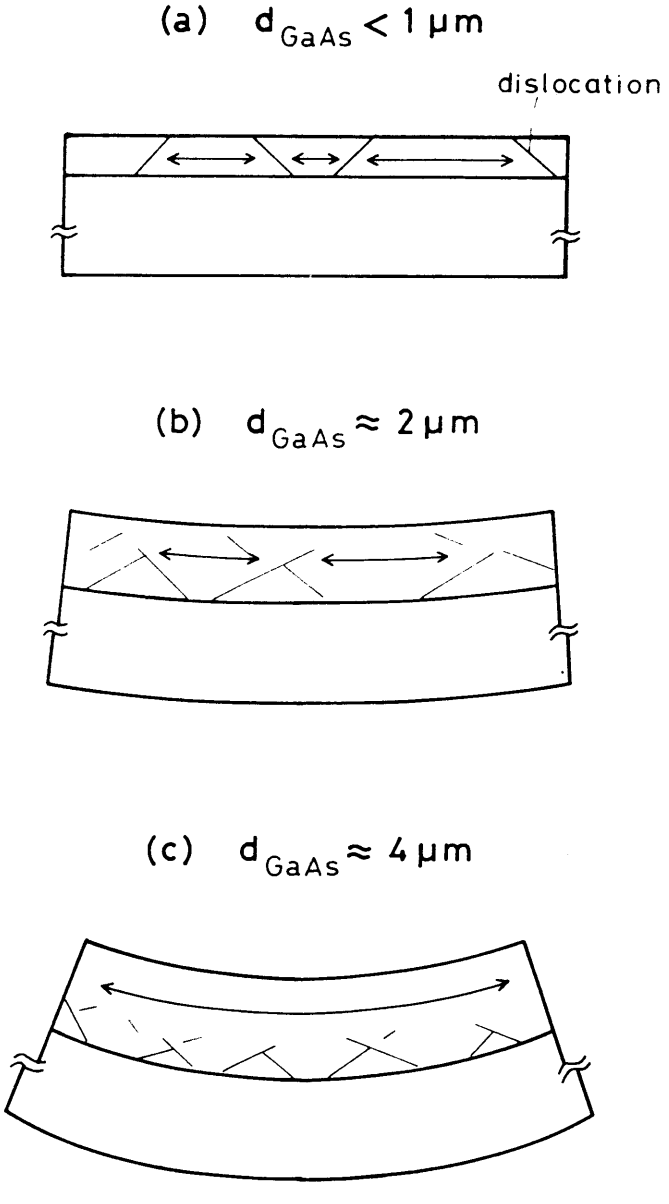

Fig. 3.15 Schematic illustration of sequence of the growth.

the warpage continues to increase to maintain a constant stress. However, some of the stress is relaxed by the dislocations or stacking faults.

As is clear from Figs. 3.6 and 3.15 the crystal becomes gradually perfect with the sequence of the growth. In other words, there is a 4 μm-thick intermediate layer in our samples, and the existence of this layer seems to relax the stress applied to the overgrown GaAs layer.

GaP/Si interface is checked by the Auger in-depth profiling as shown in Fig.3.16. The inter-diffusion of Ga, P and Si is quite clear. The thickness of the interface region extends over 20 nm which seems quite different from the two-step growth method where the atomic scale sharp interface between GaAs and Si is obtained as checked by the cross-sectional TEM[27]. The existence of this large inter-diffused layer must change the mechanism to obtain a single domain GaAs on Si and hence the characteristics of the over grown GaAs layer from those obtained by the two-step growth method. The formation mechanism of this rather thick imperfect layer must be related to the existence of this inter-diffusion layer between GaP and Si.

The band gap energies and broadening parameters are shown in Figs. 3.17 and 3.18 as functions of the growth temperatures of GaAs and GaP, T_{GaAs}, T_{GaP}, respectively for 2 μm-thick GaAs. The linear increase in Γ with T_{GaAs} shows that the crystal itself becomes worse with increasing growth temperature . The nearly same E_g at 650 - 730 ^{o}C as that of GaAs/GaAs suggests the exist-

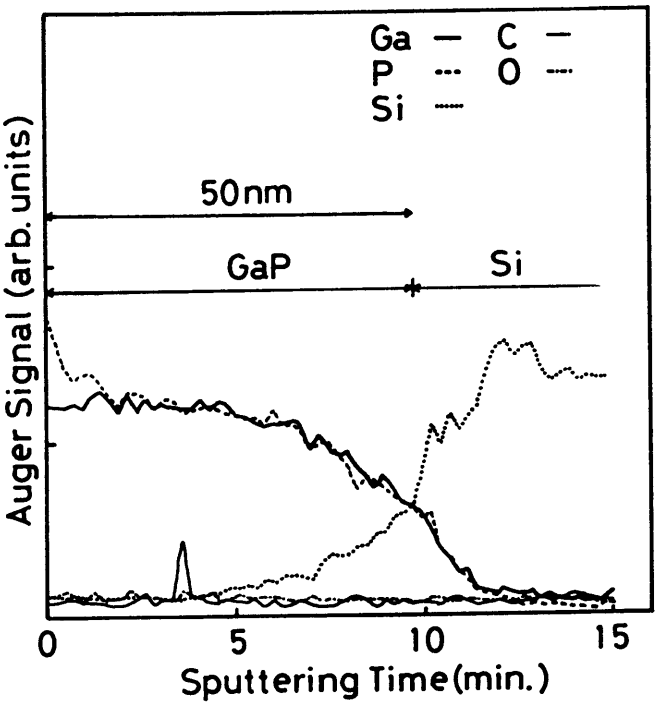

Fig. 3.16 In-depth Auger profile of GaP grown at 900°C.

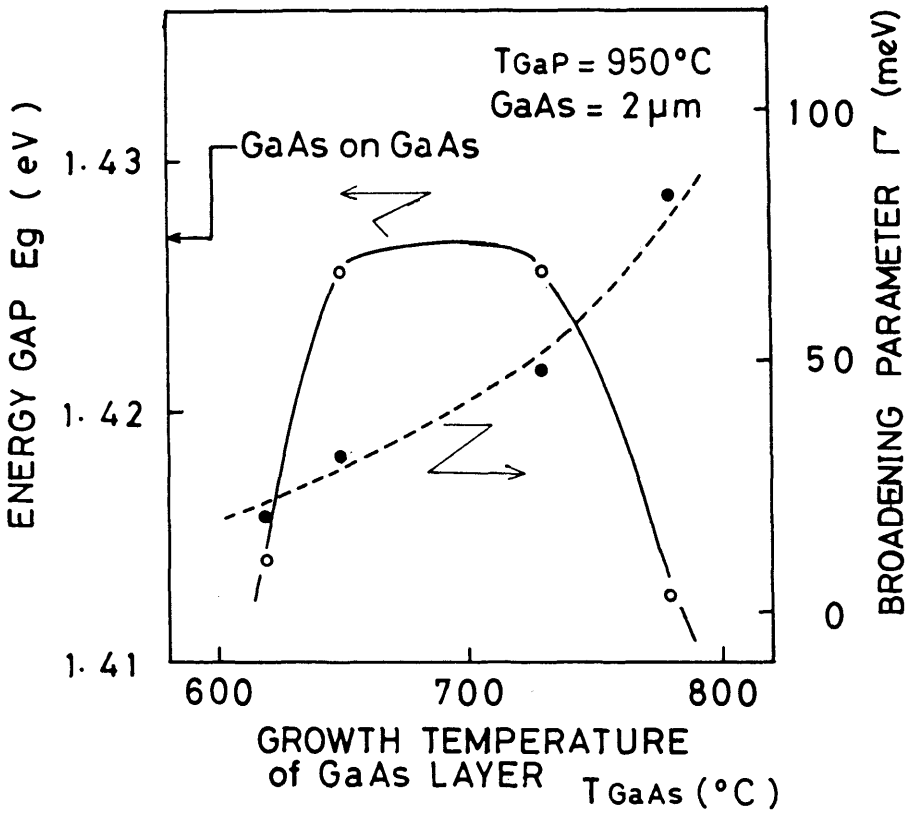

Fig. 3.17 Band gap energy and broadening parameter as a function of T_{GaAs}.

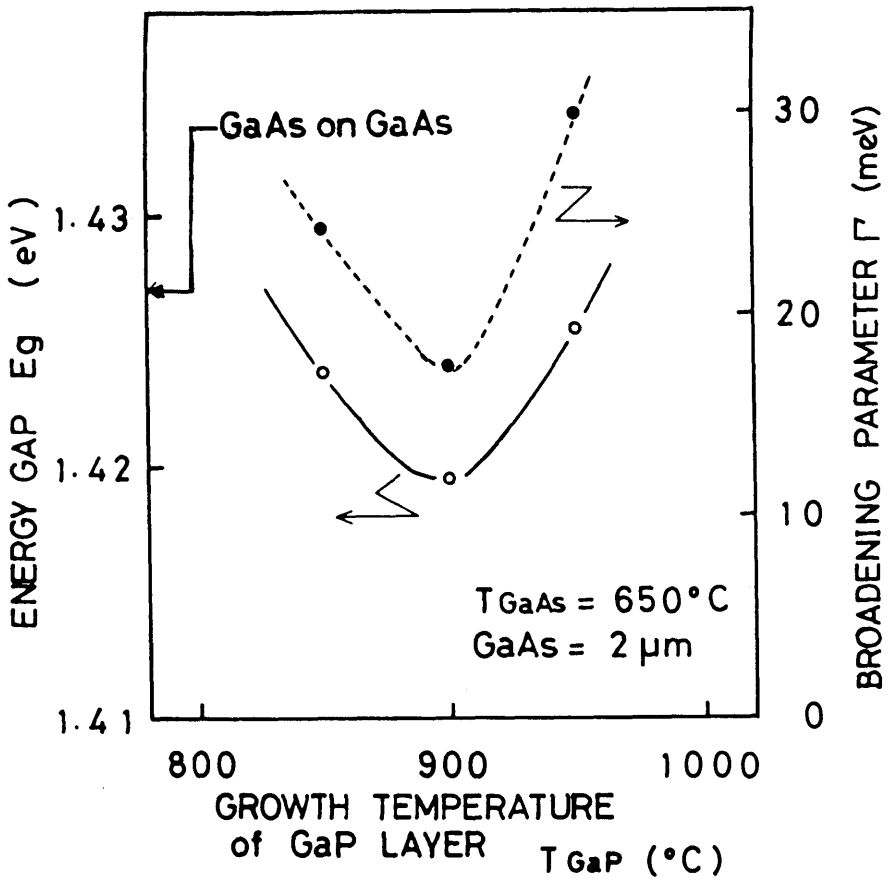

Fig. 3.18 Band gap energy and broadening parameter as a function of T_{GaP}.

ence of the high density of dislocations which relax the stress. The decrease in Eg at 780 ^{o}C is probablly due to the lattice deformation taking into account the large Γ. The photolumines-cence half width also becomes broader at this growth temperature as previously mentioned. But, it is supposed, by comparing Figs. 3.17 and 3.18, that the dependence of E_g on T_{GaAs} might be effected by T_{GaP} showing both T_{GaAs} and T_{GaP} to have the impor-tant effect in generating the dislocations. The lower T_{GaAs} gives the better crystal, but the surface becomes worse for T_{GaAs} lower than 620 ^{o}C.

Both E_g and Γ have minimum at T_{GaP}=900 ^{o}C as shown in Fig.3.18 which indicates the growth temperature of the first GaP layer has significant effects on the crystal perfection and defect formation in the overgrown GaAs layer.

3.4 Measurement of deep levels[28)]

Deep levels in GaAs on Si substrate are investigated by DLTS (deep level transient spectroscopy)[29)], which is the most familiar and accurate technique for the study of deep levels, because deep levels play important roles in the device perform-ance. The nature of the deep level in GaAs on Si must be dif-ferent from that on GaAs substrate by the auto-doped Si into the epi-layer, stress in the layer and induced defects.

In this section, deep levels in GaAs grown on Si substrate are investigated by DLTS and compared to those in GaAs on GaAs.

3.4.1 DLTS measurement

Schottky and ohmic contacts are fabricated by evaporating Au and Au/Sn on the epi-layer, respectively. All the grown layers are undoped and n-types having a mirror-like surface.

Deep levels are characterized by a conventional DLTS measurement. The rate window (τ^{-1}) is changed from 51 to 512 sec^{-1}, the reverse bias voltage is 1V and the bias pulse height and width are 1V and in the range 5 μsec - 1msec, respectively. The temperature of the sample is varied from 100K to 450K, which is carefully measured by a thermocouple. The DLTS measurement system is schematically shown in Fig.3.19.

3.4.2 Deep levels in GaAs on Si

Figure 3.20 shows a typical DLTS spectra for a 2 μm-thick GaAs layer grown on GaAs (upper) and (100)2^{o} off Si (lower) (solid lines). Only one trap is observed in the sample grown on GaAs while two electron traps are seen in GaAs on (100)2^{o} off Si. The activation energies of these peaks are 0.73eV below the conduction band for GaAs on GaAs and 0.44 and 0.73eV for GaAs /Si as shown in Fig.3.21. The energy level E_{ct}, the trap concentration N_t and the capture cross section σ_n of these traps are summarized in Table 3.1. The 0.73 eV trap is thought to be EL2, very popular in MOCVD grown GaAs[30,31].

The nature of 0.44eV trap is investigated in more detail.

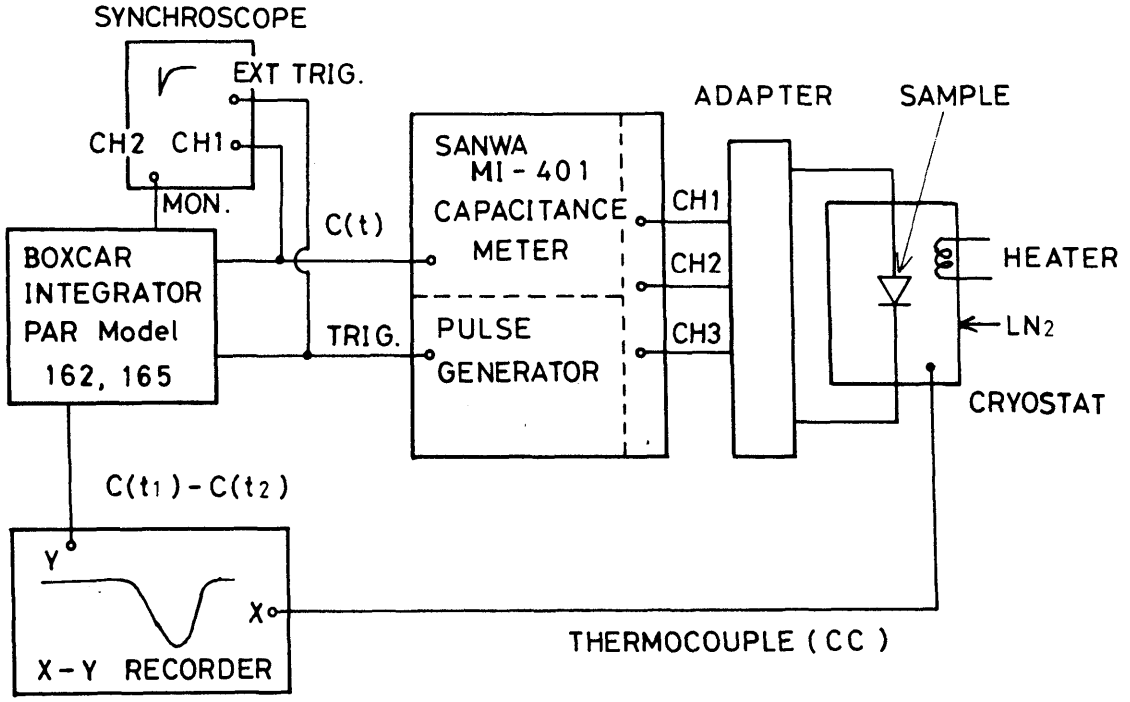

Fig. 3.19 DLTS measurement system.

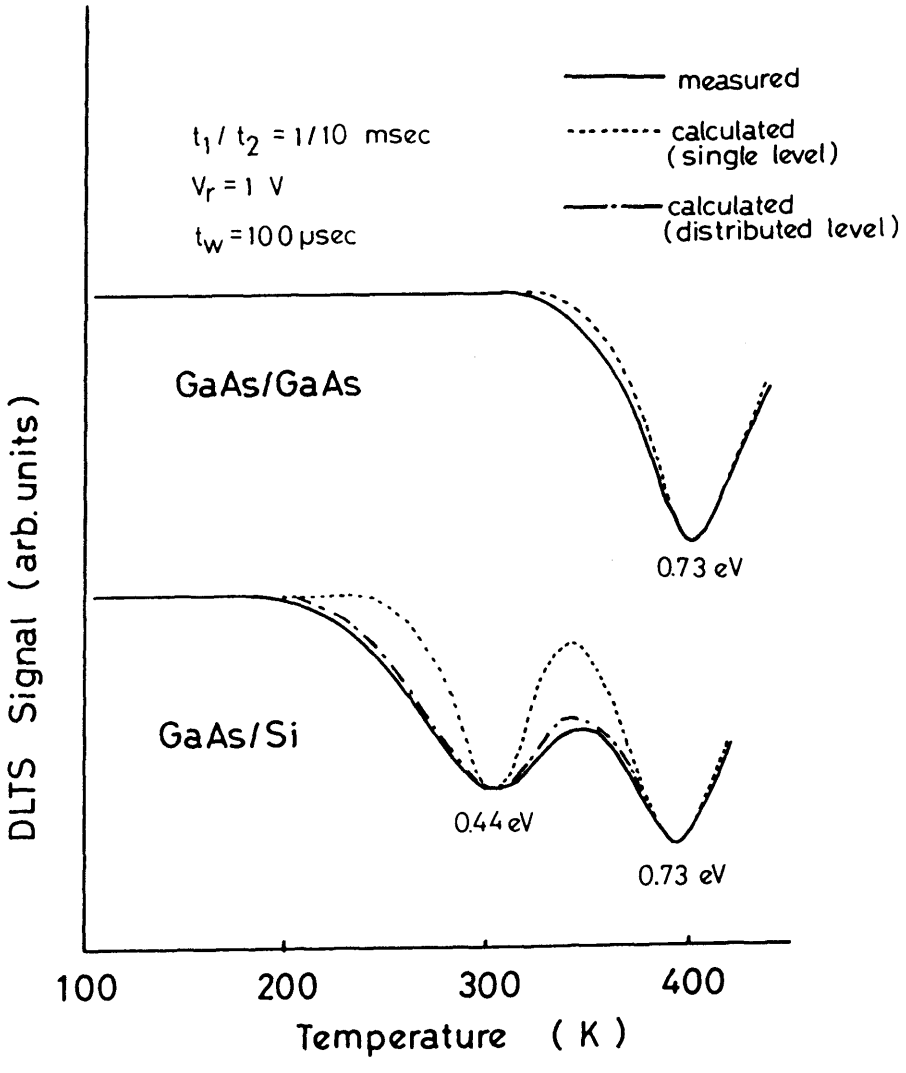

Fig. 3.20 Typical DLTS spectra of 2μm-thick GaAs grown on GaAs and Si.

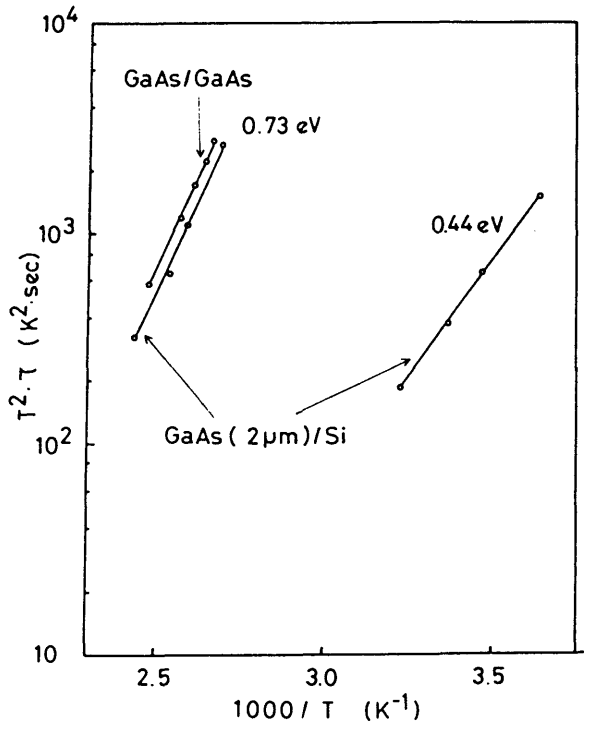

Fig. 3.21 Arrhenius plots of deep levels.

Table 3.1 Summary of deep levels observed in 2μm-thick GaAs grown on GaAs and Si.

Sample	E_{ct} (eV)	N_t (cm^{-3})	σ_n (cm^2)
GaAs/GaAs	0.73	8.0×10^{13}	1.7×10^{-14}
GaAs/Si	0.73	3.4×10^{14}	3.1×10^{-14}
	0.44	2.7×10^{14}	6.1×10^{-16}

Figure 3.22 shows the carrier and trap concentrations as a function of GaAs thickness. The carrier concentration decreases and saturates over 2 μm at about 2.0 x $10^{16}cm^{-3}$. On the other hand, the both trap concentrations decrease with increasing GaAs thickness. Figure 3.23 shows the capture cross section of a 0.44eV trap being decreased with increasing thickness while that of a 0.73eV trap is almost unchanged.

It was reported that the electron trap at 0.47eV (EB4) was induced when undoped VPE (vapor phase epitaxy) grown GaAs on Si-doped GaAs was deformerd at the temperature higher than 600 ^{o}C and its concentration increased with increasing Si concentration in the GaAs substrate[32]. This level was attributed to the Si-defects complex. The 0.44eV level seen in GaAs on Si must be related to this EB4 as the substrate is Si itself and the wafer is bent due to the difference in the thermal expansion coefficients between GaAs and Si. The decrease in the trap concentration with increasing GaAs thickness must be due to the reduced auto-doped Si in GaAs.

The calculated DLTS spectra using experimentally obtained deep level energy and capture cross section are also shown in Fig.3.20 by broken lines. The spectra of EL2 coincide with the calculated curves for both samples, but the experimental spectrum is broader than the calculated EB4. If this broading is due to the stress, the broadening in EL2 should also be observed, but this is not the case here. Figure 3.24 shows the DLTS half width of EB4 and the calculated value assuming a single level as a

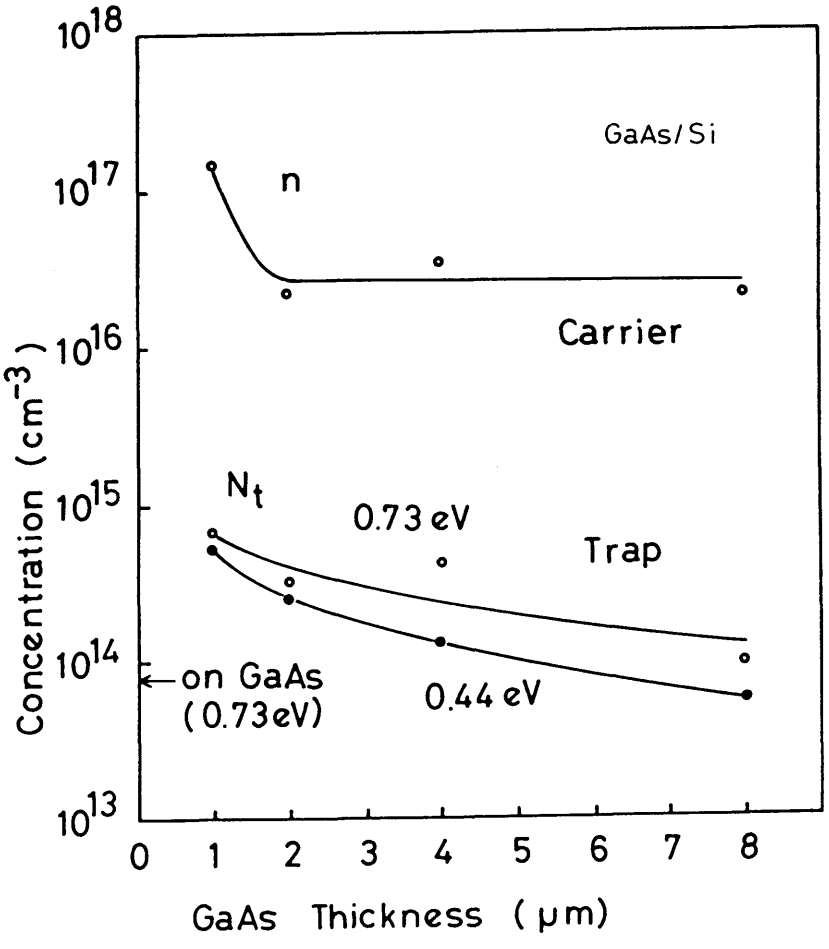

Fig. 3.22 Carrier concentration and trap concentration as a function of GaAs thickness.

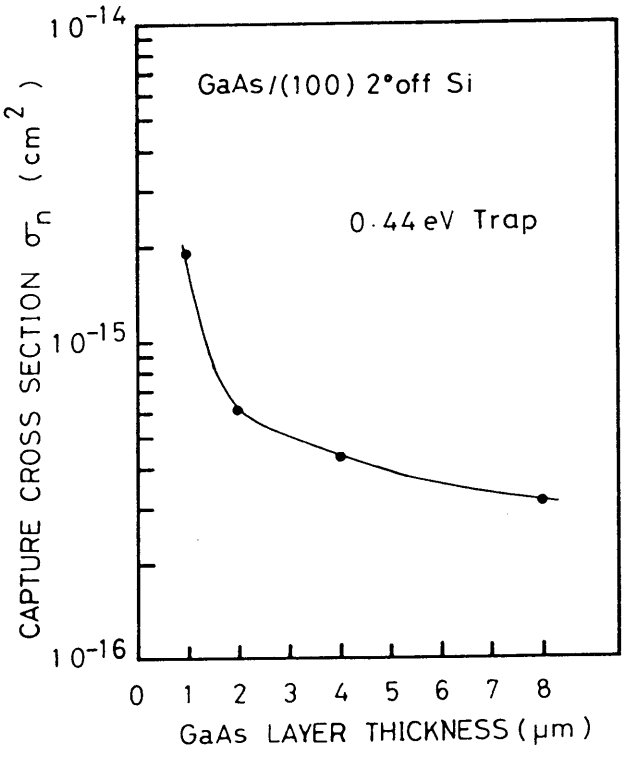

Fig. 3.23 Capture cross section of 0.44eV trap as a function of GaAs thickness.

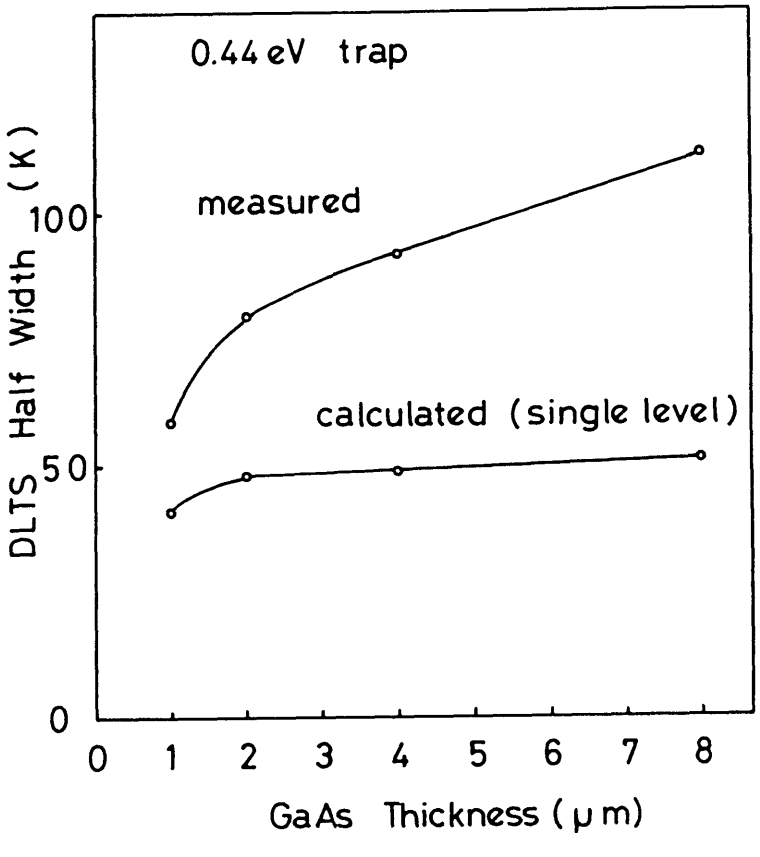

Fig. 3.24 DLTS half width of 0.44eV trap as a function of GaAs thickness.

function of GaAs thickness. The half width increases with increasing the thickness while the calculated value is almost unchanged.

These observations suggest the existence of several levels around 0.44eV. It is difficult to explain these results by considering only two or three levels or several levels and the broad background level having the different dependence on GaAs thickness, because the trap concentration, cross section and broading change very smoothly with thickness. It seems that one origin having energy distribution changes its shape with the sequence of the growth. In considering Si-dislocation complexes, the site of Si atom in dislocation must be taken into account. If the size of dislocation is sufficiently large, there are so many states for a Si atom to take its site, and each of them must have different but very close energies. This results in the continuous distribution of trap density rather than the discrete levels. The distribution of this trap is Gaussian centered at some energy as the Si atom can select its site at random. DLTS spectra are calculated for this distributed trap levels while assuming a constant capture cross section in energy. The DLTS spectrum is expressed as follows,

$$S(T) = \Delta C \int_0^{E_g} \frac{1}{V\sqrt{2\pi}} \exp\left(-\frac{(E-\bar{E})^2}{2V^2}\right)\left(\exp\left(-N_c v_n \sigma_n T^2 t_1 \exp\left(-\frac{E}{kT}\right)\right)\right.$$

$$\left.-\exp\left(-N_c v_n \sigma_n T^2 t_2 \exp\left(-\frac{E}{kT}\right)\right)\right)dE$$

where ΔC is a peak value of the capacitance change, V is a variance of the trap concentration in energy, $\bar{E}$ is a deep level center energy, N_c is a effective density of states of electron, v_n is a mean thermal velocity, σ_n is a capture cross section and E is the energy below the conduction band. To calculate the trap distribution, the variance V is determined so as to give the best fitting of the calculated DLTS spectrum to the experimental using the total trap concentration given in Fig. 3.22. An example of the best fitted spectrum is shown in Fig. 1 by a dash dotted line. Figure 3.25 shows the calculated trap concentration distribution in energy for different GaAs thickness. The decrease in total concentration with thickness must be due to the reduction in densities of the dislocation and Si. The decrease in capture cross section with thickness shown in Fig. 3.23 must correspond to a defect size reduction which also related to the broadening of the level. The detailed mechanism of energy broadening with decreasing size of defects is not clear yet.

The curvature radius of 2 μm-thick GaAs on Si substrate is about 15m, producing the stress of about $9 \times 10^8 dyn/cm^2$. The curvature radius is decreased by polishing back side of the

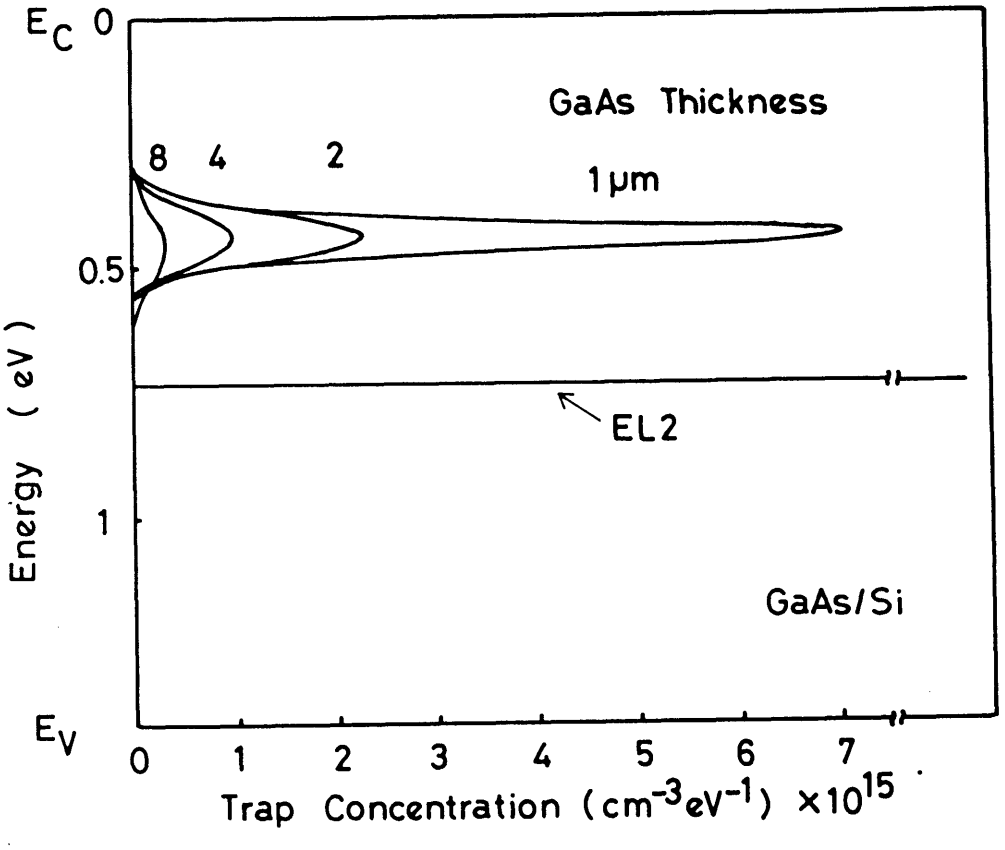

Fig. 3.25 Calculated trap levels in GaAs on Si.

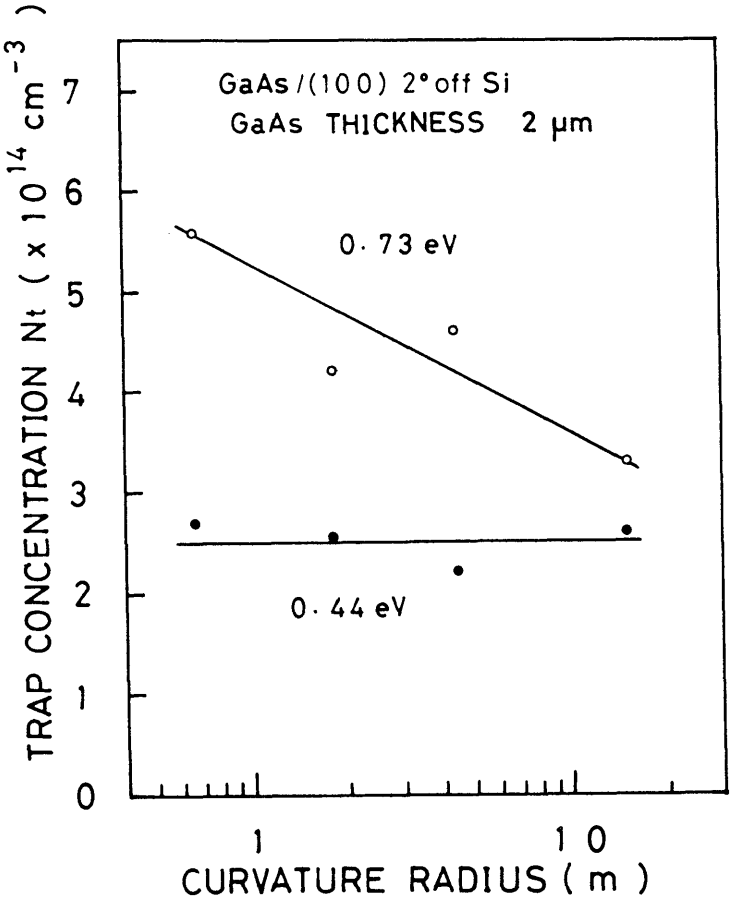

Fig. 3.26 Trap concentration as a function of the curvature radius of the wafer.

substrate and DLTS measurement is performed. The result is shown in Fig.3.26. The trap concentration of EL2 increases with decreasing the curvature radius but that of EB4 is unchanged. This result also supports that the 0.73eV trap is being originated from a point defect[33,34], but the 0.44eV trap is related to the dislocation that is not affected by the wafer bending.

3.5 Characteristics of p-n junction[35]

GaAs solar cells fabricated on Si substrates have many advantages over conventional GaAs cells, such as low cost, large area, light weight and high efficiency forming p-n junctions both in GaAs and Si. Up to now, several authors have described the GaAs solar cells on Si, but the obtained results are still far from satisfaction[36].

In this section, the very primitive results of the p-n junction characteristics formed in GaAs layers grown on Si which are the most important properties to fabricate and design the solar cells on Si substrates are described.

The fabricated diode structure to evaluate the p-n junction properties is shown schematically in Fig. 3.27. The structure and the growth procedure are as follows.

GaAs is grown on Si substrate with the intermediate layers described in chapter 2. p-n junction layer and AlGaAs window layer are grown at 650 ^{o}C. The total layer thickness is about 4 μm. The window layer thickness is 150 nm. The substrates are Si

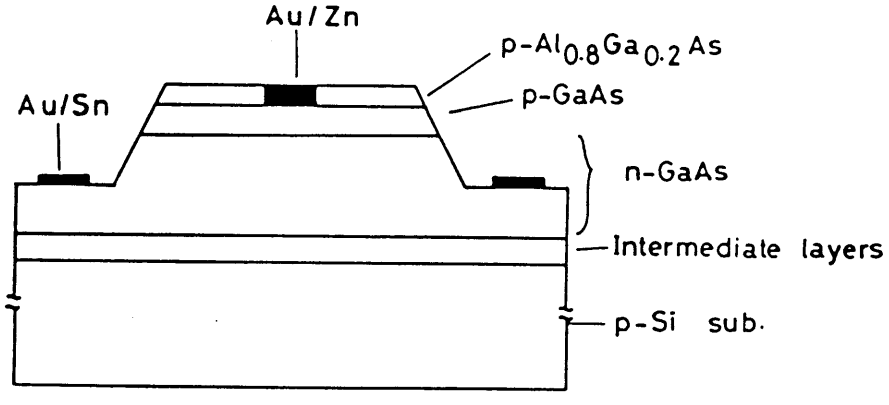

Fig. 3.27 Schematic illustration of the fabricated diodes.

having the surface orientation of (100) 2^{o} off toward [011] $+15^{o}$.

The p-type layer is formed by Zn doping using DEZ as a source, and n-type layer is undoped. The carrier concentrations in n and p layers are 1×10^{16} and 5×10^{18} cm^{-3}, respectively. After the growth, a part of the wafer is etched down to n-GaAs layer to make ohmic contact in this layer as shown in Fig. 3.27.

The current voltage characteristic of the diode shown in Fig.3.27 is shown in Fig.3.28 together with the diode fabricated on GaAs substrate under the same conditions as on Si. The diode factors n for both samples are about the same to be 2, but the reverse saturation current I_0 of the diode on Si is about two orders of magnitude larger than that on GaAs substrate, showing the existense of some recombination current.

The EBIC (electron beam induced current) measurements are performed for the diodes on Si and GaAs substrates as shown in Fig.3.29. The EBIC signal of the diode on Si does not show the simple exponential decay, as the diffusion length and hence the carrier life time are functions of distance from the Si/GaAs interface, and there is a high density of recombination centers near the interface which change the shape of the hole population in n-type GaAs layer.

On the other hand, there are two exponential decays in the diode on GaAs substrate. The reason is not known yet, but it will probablly due to the Zn diffusion from p layer into n-GaAs changing the carrier concentration near the p-n juncton. The gradients of the exponential decay give the diffusion lengths of

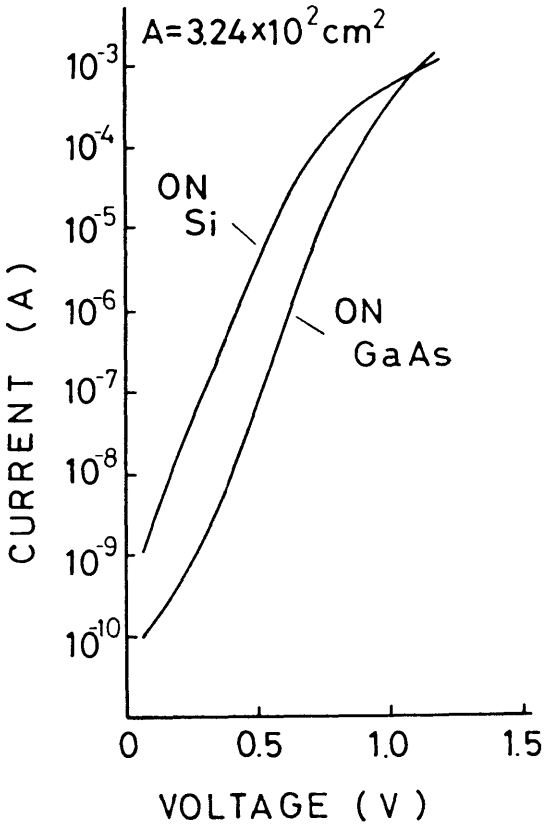

Fig. 3.28 Current voltage characteristics of the diode grown on GaAs and Si.

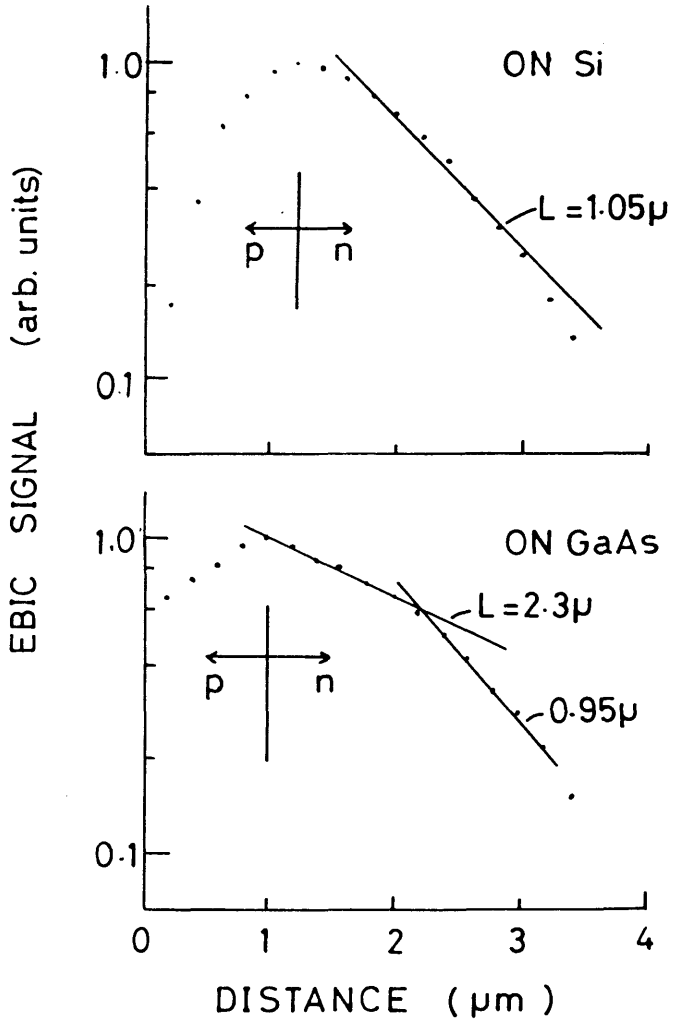

Fig. 3.29 Results of the EBIC measurement.

holes in n-GaAs to be 1.05 and 2.3 or 0.95 μm for the diodes on Si and GaAs substrates, respectively. Although there is a difference in these values, this difference is not so serious, as the EBIC signal on Si substrate is not exponential and the interfacial recombination makes the apparent exponential gradient steep, resulting in the under estimate of the diffusion length.

On the other hand, there is a clear difference in the electron diffusion length in p-GaAs. This result shows the electron diffusion length is much more sensitive to the crystal perfection compared to the holes in n-GaAs. But, there is still in question whether the shorter electron life time in p-GaAs or the fast interfacial recombination velocity are affecting the apparent diffusion length.

Figure 3.30 shows the spectral response of the diodes on Si and GaAs. There is not so much difference between the diodes except the slight shift in band gap for the diode on Si toward longer wavelength due to the stress applied to the layer produced by the thermal expansion coefficient difference of Si and GaAs.

According to the above mentioned results, the suitable solar cell structure becomes clear. Namely, there is an advantage to use a double heterostructure instead of the conventional single heterostructure. The structure must be first n-AlGaAs hole blocking layer, n-GaAs, p-GaAs photo-absorbing layer, and final AlGaAs window layer on intermediate layers on Si substrate. The first hole blocking layer prevents the photo-generated holes in n-GaAs to recombine at the interface region. Thus, the energy gap

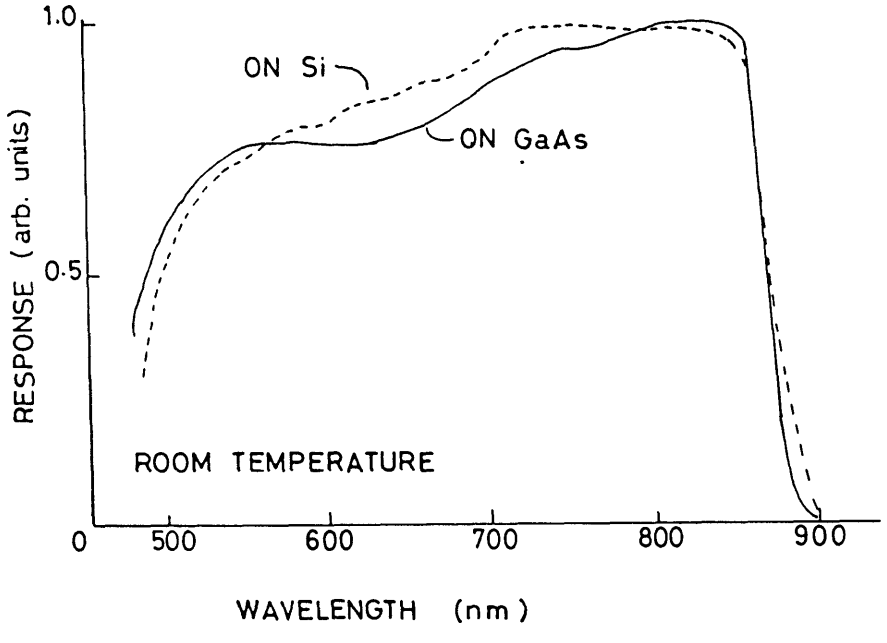

Fig. 3.30 Spectral photo-responses of the diodes grown on GaAs and Si.

difference at GaAs/AlGaAs interface must be larger than about 150 meV to prevent the carrier leakage.

The next point is the lower apparent electron diffusion length in p-GaAs layer. Thus, the p-GaAs layer must be as thin as possible.

3.6 Conclusion

The characteristics of GaAs grown on (100)2^{o} off Si substrates with strained layer superlattice intermediate layers are described. The relationship between the direction of off angle and the crystallographic structure of GaAs and the conditions to obtain a single domain structure are made clear. The grown GaAs layer is characterized by PL, ER, X-ray diffraction, DLTS and EBIC. It is found that the high quality GaAs is obtained by growing layer thicker than 4 μm. And the existence of relatively thick low grade GaAs layer between GaAs and Si seems to relax the stress produced by the thermal expansion differences, comparing with the results of GaAs grown by the two-step growth method. Two electron traps with the activation energies of 0.73 and 0.44 eV are observed for GaAs grown on Si, but only 0.73 eV trap is detected for GaAs on GaAs. The p-n junction characteristics for the solar cell application in GaAs on Si substrates are still inferior to that on GaAs, but much improvement can be expected by optimizing the growth procedure and the device structure.

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Chapter 4. AlGaAs/GaAs double heterostructure lasers on Si substrates

4.1 Introduction

The fabrication of lasers on Si substrates makes it possible to produce OEIC's which contain GaAs optical and Si electronic devices.

When this experiment was started, only the laser which operated at 77K was fabricated on Si by MBE[1]. Recently, a few lasers which operate at room temperature have been fabricated on Si[2,3] by MBE.

This chapter gives room temperature operation oxide stripe AlGaAs/GaAs double heterostructure lasers and transverse junction stripe lasers on Si substrates grown entirely by MOCVD[4-7].

4.2 Oxide stripe lasers

One feature of a laser diode (LD) on Si is the low thermal resistance of Si[8]. Figure 4.1 shows the calculated thermal resistance of the stripe LD on Si and GaAs. The method and values used in the calculation are the same as in ref.9. It should be noted that the thermal registance <R> of Si substrate-junction up configuration is only 1.5 times of <R> of GaAs substrate-junction down configuration in spite of the difference of 2.3 times for GaAs substrate at the stripe width of 10 μm.

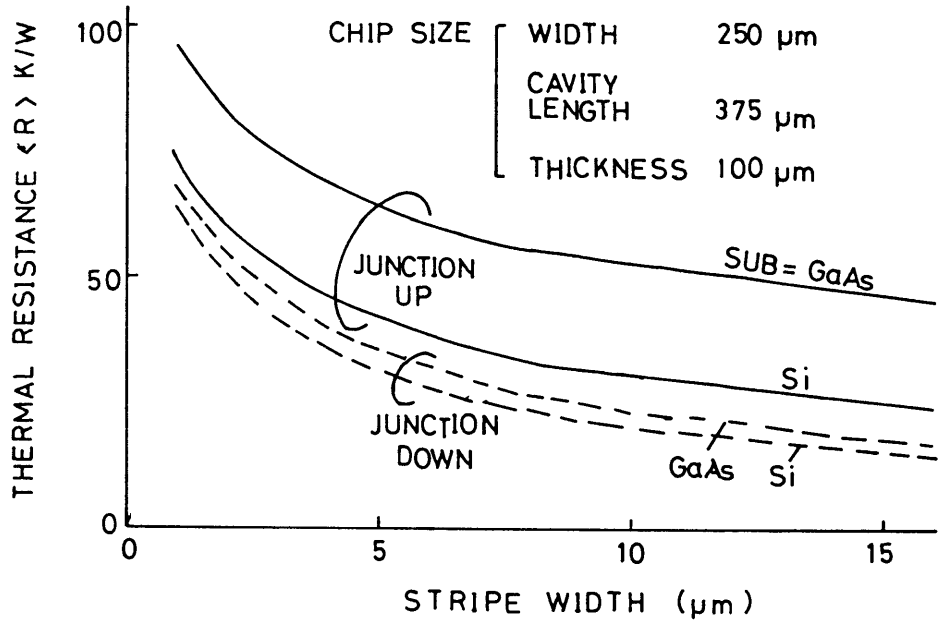

Fig. 4.1 Calculated thermal resistance of stripe LD on Si and GaAs as a function of stripe width.

This indicates that LD on Si can easily be operate under a junction up configuration.

The structure of the fabricated LD and the cross sectional scanning electron microphotographs are shown schematically in Fig. 4.2. After the growth of the intermediate layer on p-(100)2^{o} off Si as described in chapter 2, the usual double heterostructure of an Se-doped n-GaAs (2.1 μm, n=2 x 10^{18} cm^{-3}), an Se-doped n-$Al_{0.3}Ga_{0.7}As$ (1.5 μm, n=1 x 10^{18} cm^{-3}), an undoped GaAs (0.12 μm), a Zn-doped p-$Al_{0.3}Ga_{0.7}As$ (1.5 μm, p=2 x 10^{18} cm^{-3}) and a Zn-doped p-GaAs (0.4 μm, p=2 x 10^{19} cm^{-3}) are grown at 675 ^{o}C. The total epitaxial layer thickness is about 6 μm.

After the growth, a part of the wafer is etched to reveal n-GaAs for ohmic contact, SiO_2 is sputtered on p-GaAs, forming 10 μm wide stripe contact on p-GaAs, and Au/Zn and Au/Sn ohmic electrodes are formed by vaccum evaporation and photolithographic lift-off on p-GaAs and n-GaAs surfaces, respectively. The back surface of the Si substrate is then polished down to 50 μm, and the cavity is formed by the usual cleaving using a knife edge. As GaAs and Si have different cleavage planes, the cleaved facet of Si is not flat. However, the facet of the epitaxial layers tends to show a flat surface in most case. The chips are mounted on a Cu heat sink with a p-side up configuration and tested. In this process the cracks are formed in the etched grooves along the stripe, as the etched part is thinner and more fragile than the other part of the wafer. This means that the stress is still applied to the epitaxial layer even using superlattice inter-

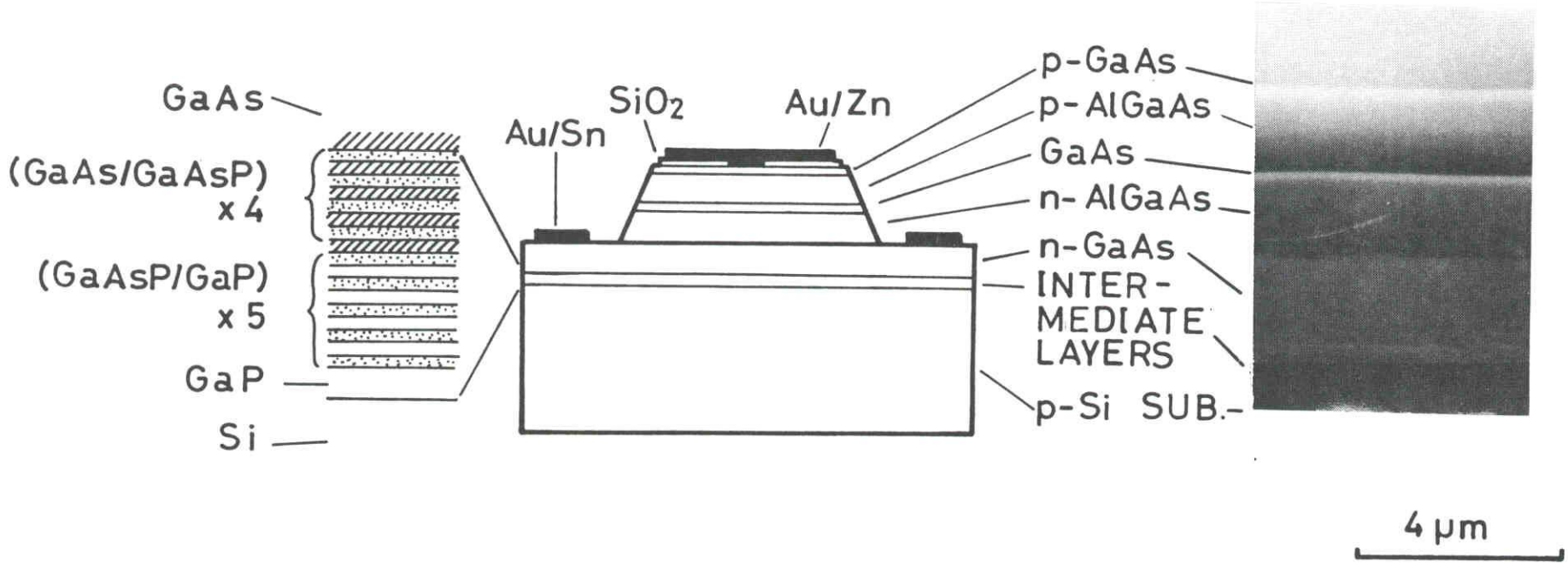

Fig. 4.2 Schematic illustration of the fabricated LD on Si and SEM microphotograph of the grown layer.

mediate layers, but some of the stress may by relaxed by this crack formation. These cracks do not affect the laser characteristics.

Figure 4.3 shows the current to voltage relation of the LD. It is obvious that the good p-n junction is fabricated on Si.

Figure 4.4 shows the current to output power relation of the fabricated laser diode at 16.5 ^{o}C, pulsed conditions. The pulse width and repetition rate are 200ns and 1kHz, respectively. The near field pattern is also shown in Fig.4.5. Although the stripe width opened on top of the p-GaAs is 10 μm, the current spreads into the grown layer over 31 μm as the current flows laterally across the grown layer, and the emission from both sides of the stripe is strong. The threshold current (I_{th}) is 450mA, which corresponds to a threshold current density of 4.9kA/cm^2.

Figure 4.5 shows the lasing spectra of the diode shown in Fig.4.2. At 700mA the diode lases at two main wavelengths while it becomes single mode at 800mA. This behavior is frequently met in broad contact lasers on GaAs substrates.

Figure 4.6 shows the temperature dependence of the threshold current I_{th}. The characteristic temperature T_0 of 179K is fairly high taking account the junction up configuration and the high threshold current density, which means a high rate of heat generation. This high value of T_0 shows the superiority of higher thermal conductance of Si compared to GaAs.

The DH lasers are grown on GaAs substrate under the same conditions as on Si for comparison. The structure is the same as

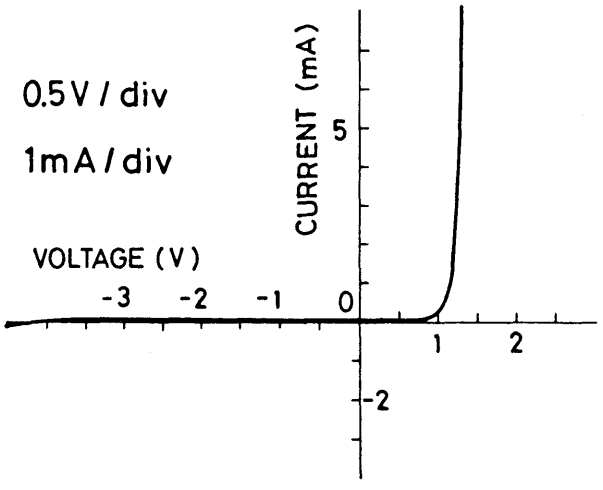

Fig. 4.3 Current/voltage relation of the LD.

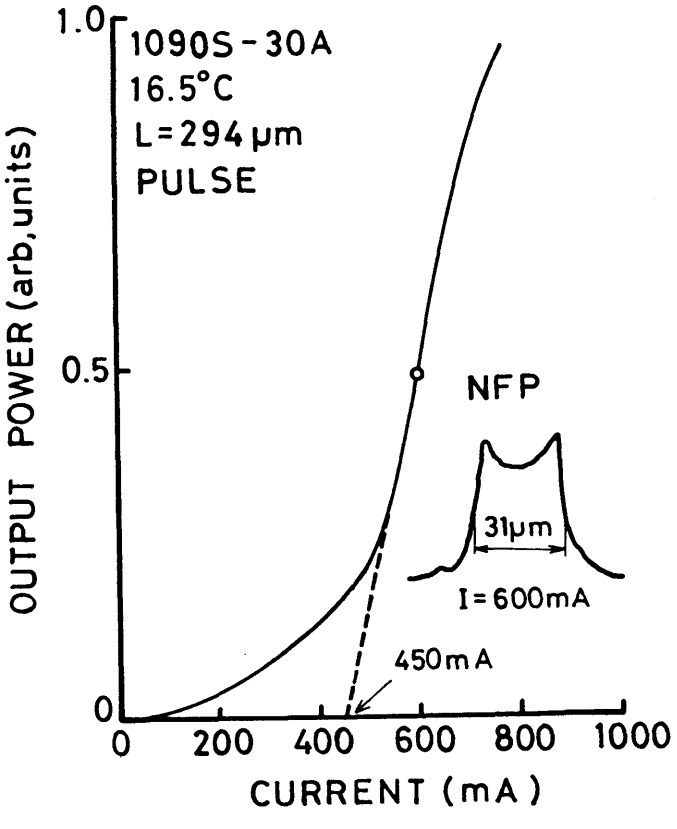

Fig. 4.4 Current/output power relation of the LD.

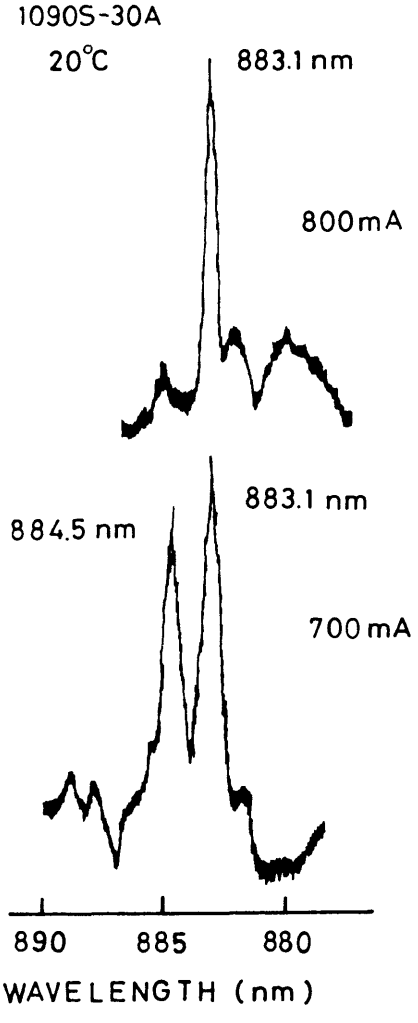

Fig. 4.5 Lasing spectra of the LD.

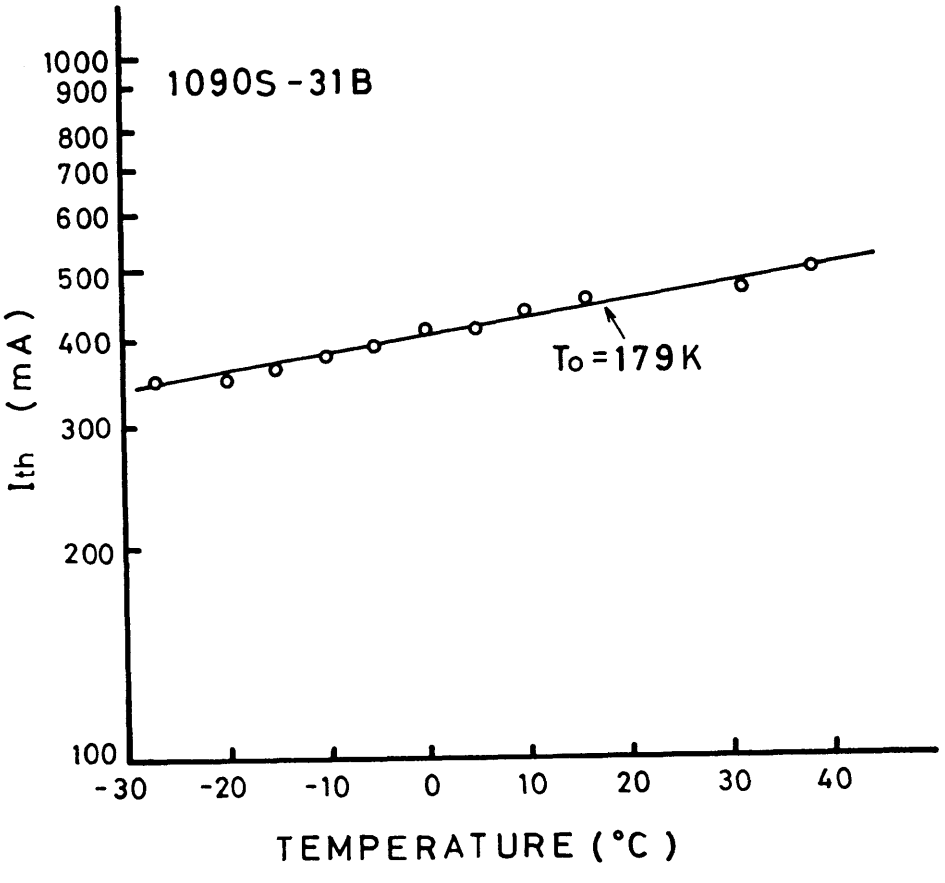

Fig. 4.6 Temperature dependence of the threshold current of the LD.

described above except that the substrate is n-GaAs (100 μm-thick, $n=2 \times 10^{18}$ cm^{-3}). There are no intermediate layers: the n-side electrode is formed on the back side of n-GaAs substrate, the emission width is 20 μm, and the chips are mounted with p-side down configuration on a Cu heat sink. The measuring conditions are also the same as described (room-temperature pulsed condition except the T_0 measurement). The typical threshold current density of 200 μm-long cavity devices is 0.8-1kA/cm^2, which is about 1/6 of the lowest value on the Si substrate. The lasing wavelength is in the range 870-877 nm, which is about 5-15 nm shorter than that on the Si substrate. The spontaneous peak emission wavelength on the Si substrate is also about 10 nm longer than that on the GaAs substrate. These shifts are caused by the stress applied to the layers due to the difference in the thermal expansion coefficient of Si and GaAs. The T_0 value is about 120-130 K in the temperature range of -60 to 50 ^oC, which is lower than that on the Si substrate.

4.3 Transverse junction stripe lasers

In the previous section, the lasing characteristics of double heterostructures fabricated on Si was described, presenting the fairly large threshold current. So the transverse junction stripe (TJS) laser is fabricated on Si to lower the threshold current.

The structure of the fabricated TJS LD is shown schematical-

ly in Fig.4.7. The intermediate layer structure and growth conditions are the same as previously. As there is a low resistive layer between Si and the intermediate layer as shown in Fig.2.11, undoped $Al_{0.4}Ga_{0.6}As$ is inserted between GaAs and the usual DH structure consisting of Se-doped n-$Al_{0.4}Ga_{0.4}$ ($n = 5 \times 10^{18} cm^{-3}$), undoped GaAs, Se-doped n-$Al_{0.4}Ga_{0.6}As$ ($n = 1 \times 10^{18} cm^{-3}$) and Se-doped n-GaAs ($n = 1 \times 10^{18} cm^{-3}$). The substrate used is p-type Si(100)2^{o} off toward [011]+15^{o}.

After the growth, 250nm SiO_2 film is sputtered and 300 μm wide stripe diffusion window is opened. The preferential Zn diffusion is performed at 650 ^{o}C for 40 min. using $ZnAs_2$ as a source. The diffusion depth is about 3 μm and the diffusion front passes through active layer and stops in n-type AlGaAs layer. The top GaAs layer of 10 μm wide at the edge of the diffusion region is etched to prevent leakage current through this layer. Au/Zn and Au/Sn ohmic contacts are formed by vacuum evaporation and photolithographic lift-off on p-GaAs and n-GaAs surfaces, respectively. The Si substrate is thinned down to about 50 μm. The cavity length is about 200 μm and the p-type Zn diffused region is cut to 100 μm wide to reduce the AlGaAs homo junction area and to decrease the leakage current through this junction.

Figure 4.8 shows the current to output power relation under pulsed operation at room temperature (27 ^{o}C). The pulsed width and the repetition rate are 100 ns and 1kHz, respectively. The lowest threshold current is 379mA. This relatively high

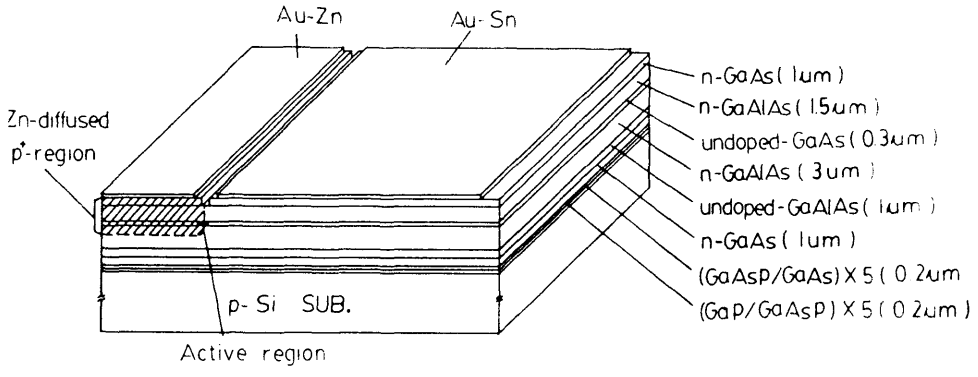

Fig. 4.7 Schematic illustration of the TJS LD on Si.

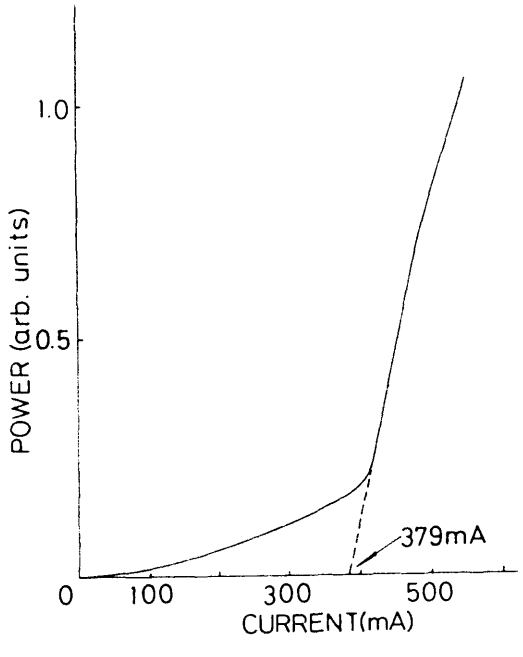

Fig. 4.8 Current/output power relation of the TJS LD.

threshold current is mainly due to the leakage through p-n junction in AlGaAs layer as the threshold current greatly depends on the area of this junction, thus , will be improved by growing high resistive layer between Si and n-AlGaAs cladding layer. However, this threshold is lower than that of the stripe lasers on Si except the GRIN-SCH structure lasers[3].

The lasing spectrum of the diode is shown in Fig. 4.9. The longitudinal mode is clearly resolved and there are also some other modes probably due to an inferiority in the mirror quality. The near field pattern spreads over 8-10 μm as the carrier is not laterally confined. The effective refractive index caluculated from longitudinal mode spacing is about 3.5 which is about smaller than that of the diodes on GaAs substrates.

4.4 Conclusion

Oxide stripe double heterostructure lasers and TJS lasers on Si which operate at room temperature under pulsed condition are demonstrated. The threshold current at 16.5 ^{o}C and the characteristic temperature of the oxide stripe laser grown on Si are 450 mA and 179 K, respectively. This threshold current is about 6 times larger than that grown on GaAs. The use of n-Si substrate will be useful as seen in the present structure where the current flows laterally in the thin n-GaAs layer, resulting in high series resistance. The lowest threshold current of the TJS laser is 379 mA at 27 ^{o}C. The threshold current will be much

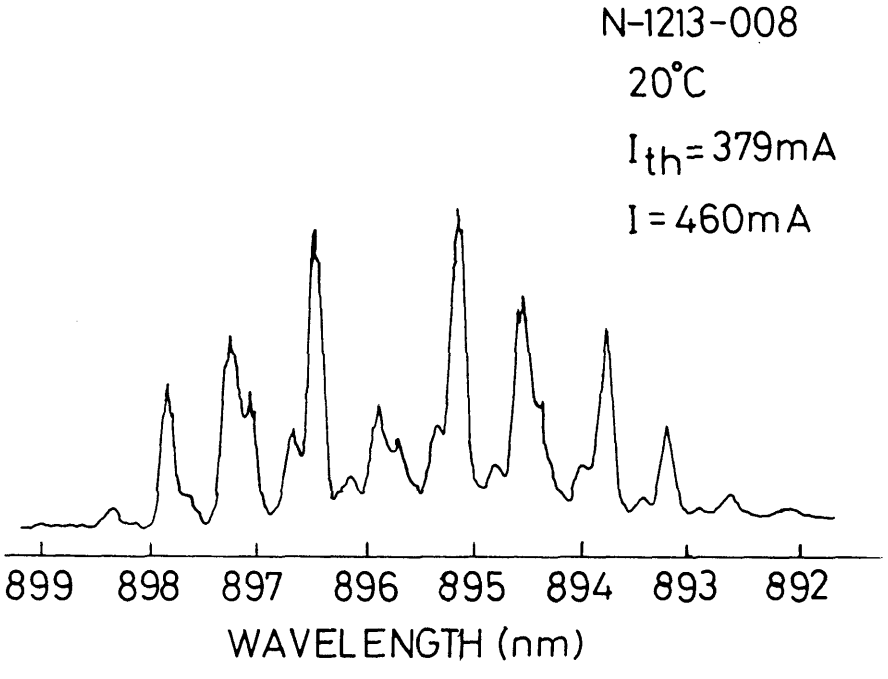

Fig. 4.9 Lasing spectrum of the TJS LD.

improved by optimizing the mirror formation, the device structure and the device fabrication procedure, i.e., the insertion of the high resistive layer between Si and n-AlGaAs and also by the two step diffusion.

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Chapter 5. MOCVD growth of $GaAs_{1-x}P_x$ (x=0-1) and $GaAs_{0.6}P_{0.4}$ LED's on Si substrates

5.1 Introduction

The heteroepitaxy of III-V compound semiconductor on Si is a promising technology which enables the monolithic integration of III-V compound-based devices with Si electronic circuits. Much efforts have been made on the heteroepitaxy of GaAs and GaP on Si, but no work has been reported on heteroepitaxy of $GaAs_{1-x}P_x$ with entire compositional range on Si except the growth of GaAsP on Ge substrates[1-3]. Among III-V compound semiconductors, GaAsP is a very important material for visible LED's (light emitting diodes) since its band gap energy covers the various color region such as red, yellow, orange and green. Moreover GaAsP can be used as solar cells[4,5] and lattice-matched substrates for InGaP and InGaAsP double heterostructure lasers[6]. These GaAsP substrates have to be grown on GaAs or GaP substrates by the vapor phase epitaxy using thick compositional graded buffer layers to relax the lattice-mismatch.

In chapter 2, It is shown that a single domain GaAs can be grown on Si using GaP and SLS's of GaP/GaAsP and GaAsP/GaAs as intermediate layers by MOCVD.

This chapter describes the MOCVD growth of $GaAs_{1-x}P_x$ with the entire compositional range of x= 0-1 on Si substrate using the same kind of intermediate layer to grow GaAs on Si[7-9].

Next, $GaAs_{0.6}P_{0.4}$ LED emitting at 655 nm is fabricated on Si substrate.

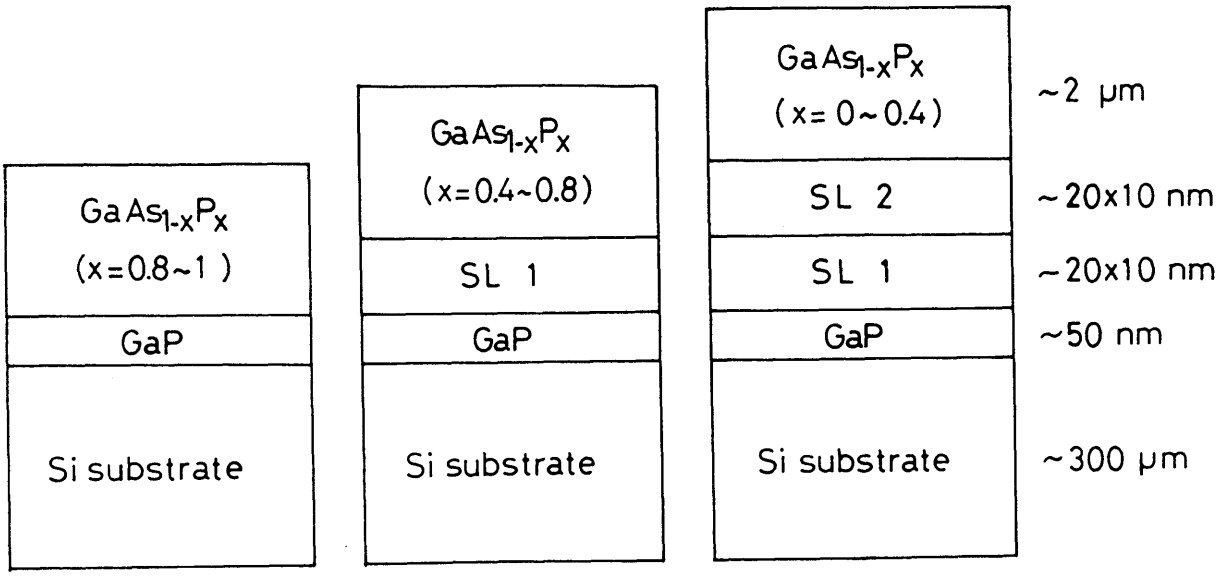
5.2 Growth conditions

The intermediate layer structure to grow $GaAs_{1-x}P_x$ on Si is almost the same as described in chapter 2. But three kinds of intermediate layers are used properly depending on the solid composition (Fig.5.1) because $GaAs_{1-x}P_x$ has compositional-dependent lattice constants from 0.5451 nm (x=1) to 0.5653 nm (x=0). For $0 < x < 0.4$, GaP, (GaP/GaAsP) SLS and (GaAsP/GaAs) SLS are inserted between GaAsP and Si, and for $0.4 < x < 0.75$ and $0.75 < x < 1$, GaP and (GaP/GaAsP) SLS and only GaP are used as intermediate layers, respectively.

The growth procedure and conditions are almost the same as described in chapter 2 to grow GaAs on Si. The growth temperature of GaP and SLS are 900 and 680 ^{o}C, respectively. Top GaAsP is grown on n-type Si with the orientation of (100)2^{o} off toward [011]+15^{o} at 650 or 730 ^{o}C, keeping V/III ratio constant at 44. The grown layer thickness is about 2 μm unless otherwise mentioned.

5.3 Growth of GaAsP on Si

The phosphorous solid composition x grown at 650 ^{o}C and 730 ^{o}C are plotted as a function of the gas phase composition,



SL 1 : $GaP / GaAs_{0.5}P_{0.5}$ superlattice

SL 2 : $GaAs_{0.5}P_{0.5}$ / GaAs superlattice

Fig. 5.1 Three kinds of intermediate layer structures to grow $GaAs_{1-x}P_x$ on Si.

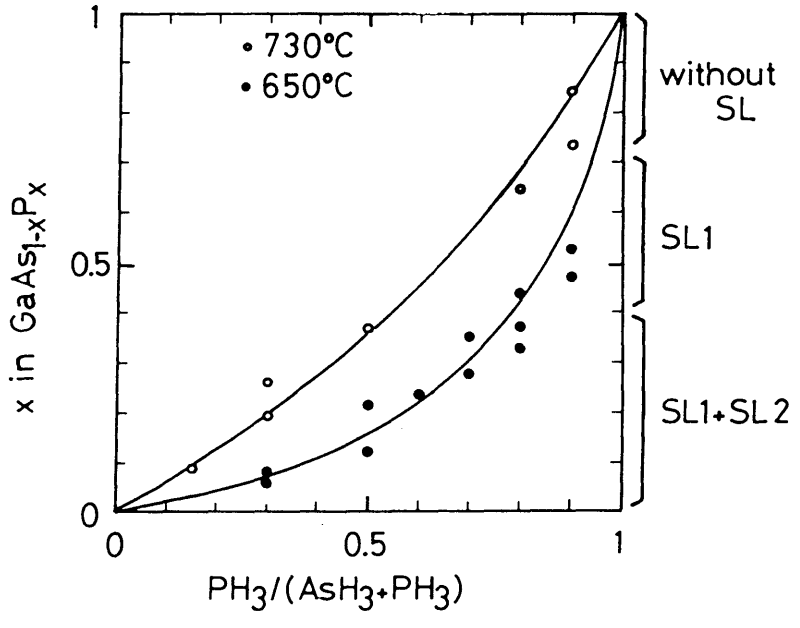


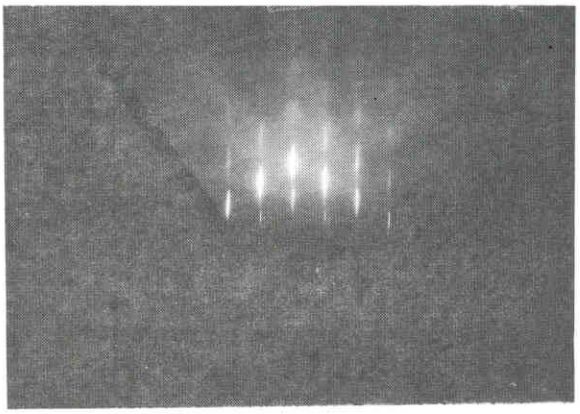
Fig. 5.2 $GaAs_{1-x}P_x$ solid composition as a function of gas phase composition $[PH_3]/[AsH_3+PH_3]$ at 650 and 730 °C.

$PH_3/(AsH_3+PH_3)$ in Fig.5.2. The solid compositions of the grown samples are determined by the lattice constants measured by the X-ray diffraction. Measured lattice constants of GaAs and GaP perpendicular to the surface grown on Si are 0.5646 nm and 0.5447 nm, respectively, which are slightly smaller than the unstrained lattice constants, as the difference in the thermal expansion coefficients of Si and GaAs or GaP produces the tensile stress in the grown layers. The solid compositions of GaAsP layers shown in Fig.5.2 are determined from their lattice constants perpendicular to the surface (refering to those of the strained GaAs and GaP layers assuming Vegard's law). The less P incorporation in the solid compared to As at lower temperature (650 ^{o}C) is explained by the relative easiness in AsH_3 cracking compared to PH_3 as many authors have reported[10].

Figure 5.3 shows the reflection electron diffraction patterns of $GaAs_{0.6}P_{0.4}$ grown at 650 and 730 ^{o}C. The spot patterns with Kikuchi line indicate the good crystallinity of the grown layers.

Figure 5.4 shows the Nomarski surface micro-photographs of the $GaAs_{1-x}P_x$ grown on Si substrates at 650 and 730 ^{o}C. The surface morphology becomes worse with increasing solid composition x in each growth temperature and the surfaces of the layers grown at 650 ^{o}C are better than those grown at 730 ^{o}C. A very smooth mirror-like surface is obtained in the sample grown at 650 ^{o}C in the range of x=0-0.4 and no crosshatch pattern such as seen on commercially available VPE-grown $GaAs_{0.6}P_{0.4}$ on GaAs sub-

(a)



(b)

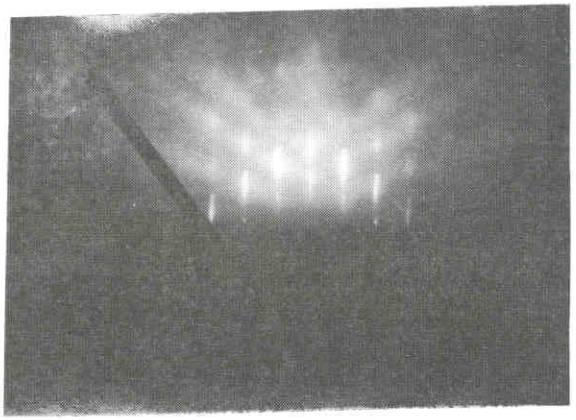


Fig. 5.3 RHEED patterns for $GaAs_{0.6}P_{0.4}/Si$ grown at (a) 650 and (b) 730 ^{o}C.

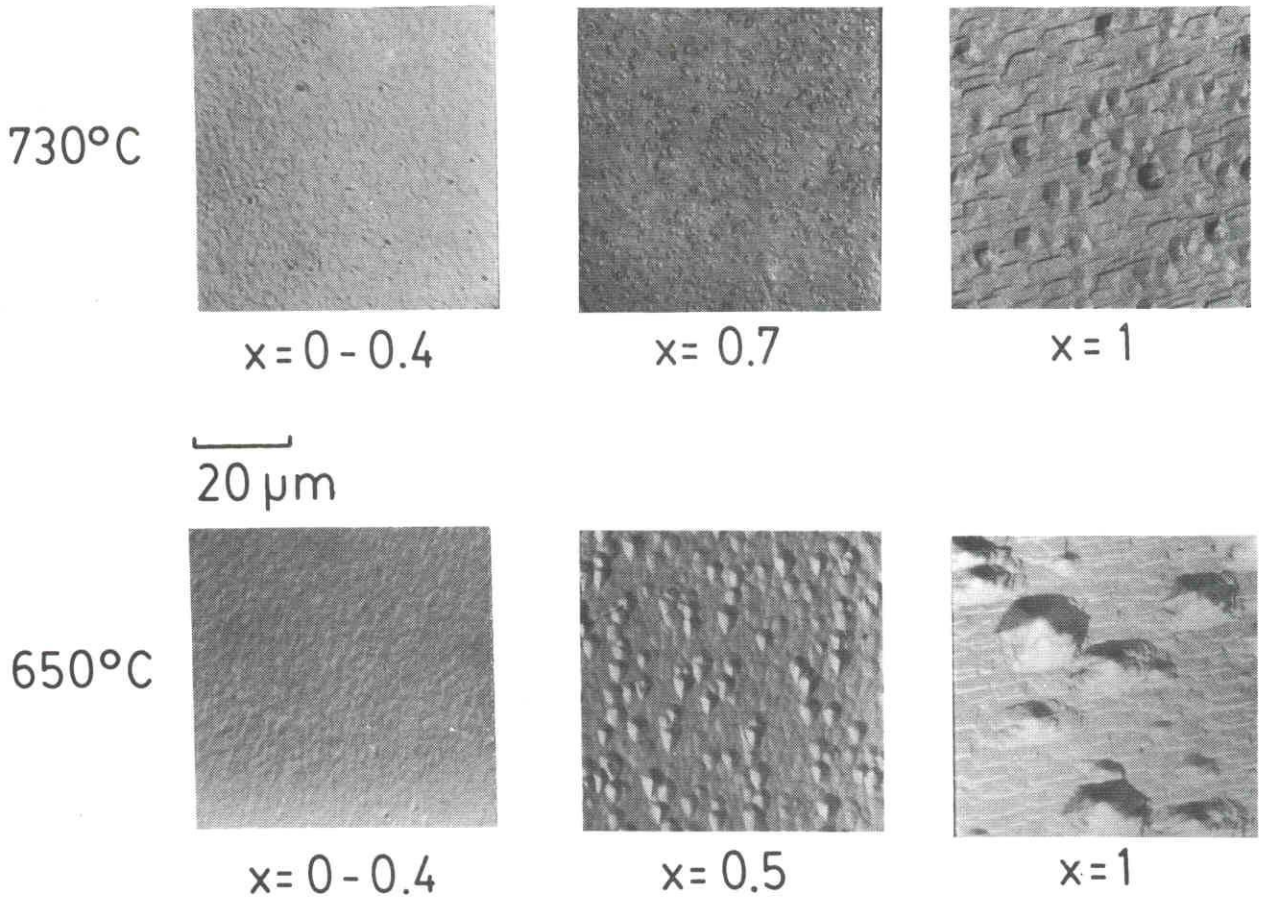


Fig. 5.4 Nomarski surface micro photographs of $GaAs_{1-x}P_x$ grown at 650 and 730 °C.

strate.

Figure 5.5 shows the room temperature PL spectra of $GaAs_{1-x}P_x$ (x=0.2-0.4) on Si grown at 650 and 730 ^{o}C. The PL intensities and half widths of the samples grown at 730 ^{o}C are one order of magnitude stronger and several meV broader than those of the samples grown at 650 ^{o}C, respectively. The PL intensity of $GaAs_{0.6}P_{0.4}$ on Si grown at 730 ^{o}C is about 40% of VPE-grown $GaAs_{0.6}P_{0.4}$ on GaAs and PL half width is a little broader than the 42meV of GaAsP/GaAs.

The PL spectra at 4.2K of $GaAs_{1-x}P_x$ (x=0-0.56) on Si grown at 650 ^{o}C are shown in Fig. 5.6. With increasing x from 0 to 0.21, two main peaks of 1.484eV (835.4 nm) and 1.461eV (848.6 nm) observed in GaAs/Si shift to larger energy side and become broader, and are not resolved at x=0.4. The PL spectrum at x=0.56 is slightly different from the others, probably due to the indirect band gap transition. The peak of 2.084eV (594.9 nm) is identified as the recombination of excitons bound to neutral donor and the peak of 2.055eV (603.3 nm) (29meV lower in energy) is an LA-phonon replica of 2.084eV (594.9 nm) peak[11].

5.4 $GaAs_{0.6}P_{0.4}$ LED's on Si

Since $GaAs_{1-x}P_x$ (x=0-0.4) can be successfully grown on Si, $GaAs_{0.6}P_{0.4}$ LED is then fabricated on a Si substrate. The structure is shown in Fig. 5.7. n-type layer is undoped and p-type layer is formed by Zn-doping using DEZ as a source. Figure 5.8

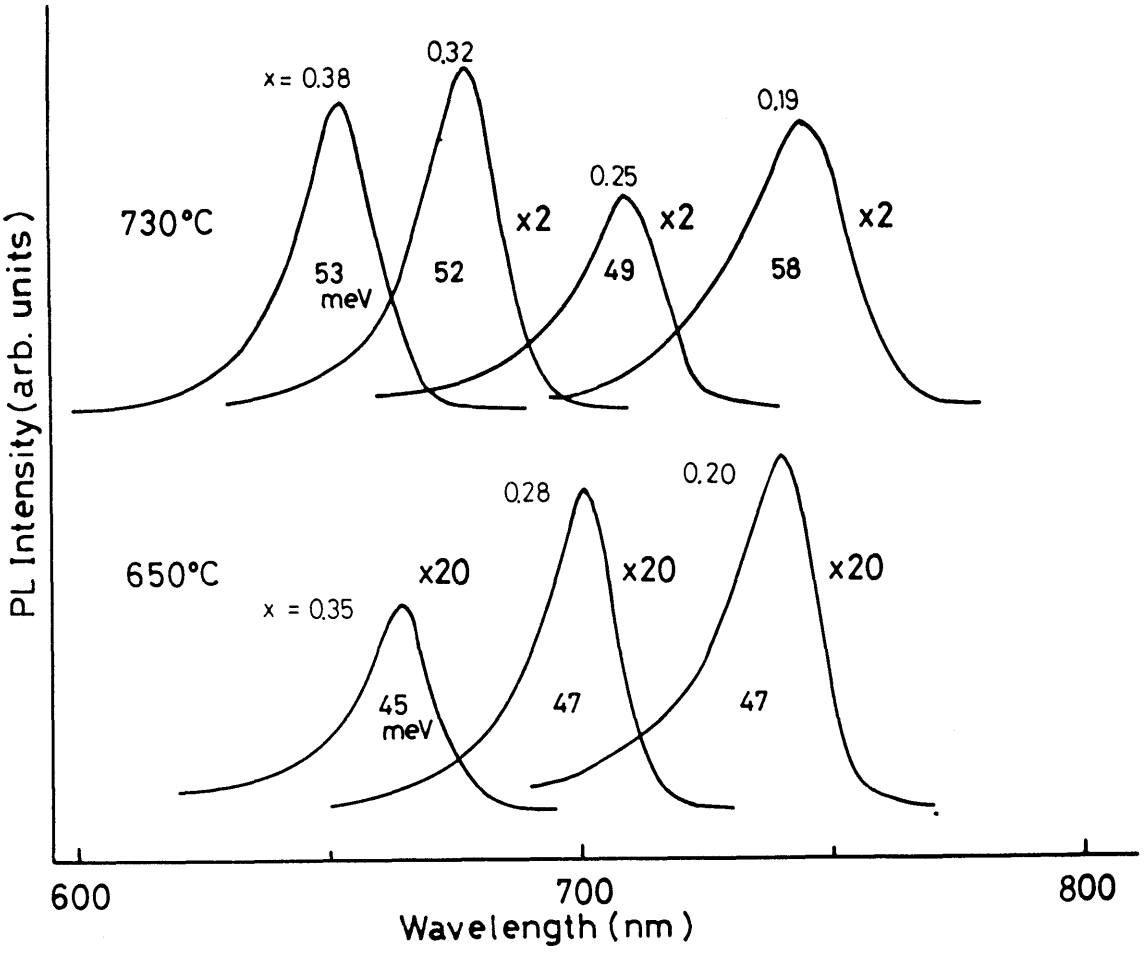


Fig. 5.5 Room temperature PL spectra and half width of $GaAs_{1-x}P_x$ (x=0.2-0.4)/Si grown at 650 and 730 ^{o}C.

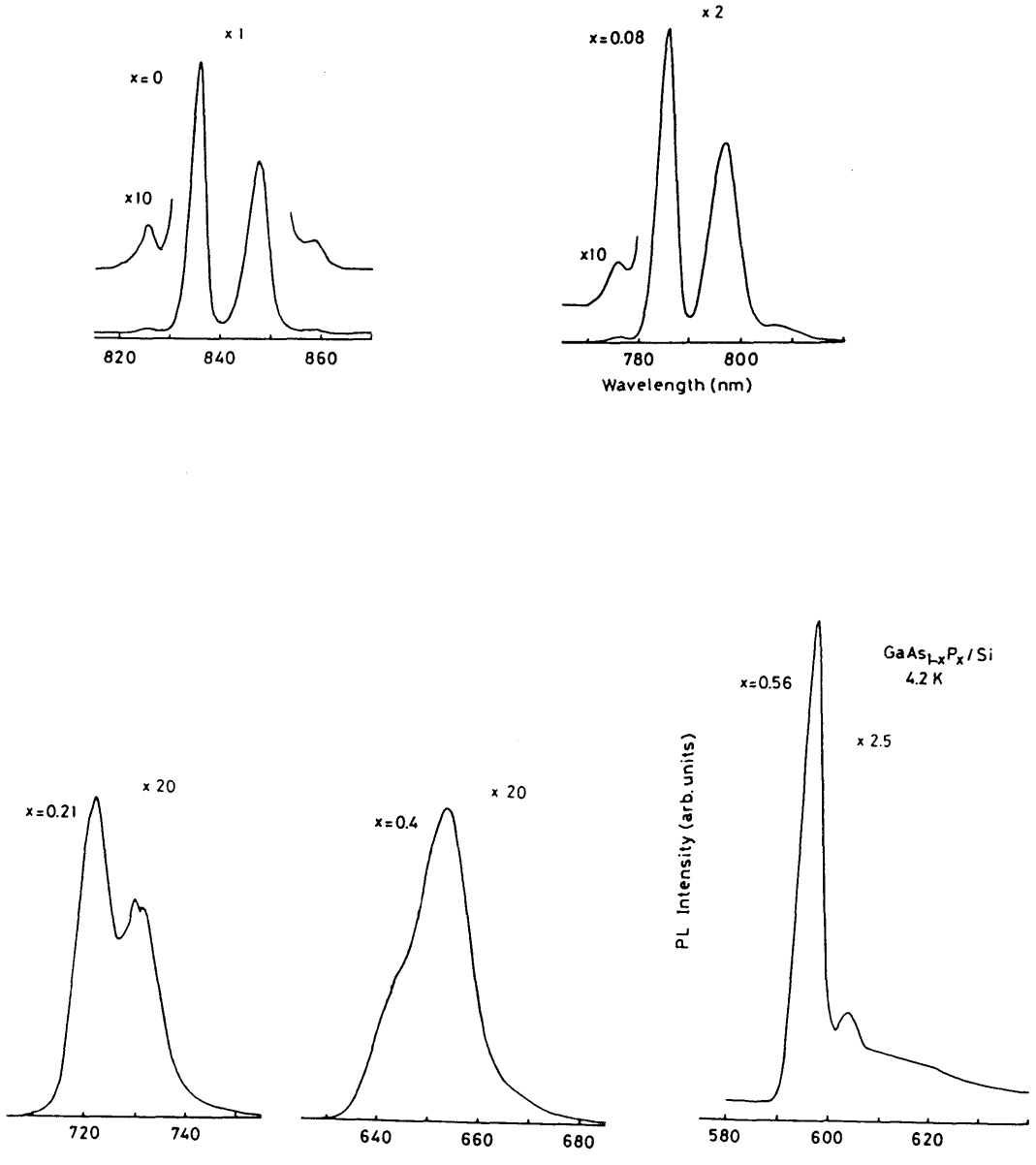


Fig. 5.6 4.2K PL spectra of $GaAs_{1-x}P_x$ (x=0-0.56)/Si grown at 650 ^{o}C.

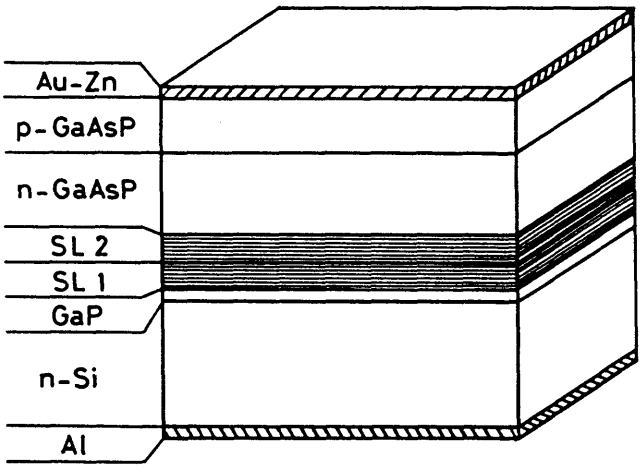


Fig. 5.7 Schematic illustration of the fabricated $GaAs_{0.6}P_{0.4}$ LED on Si.

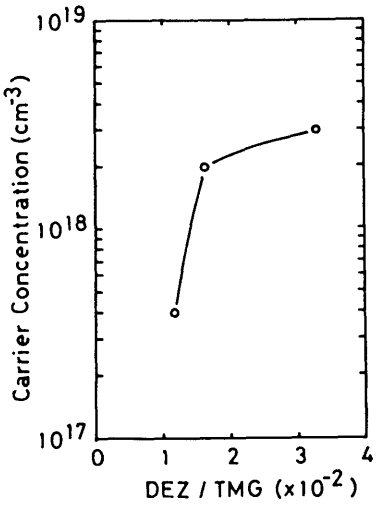


Fig. 5.8 Hole concentration of $GaAs_{0.6}P_{0.4}$ as a function of DEZ/TMG mole ratio.

shows the hole concentrations of $GaAs_{0.6}P_{0.4}$ grown on Si at 650 ^{o}C as a function of DEZ/TMG mole ratio. The hole concentration is measured by the C-V method. Figure 5.9 shows the in-depth profile of carrier concentration measured by the C-V method using an electrochemical cell. The 2 μm p-type layer ($p = 2 \times 10^{18}$ cm^{-3}) and the 3 μm undoped n-type layer ($n=1 \times 10^{17}$ cm^{-3}) are grown on an n-type Si substrate. The hole and electron concentrations increase at the p-n junction interface, but the reasons are not in question. The ohmic contacts on the back n-Si and the top p-$GaAs_{0.6}P_{0.4}$ are formed by evaporating Al and Au/Au:Zn, respectively and annealing.

The current versus light output power characteristic of the fabricated $GaAs_{0.6}P_{0.4}$ LED on Si is shown in Fig.5.10. Almost linear relation is obtained in the current range of 20mA to 120mA. The super linear increase in output power at the current below 20 mA suggests the existence of the leakage current. The output power of the diode is not measured exactly, but is still much lower compared with the commercially available GaAsP LED emitting at the same wavelength as the device structure is not optimized at all. However, the emission power will be much improved by optimizing the device structure, because the room temperature photoluminescence intensity of the undoped GaAsP layer on Si is in the same order as the commercial GaAsP wafer which is used to fabricate LED.

Figure 5.11 shows the emission spectrum through the p-side electrode of the LED. The emission peak wavelength and the half

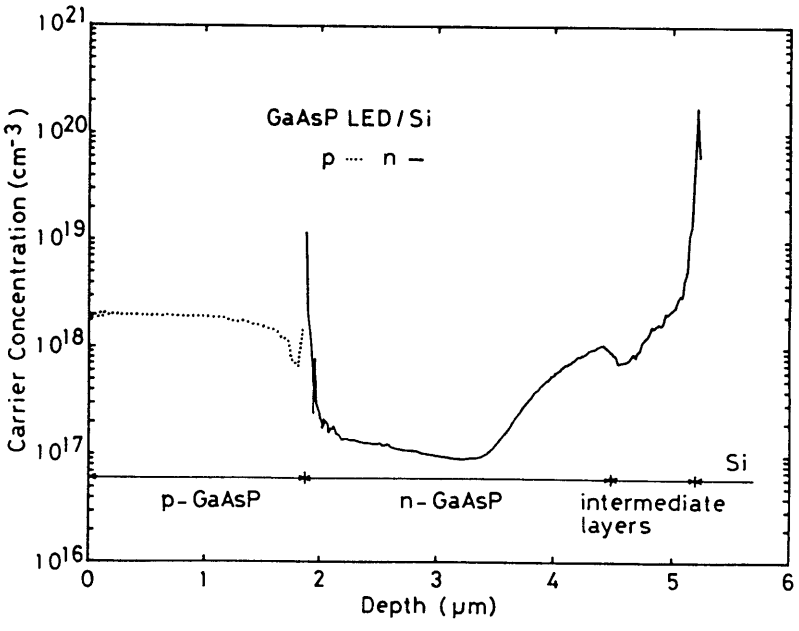


Fig. 5.9 In-depth carrier concentration profile of $GaAs_{0.6}P_{0.4}$ LED on Si.

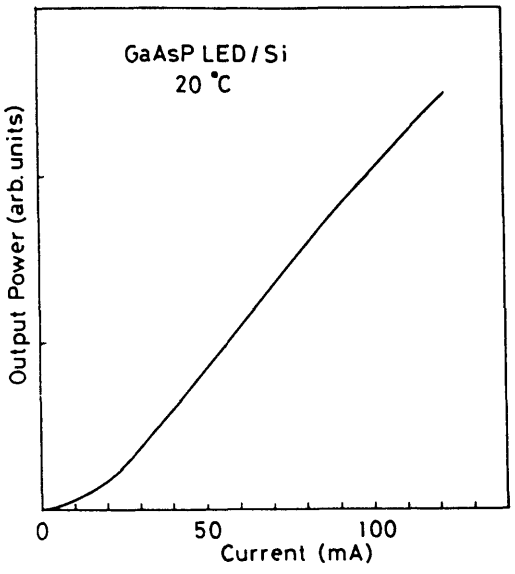


Fig. 5.10 Current/output power relation of the $GaAs_{0.6}P_{0.4}$ LED on Si.

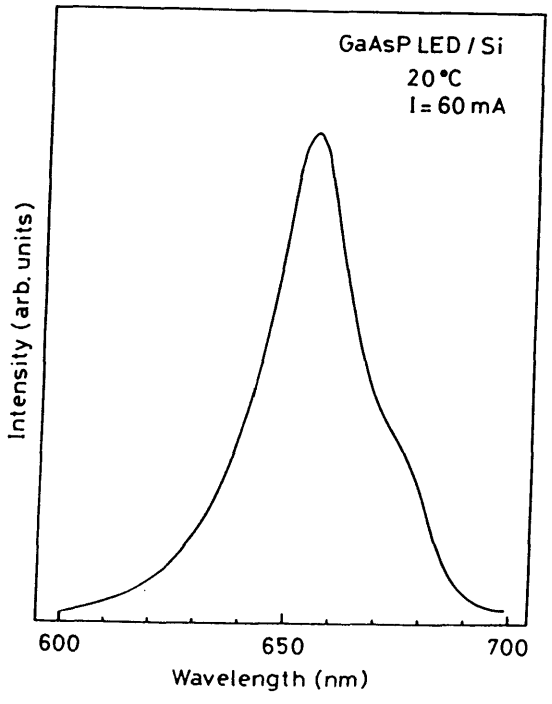


Fig. 5.11 Emission spectrum of $GaAs_{0.6}P_{0.4}$ LED.

width are 655nm and 24nm (68meV), respectively. The shoulder in the lower energy side can be attributed to the reflection at the intermediate layers and a selective absorption through the n-type region[12].

5.5 Conclusion

Single crystalline $GaAs_{1-x}P_x$ with entire compositional range of x = 0-1 are grown on (100)2° off Si substrats by MOCVD with three kinds of intermediate layers, GaP/(GaP/GaAsP) superlattice/(GaAsP/GaAs) superlattice for x=0-0.4, GaP/(GaP/GaAsP) superlattice for x=0.4-0.75 and only GaP for x=0.75-1, respectively. Very smooth mirror-like surfaces are obtained in the range of x=0-0.4, but the surface morphology becomes worse with increasing x, but the growth optimization of V/III ratio, growth rate and the growth temperature would produce a more superior surface even when x increases. The room temperature PL half width of 45-58meV is obtained in the range x = 0.2-0.4, and 4.2K PL spectra of $GaAs_{1-x}P_x$ (x=0-0.56) on Si grown at 650 °C are measured. The PL intensity of $GaAs_{0.6}P_{0.4}$ grown on Si is about 40% of a $GaAs_{0.6}P_{0.4}$/GaAs commercial sample. No crosshatch pattern such as seen on $GaAs_{0.6}P_{0.4}$/GaAs is observed on the surface. The similar PL spectra as those of GaAs on Si are obtained for $GaAs_{1-x}P_x$ in the compositional range x=0-0.1, and the peak half width becomes wider with increasing x up to x=0.4. The shape of the spectrum drastically changes at x=0.56 as the band gap of the

grown layer becomes indirect. A $GaAs_{0.6}P_{0.4}$ LED has been successfully fabricated on a Si substrate, and light emission centered at 655nm has been observed. An optimization of the growth conditions of $GaAs_{1-x}P_x$ ($x>0.4$) will enable the fabrication of a visible LED which can emit shorter wavelengths such as orange, yellow and green as well as red.

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Chapter 6. Summary

The technique to grow GaAs on Si has made a remarkable progress after the device-quality GaAs was successfully grown on Si with a Ge buffer layer in 1982. After that, several methods to grow GaAs on Si, such as a two-step growth method or a directly growth method, have been proposed and some kinds of electronic devices have been fabricated. However, little work has been made on the studies on the crystal properties of GaAs and the optical devices grown on Si.

In this dissertation, GaAs was grown on Si substrate with strained layer superlattice intermediate layers and its material properties were made clear. Room temperature operation AlGaAs /GaAs double heterostructure lasers were fabricated on Si, demonstrating the superiority of the crystal quality. $GaAs_{1-x}P_x$ with the entire compositional range of x = 0-1 were grown on Si to indicate the usefulness of this method.

In chapter 1, the purpose of this study, the present status of various compound semiconductors on Si substrates were summarized. Scope of this dissertation was also given.

Important results obtained by the experiments are summarized as follows.

In chapter 2, single crystalline GaAs was grown on a Si substrate using the strained layer superlattice intermediate layers together with GaP or AlP. The condition of the interface between the III-V compound semiconductor and Si was found to be

very important to obtain a high quality GaAs with a single domain structure. The optimum intermediate layer structure is composed of GaP, GaP/$GaAs_{0.5}P_{0.5}$ SLS and $GaAs_{0.5}P_{0.5}$/GaAs SLS and the growth temperatures of these layers are 900, 680 and 680 ^{o}C, respectively. The layer number in one superlattice is 10 and the thickness of the respective layer is 20 nm. The room temperature PL intensity is comparable to that grown on GaAs. The annealing of susceptor in H_2, the annealing of the substrate in H_2 + PH_3 before the growth and the use of a (100)2^{o} off Si substrate are indispensable to obtain a single domain GaAs on Si reproductively.

In chapter 3, the condition to obtain a single domain structure was made more clear and GaAs grown on Si with the optimized intermediate layer was characterized by photoluminescence, electroreflectance, deep level transient spectroscopy etc. to evaluate the crystallinity. The band gap energy was found to shift to the lower energy side because of the tension due to the difference in the thermal expansion coefficients of GaAs and Si.

The experimental observations with decreasing the GaAs thickness are summarized as,

(1) The etch pit density drastically increases,

(2) The stress calculated from curvature radius decreases,

(3) The lattice constant comes near to the GaAs original value,

(4) The energy gap approaches the originals.

These results all suggest that the stress is relaxed by the dislocation when GaAs is thin and that the GaAs layer gradually

becomes perfect with increasing the thickness. The applied stress is about 9.2 x 10^8 dyn/cm^2 which is about one half of the caluculated thermal stress.

Two electron traps with the activation energies of 0.73 and 0.44eV are observed for GaAs grown on Si, but only the 0.73eV trap is detected for GaAs grown on GaAs. Both 0.44 and 0.73 eV trap concentrations decrease with increasing the GaAs thickness and that of 0.73eV becomes comparable to GaAs on GaAs. The 0.44eV trap is attributed to the Si-dislocation complex which have the distributed energy centered at around 0.44eV and changes their shapes with the sequence of the growth.

The diffusion length of electrons in p-GaAs is smaller than that grown on GaAs, while that of holes in n-GaAs is comparable, demonstrating that the performance of devices using the minority carrier is still inferior to that grown on GaAs.

In chapter 4, room temperature operation AlGaAs/GaAs laser diodes were fabricated on Si substrates using III-V compound intermediate layers grown entirely by MOCVD. The threshold current density at 16.5 ^oC and the characteristic temperature of the stripe laser are 4.9kA/cm^2 and 179K, respectively, under the pulsed condition at room temperature. This threshold current is about 6 times larger than that grown on GaAs, which would be due to the existence of nonradiative center in the active layer and the applied stress. The lasing wavelength is about 5-15 nm longer than that grown on GaAs due to the difference in the thermal expansion coefficient. The TJS laser which operate at

room temperature was also fabricated on Si. The threshold current of this laser is as low as 379mA.

In chaper 5, single crystalline $GaAs_{1-x}P_x$ with entire compositional range of x = 0 - 1 was grown on Si substrates by MOCVD with three kinds of intermediate layers such as GaP/ (GaP/GaAsP)SLS/(GaAsP/GaAs)SLS for x = 0 - 0.4, GaP/(GaP/GaAsP) SLS for x = 0.4 - 0.75 and only GaP for x = 0.75 - 1, respectively. Very smooth mirror-like surface is obtained for x = 0 - 0.4. The room temterature PL half width of 45-58meV is obtained in the range x = 0.2 - 0.4 and the PL intensity of $GaAs_{0.6}P_{0.4}$ grown on Si is about 40% of $GaAs_{0.6}P_{0.4}$/GaAs commercial sample. No crosshatch pattern is observed at the surface. $GaAs_{0.6}P_{0.4}$ LED emitting at 655nm has been successfully fabricated on Si substrates.

Scope for the future work

In this dissertation, the technique to grow GaAs and GaAsP on Si substrates with strained layer superlattice intermediate layers was described and AlGaAs/GaAs lasers and $GaAs_{0.6}P_{0.4}$ LED's were fabricated on Si.

The attempt to grow GaAs on Si substrate was first made by using Ge intermediate layer. Recently, GaAs is usually grown on Si only by MOCVD or MBE without using additional technique to form Ge on Si. Although some kinds of devices have been fabricated on Si, these device performances are still inferior to

those grown on GaAs. If the material propereties of GaAs grown on Si become clarified, the suitable device structure on Si substrates becomes clear. In view of this, the result described in chapter 3 is very significant. But the details of the reasons such as why the etch pit density in GaAs on Si is reduced with the sequence of the growth and a high quality GaAs can be grown on Si in spite of the existence on the large lattice mismatch are still in question. The clarification of such a fundamental problem would be necessary in the future to obtain a more superior crystal on Si.

It is desired to establish the technique to grow every compound semiconductor such as InP and InAs on Si substrate to integrate Si devices and III-V compound-base devices. The growth using strained layer superlattice intermediate layers is one of the promising technique for this purpose. This technology will enable the new material combination using Si as a common substrate.

Even if the technique to grow III-V compound semiconductors on Si is established, the problems concerning with the stress due to the difference in the thermal expansion coefficient will remain. This affects the life time of the device and/or the device fabrication process. The technique of the selective epitaxy on Si substrates, suppressing the wafer curvature and the development of the intermediate layer to relax not only the lattice mismatch but also the difference in the thermal expansion coefficient perfectly will be very important in the future.

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2. MOCVD Growth of GaAs and AlGaAs for Solar Cell Application	Tech. Dig. of Int. PVSEC-1, pp. 357-360, 1984.	S. Sakai M. Takeyasu M. Umeno
3. Characterization of Epitaxially Grown GaAs on Si with III-V Compounds Intermediate layers by Metalorganic Chemical Vapor Deposition	J. Appl. Phys. Vol. 57, No. 10, pp. 4578-4582, 1985.	S. Hattori S. Sakai M. Takeyasu M. Umeno
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Title	Journal	Coauthor
6. Room Temperature Operation of AlGaAs/GaAs DH Lasers on Si Grown Entirely by MOCVD	Inst. Phys. Conf. Ser., No. 79, pp. 751-752, 1986.	S. Sakai M. Takeyasu M. Umeno
7. Room Temperature Operation of AlGaAs/GaAs Double Heterostructures fabricated on Si Substrates by Metalorganic Chemical Vapor Deposition	Appl. Phys. Lett. Vol. 48, No. 6, pp. 413-414, 1986.	S. Sakai M. Takeyasu M. Umeno
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Title	Journal	Coauthor
11. Epitaxial Growth and Material Properties of GaAs on Si Grown by MOCVD	J. Cryst. Growth Vol. 77, No. 1, pp. 498-502, 1986.	S. Hattori S. Sakai M. Umeno
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13. Deep levels in GaAs Grown Using Superlattice Intermediate Layers on Si Substrates by MOCVD	Jpn. J. Appl. Phys. Vol. 25, No. 10, pp. 1510-1513, 1986.	S. Sakai M. Umeno S. Hattori
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15. GaAlAs/GaAs TJS Lasers on Si Substrate Operating at Room Temperature Fabricated by MOCVD	Jpn. J. Appl. Phys. Vol. 25, No.12, pp. 1957-1958, 1986.	S. Sakai X. W. Hu M. Umeno

Title	Journal	Coauthor
16. MOCVD Growth of III-V Compounds on Si Using Strained Super Lattices	Proc. of MRS 1986 Spring Meeting vol. 67 pp. 15-27.	S. Sakai M. Takeyasu M. Umeno
17. MOCVD Growth of GaAsP on Si(100) Substrate with GaP and Strained-Layer Superlattice	Proc. of MS-MRS 1986 Meeting to be published.	M. Umeno S. Sakai M. Takeyasu
18. Crystal Growth of GaAs on Si Substrate and its Application to Optical Devices	J. IECE Vol. 70, 1987, to be published.	M. Umeno

Other papers

Title	Journal	Coauthor
19. Solid Composition and Growth Rate of $Ga_{1-x}Al_xAs$ Grown Epitaxially by MOCVD	Jpn. J. Appl. Phys. Vol. 22, No. 9, pp. 1357-1360, 1983.	Y. Takahashi S. Sakai M. Umeno S. Hattori

Title	Journal	Coauthor
20. Mechanism of MOCVD Growth for GaAs and AlAs	Jpn. J. Appl. Phys. Vol. 23, No. 6, pp. 709-713, 1984.	Y. Takahashi S. Sakai M. Umeno S. Hattori
21. High Temperature Gowth Rate in MOCVD Growth of AlGaAs	J. Cryst. Growth Vol. 68, No. 1, pp. 169-175, 1984.	Y. Takahashi S. Sakai M. Umeno
22. Selective MOCVD Growth of GaAs on Si Substrates with Superlattice Intermediate Layers	Jpn. J. Appl. Phys. Vol. 26, No. 2, 1987, to be published.	S. Sakai M. Umeno S. Hattori
23. Stress of GaAs on Si Grown by MOCVD Using Strained Superlattice Intermediate Layers and Two-Step Growth Method	Jpn. J. Appl.Phys. in process.	T. Imori M. Umeno S. Hattori

International conference

Title	Conference	Coauthor
1. High Temperature Growth Rate in MOCVD Growth of AlGaAs	2nd. Int. Conf. on Metalorganic Vapor Phase Epitaxy, 1984, Sheffield, England.	S. Sakai Y. Takahashi M. Umeno
2. MOCVD Growth of GaAs and AlGaAs for Solar Cell Application	1st. Int. Photo-voltaic Sci. and Eng. Conf., 1984, Kobe, Japan.	S. Sakai M. Takeyasu M. Umeno
3. GaAs/GaAlAs Light Emitting Devices on Si Substrate by MOCVD	2nd. Biennial OMVPE Workshop, 1985, Ithaca, USA.	S. Sakai M. Takeyasu M. Umeno
4. Heteroepitaxial Growth of III-V Compounds on Si by MOCVD	12th. Int. Symp. on GaAs and Related Compounds, 1985, Karuizawa, Japan.	S. Sakai M. Takeyasu M. Umeno S. Hattori
5. Room temperature Operation of AlGaAs/GaAs DH Lasers on Si Grown Entirely by MOCVD	12th. Int. Symp. on GaAs and Related Compounds, 1985, Karuizawa, Japan.	S. Sakai M. Takeyasu M. Umeno

Title	Conference	Coauthor
6. Epitaxial Growth and Material Properties of GaAs and GaAsP on Si Grown by MOCVD	3rd. Int. Conf. on Metalorganic Vapor Phase Epitaxy, 1986, Universal City, USA.	S. Sakai M. Takeyasu M. Umeno S. Hattori
7. GaAs/AlGaAs DH Lasers Fabricated on Si Subsatates by MOCVD	3rd. Int. Conf. on Metalorganic Vapor Phase Epitaxy, 1986, Universal City, USA.	S. Sakai M. Takeyasu X. W. Hu M. Imaizumi M. Umeno
8. MOCVD Growth of III-V Compounds on Si Using Strained Super Lattices (Invited)	MRS Spring Meeting 1986, Palo Alto, USA.	S. Sakai M. Takeyasu M. Umeno
9. MOCVD Growth of GaAsP on Si(100) Substrate with GaP and Strained-Layer Superlattice	MS-MRS Northeast Regional Meeting, 1986, New Jersey, USA.	M. Umeno S. Sakai M. Takeyasu
10. MOCVD Growth of GaAs on Si for Light Weight High Efficiency Solar Cells	2nd. Int. Photo-voltaic Sci. and Eng. Conf., 1986, Peking, China.	S. Sakai M. Takeyasu M. Umeno

Title	Conference	Coauthor
11. AlGaAs/GaAs Stripe Laser Diodes Fabricated on Si Substrates by MOCVD	10th. IEEE Int. Semicond. Laser Conf. 1986, Kanazawa, Japan.	S. Sakai X. W. Hu M. Umeno