Wet Etched Complex Three Dimensional MEMS Structures

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Abstract:

The present research reports the fabrication techniques for the formation of complex three dimensional structures. The process is developed using very economic wet anisotropic etching in pure and surfactant Triton X-100 [$C_{14}H_{22}O(C_2H_4O)_n$, n= 9-10] added 25 wt% tetramethyl ammonium hydroxide (TMAH) solutions. The structures are fabricated in single and nitride-based silicon on insulator (SOI) Si{100} wafers. In single wafer, both fixed and suspended structures are manufactured, while in SOI wafers only freestanding structures are realized. The present research is aimed to enhance the range of 3D structures fabricated using wet etching.

1. INTRODUCTION

In bulk micromachining using wet anisotropic etchants, the crystallographic properties restrict the size and shape of the silicon microstructures. Tetramethyl ammonium hydroxide (TMAH) is a preferred choice in wet etchants when oxide is used as etch mask and/or complementary metal oxide semiconductor (CMOS) process issues are considered. In the last decade, different kinds of ionic and non-ionic surfactants are studied in TMAH to widen the applications of wet etching in microelectromechanical systems (MEMS) [1-6]. The etch rate of Si{110} is strongly reduced when the surfactant is incorporated in TMAH, while the Si{100} etch rate is almost unaffected. The results for Si{110} can directly be correlated to other orientations, such as {441}, {331} or {221}, as their etch rates are also reduced significantly in other etchants containing TMAH and other surfactants [6]. Consequently the undercutting at convex corners, curved edges and the straight edges not aligned with <110> directions reduces considerably in surfactant added TMAH. In our previous study, the effect of 0.1% v/v non-ionic surfactant in different concentrations of TMAH is performed [2]. In this study, 25 wt% TMAH has found an optimal choice for achieving suppressed (in TMAH+surfactant) and enhanced (in pure TMAH) undercutting. Interestingly, the addition of surfactant in 25 wt% TMAH does not affect the etch rate of {100}Si which is most widely used in silicon bulk micromachining for the formation of MEMS structures. Figure 1 shows the serpentine shape etched profile and etching results in pure and surfactant Triton X-100 [$C_{14}H_{22}O(C_2H_4O)_n$, n = 9-10] added TMAH solution. Difference in the etching characteristics can be clearly noticed. The undercutting at all along the serpentine mask edge is noticeably suppressed. At the sidewalls of the serpentine channel, different index planes such as {110}, {441}, {331} or {221}, etc., are appeared. In other words we can say that the etch rates of these planes in surfactant added TMAH reduce to a significantly low level.

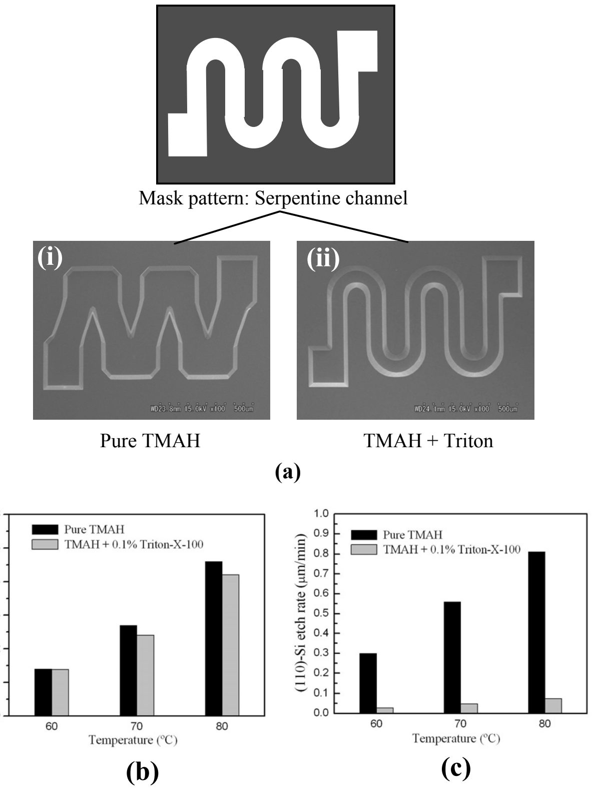

Fig. 1: Etching characteristics of pure and Triton X-100 added 25 wt% TMAH: (a) etched profiles of serpentine channel; (b) {100}Si etch rate; (c) {110}Si etch rate [17].

In order to extend the range of 3D structures in {100}Si, several techniques based on two-step etching [7-15], double side etching [16], wafer bonding [17], P^+-silicon as etch stop [18], and electrochemical etching [19] have been reported. Zubel *et. al* explored the possibilities to realize new shapes of etched profiles in silicon wafers with unconventional orientations such as {113}, {112}, {335}, {557}, {331}, etc [20].

In this paper, we have proposed and demonstrated the novel fabrication methods for the realization of complex 3D structures using two-step wet etching and local oxidation of silicon (LOCOS) processes. Wet etching is performed in pure and non-ionic Triton X-100 added 25 wt% TMAH solutions. The structures are fabricated in single and nitride-based silicon on insulator (SOI) wafers.

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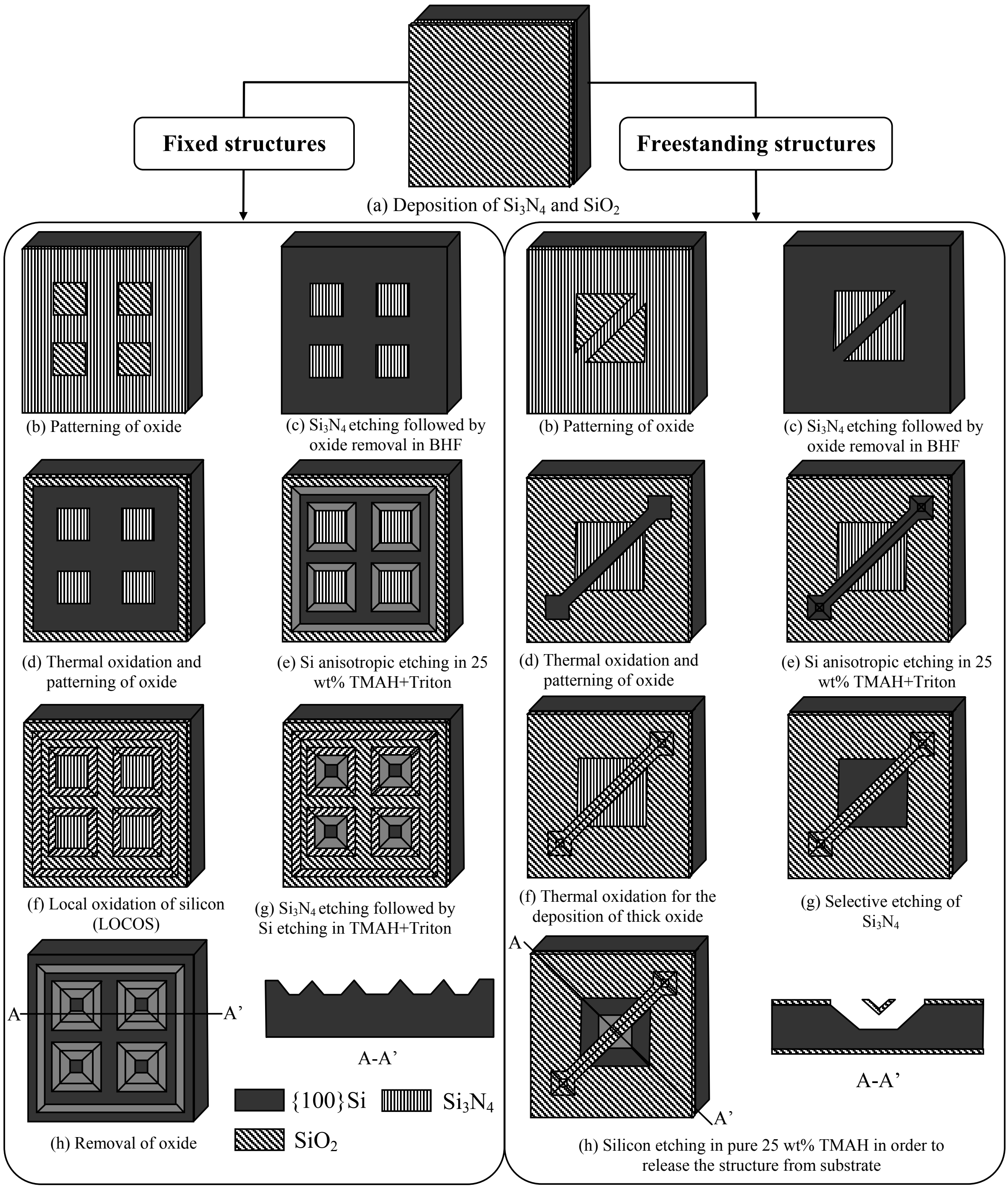


(a) Deposition of Si_3N_4 and SiO_2

(b) Patterning of oxide

(c) Si_3N_4 etching followed by oxide removal in BHF

(d) Thermal oxidation and patterning of oxide

(e) Si anisotropic etching in 25 wt% TMAH+Triton

(f) Local oxidation of silicon (LOCOS)

(g) Si_3N_4 etching followed by Si etching in TMAH+Triton

(h) Removal of oxide

(b) Patterning of oxide

(c) Si_3N_4 etching followed by oxide removal in BHF

(d) Thermal oxidation and patterning of oxide

(e) Si anisotropic etching in 25 wt% TMAH+Triton

(f) Thermal oxidation for the deposition of thick oxide

(g) Selective etching of Si_3N_4

(h) Silicon etching in pure 25 wt% TMAH in order to release the structure from substrate

Fig. 2: Fabrication steps for the realization of fixed and suspended structures in {100} single wafers

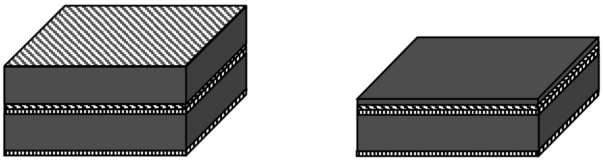
2. EXPERIMENTAL

To illustrate the proposed fabrication methods for the realization of complex three dimensional MEMS structures, {100} oriented CZ grown p-type of three inch diameter silicon wafers are used. 0.1% v/v Triton X-100 is used to prepare the surfactant added 25 wt% TMAH solution. Fabrication processes are developed for single and the nitride-based silicon on insulator (SOI) wafers. Firstly, silicon nitride of about 150 nm is deposited on thermally grown buffered oxide (50 nm) by low-pressure chemical vapor deposition (LPCVD). The wafers are divided into two batches in order to develop the process for single and SOI wafer. Process steps are described below:

Single wafer: The process steps for the fabrication of fixed and freestanding structures in single {100} wafers are shown in Fig. 2 in left and right columns, respectively. The nitride deposited wafers are patterned and the first step of anisotropic etching is carried out in TMAH+Triton. The LOCOS process is then carried out to grow an oxide layer on the exposed silicon. Now, the nitride is etched out globally. Thereafter, second etching is performed in TMAH+Triton (or pure TMAH) followed by global oxide etching in BHF. The selection of the etchant for both etching steps depend upon the requirement of undercutting. For the fabrication of structure shown in Fig. 2, the undercutting at sharp convex corner during the first etching step is undesirable. Therefore etching must be employed in TMAH+Triton. However second etching step can be carried out either in pure TMAH or TMAH+Triton as the etching encounter only sharp concave corners

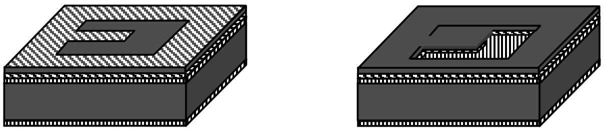
In order to fabricate the freestanding structures, a thick oxide layer (1-2 μm) is thermally grown after first anisotropic etching step. The etched profile formed during first etching works as mold for oxide layer (Fig. 2(d), right side column). The nitride layer is then removed in hot phosphoric acid. The second etching is then employed in pure 25 wt% TMAH solution as it provides high undercutting which is essentially needed for fast release of the structures.

SOI wafer: Nitride-based SOI wafers are prepared using bonded and etched back method [21]. Fabrication steps are illustrated in Fig. 3. First, the oxidized structural layer of SOI wafers are patterned and etched in TMAH+Triton in order to define the shapes of the structures. After this step, the wafers are thermally oxidized and the nitride layer is etched out selectively. Thereafter, second etching is carried out in pure TMAH to release the structures from the substrate. Final shape of released micro-cantilever is schematically shown in Fig. 3(g).



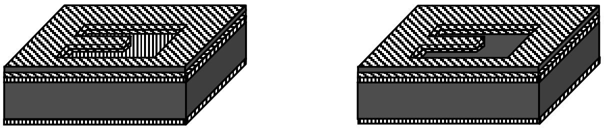
(a) Direct wafer bonding between silicon nitride (Si_3N_4) and oxide deposited wafers

(b) Thinning down of the top wafer for structural layer up to desired thickness



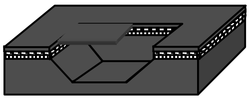
(c) Oxidation and patterning

(d) Silicon etching in 25 wt% TMAH+Triton in order to define the shapes of the structures followed by oxide etching



(e) Local oxidation of silicon (LOCOS)

(f) Silicon nitride etching while protecting the backside



(g) Silicon anisotropic etching in 25 wt% TMAH for releasing the structures followed by removal of nitride and oxide

▇ {100}Si

▨ SiO_2

▥ Si_3N_4

Fig. 3: Process steps for the fabrication of silicon cantilever beams using only single lithography step.

3. RESULTS AND DISCUSSION

SEM pictures of fabricated fixed and suspended structures in single Si{100} wafers are shown in Figs. 4 and 5, respectively. The fixed structures contain perfectly sharp edges and smooth etched surface finish. The structures shown in Fig. 4 are realized in Triton X-100 added 25 wt% TMAH solution, whereas the structure shown in Fig. 5 utilizes both pure and Triton X-100 added TMAH solutions. As mentioned before, the selection of pure and Triton added TMAH depends upon the requirement of undercutting. For instance, the structures shown in Figs. 4(b), 4(c), 4(d) and 4(e) require both anisotropic etching steps with a minimum undercutting; therefore etching must be performed in TMAH+Triton.

Figures 4(a)-(b) present the square and circular “ashtray” shapes structures, respectively. Due to roundness of the mask edges for both etching steps in the case of circular trays (Fig. 4(b)), etching should be performed only in

TMAH+Triton, whereas for the structure shown in Fig. 4(a) the second step etching can be performed either in pure TMAH or TMAH+Triton.

The concentric rectangular and circular corrugation patterns shown in Fig. 4(c) and 4(d), respectively, are promising structures for the formation of corrugated diaphragms on P^+-Si (and other materials) for the realization of MEMS based devices such as capacitive pressure sensors, microphones, etc. [22-24]. Figures 4(e)-(f) show adjacent V-grooves with perfectly sharp edges aligned along <100> and <110> directions, respectively. For <100> and <110> aligned grooves the sidewalls are formed by {110} and {111} planes, making an angle of 45º and 54.7º with the {100} wafer surface, respectively. Although both types of grooves are realized in TMAH+Triton solution, the grooves shown in Fig. 4(f) can also be manufactured in pure TMAH as the mask edges for both etching steps are aligned along the <110> direction.

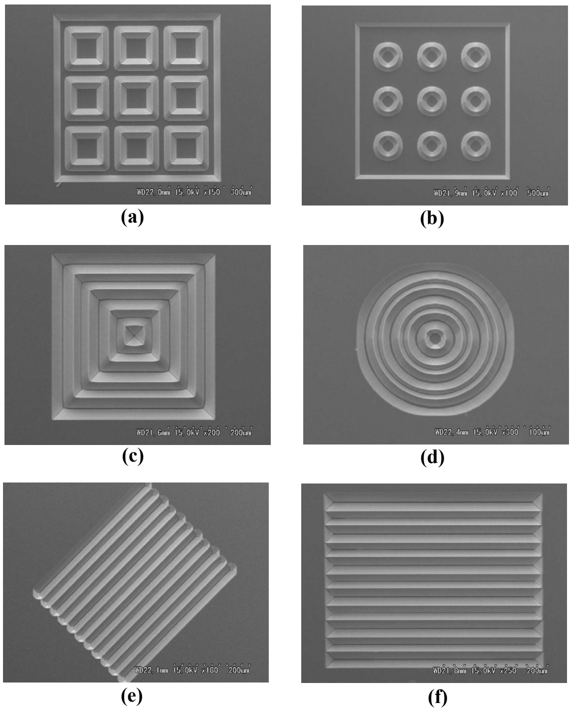


Fig. 4: SEM pictures of various fixed structures with perfectly sharp edges and corners: (a) square and (b) circular shapes ashtrays; (c) rectangular and (d) circular corrugations; adjacent grooves aligned along (e) <100> and (f) <110> directions.

The freestanding microfluidic channels with different shapes fabricated using the process steps illustrated in Fig. 2 (right side column) are shown in Fig. 5. The channel shown in figure 5(a) has been slightly twisted after release due to compressive stress of the thermally grown oxide. In the case of the meandering channel shown in Fig. 5(b) no bending is observed as the compressive stress is relieved after release from the substrate.

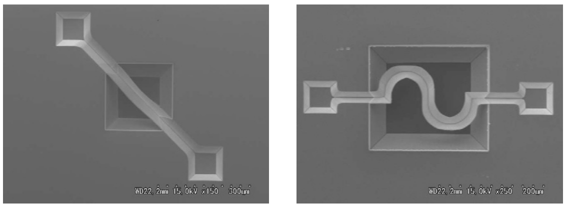


Fig. 5: Different shapes of overhanging SiO_2 microfluidic channels realized in {100}Si single wafer.

Different shapes of overhanging silicon structures realized in nitride-based SOI wafer using process steps illustrated in Fig. 3 are shown in Fig. 6. Cantilever beam shown in Fig. 6(a) contains sharp concave and convex corners, while shown in Fig. 6(b) contains rounded concave and sharp convex corners. In MEMS design rounded concave corners are very useful to minimize the stress concentrations at sharp corners. Two types of overhanging channels are shown in Fig. 6(c)-(d). In order to calculate the dimensions of mask patterns for desired shape structures, undercutting and crystallographic limitations of {100} silicon surface should be taken into consideration.

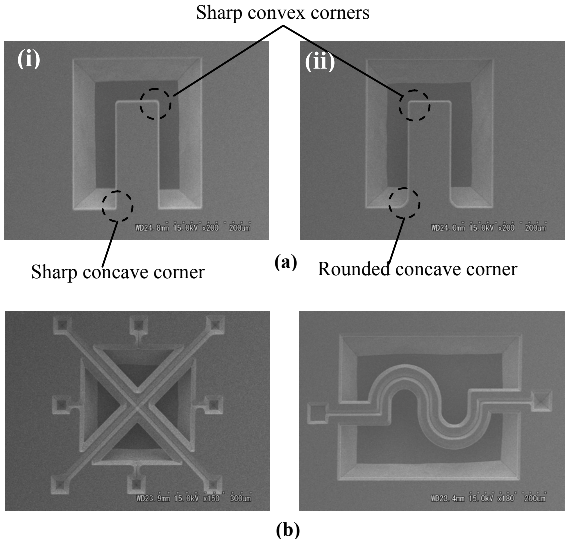


Fig. 6: Freestanding structures fabricated using process steps illustrated in Fig. 3: (a) Cantilever beams with (i) sharp concave and convex corners (ii) rounded concave and sharp convex corners; (b) Microfluidic channels.

Considering the various shapes shown in Figs 4-6, it can be claimed that the proposed fabrication methods provide the scope to extend the range of 3D structures fabricated by silicon anisotropic etching

4. CONCLUSIONS

New fabrication methods for the realization of different kinds of fixed and freestanding are proposed and demonstrated. Fixed structures are fabricated on single wafers, whereas freestanding are formed in both single and SOI wafers. The fixed structures contain perfectly sharp edges and corners, as well as smooth etched surface finish. The fabrication methods are developed using very economic wet anisotropic etching, and enable the formation of densely arrayed structures. The process steps are fully compatible to complementary metal oxide semiconductor (CMOS) process as both TMAH and a non-ionic surfactant are employed for wet etching. The present research has a wide scope, including, but not limited to, the fabrication of mold pattern for PDMS (or other materials), corrugated diaphragms, compact size liquid (or gas) delivery systems, overhanging microfluidic channels, etc. The present research expands the range of 3D structures fabricated by silicon anisotropic etching.

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