Influence of Interfacial Structure on Electrical Properties of Metal/Ge Schottky Contacts

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1. Introduction

A Ge channel metal-oxide-semiconductor field effect transistor (MOSFET) is an attractive alternative to a Si MOSFET for future ultra large integrated circuits because both electron and hole mobility in Ge are higher than Si [1]. It is necessary to establish metal/Ge contact technology for Ge MOSFET in order to realize high performance Ge devices. Schottky barrier heights (SBH) engineering at a metal/Ge interface is a key factor to realize a low contact resistance for Ge MOSFET. SBH for n-type contact, ϕ_{Bn} is generally formulated,

$$\phi_{Bn} = S(\phi_m - \chi_s) + const. \quad (1)$$

where ϕ_m is the work function of a metal, χ_s is the electron affinity of a semiconductor [2]. The index of interface behavior, S is

$$S = \partial\phi_{Bn} / \partial\phi_m . \quad (2)$$

It is known that the S value for metal/Ge contacts is very low (S~0.03) compared to Si contacts (S=0.27) and SBHs in various metal/n-type Ge contacts show values higher than 0.5 eV because of Fermi level pinning (FLP) at the metal/Ge interface [3,4]. Many reports discussed the origin of FLP such as interface states due to metal induced gap states (MIGS) or disorder induced gap states (DIGS). However, the detail has not been clarified yet. Some control technologies of SBH for metal/Ge contacts were also proposed; e.g. the introduction of an insulator interfacial layer such as Al_2O_3, Ge_2O_3 or Ge_3N_4 [5,6] and the segregation of sulfur at the NiGe/Ge interface [7]. However, the reduction mechanism in the SBH has not been understood well.

In this study, firstly, we investigated the influence of native oxide at the Ge surface on the metal/Ge contacts. Secondly, we investigated the effect of a Si intermediate layer between metal and Ge on the electrical properties.

2. Experimental

Substrates used were n-type Ge(001) wafers with a resistivity of 2.3-4.9 Ω-cm. A SiO_2 layer was deposited on a Ge wafer by spin-coating method and a contact hole whose area size of 1×1 mm^2 was patterned by using lithography. A substrate was chemically cleaned with diluted HF solutions and rinsed with deionized water. A wafer took into an ultra-high vacuum (UHV) chamber whose base pressure was below 2×10^{-8} Pa. After the chemical cleaning, the surface of the Ge substrate was covered with native oxide and surface oxide was removed by annealing at 550ºC for 20 min in UHV chamber. Formation of a Ge(001) 2×1 clean surface was confirmed by reflection high-energy electron diffraction. An Er, Zr, or Pt layer with a thickness of 30 nm was successively deposited by using electron-gun in the same UHV chamber. A 5-nm-thick Pt capping layer was also deposited on a Er/Ge sample to prevent the oxidation of the Er layer. Al layers were deposited on both front- and back-sides to form electrodes.

3. Results and Discussion

Influence of native oxide on contact properties

Figure 1 shows the current density-forward bias voltage (J-V) characteristics of the Er/Si sample with removing native oxide for various measurement temperature ranging from 100 K to 300 K. Typical thermionic emission current characteristic is observed especially near room temperature. The current-voltage characteristic is

$$J = J_s \exp\left(\frac{q(V - IR_s)}{nk_BT} - 1\right) \quad (3)$$

and the saturation current density J_s is

$$J_s = A^*T^2 \exp\left(-\frac{q\phi_{Bn}}{k_BT}\right) \quad (4)$$

where q is the elementary charge, n is the ideality factor, k_B is the Boltzmann constant, T is the temperature, I is the current and R_s is the substrate resistance, A^* is the effective Richardson constant, ϕ_{Bn} is the SBH [2].

SBHs for Er, Zr, and Pt/Ge contacts were estimated from J-V characteristics by using eqs. (3) and (4) and summarized in Table I. The Schottky barrier heights of Er

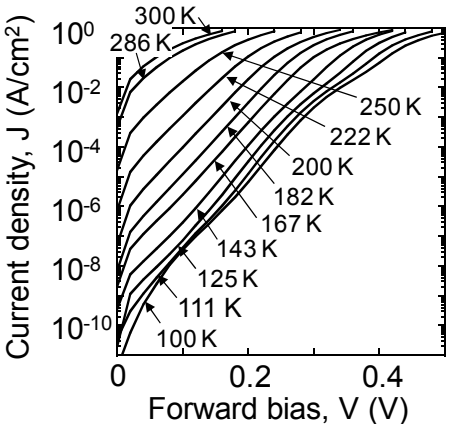

Fig. 1 The current density-forward bias voltage characteristics of the Er/Si sample with removing native oxide for various measurement temperature ranging from 100 K to 300 K.

Table I. Summary of Schottky barrier heights estimated from *J-V* characteristics for metal/Ge contacts.

Metal	Work function of metal (eV)	Schottky barrier height (eV)	
		w/o removing native oxide	with removing native oxide
Er	3.0	0.53 ± 0.01	0.52 ± 0.01
Zr	4.05	0.51 ± 0.05	0.52 ± 0.01
Pt	5.65	0.49 ± 0.12	NA

and Zr/Ge contacts were estimated to be about 0.5 eV and those were independent on the work functions of metals regardless of annealing for removing native oxide before the contact formation. This result indicates occurrence of the FLP at these contacts. Since the heats of formation of Er_2O_3 and ZrO_2 (-1904 and -1095 kJ/mol, respectively) were negatively larger than GeO_2 (-593.2 kJ/mol), the native oxide on Ge surface before the metal deposition is reduced with reaction of Er and Zr. Moreover, Er and Zr probably react with Ge and form a germanide at the interface even at room temperature. These results imply that the FLP is caused by the reaction and the formation of point defects such as Ge vacancy at the metal/Ge interface.

On the other hand, in the Pt/Ge sample without oxide-removing process, the variability of SBH is very large. Additionally, we could not estimate the SBH in Pt/Ge sample with the oxide-removing process due to the large current component other than the thermionic emission current. The less reactivity of Pt with Ge and Ge oxide than other metals might cause this characteristic property and further investigation needs to clarify the relationship between the FLP and the interfacial reaction.

Si interfacial layer into metal/Ge contacts

We also prepared the metal/Si/Ge contacts in order to investigate the influence of a Si interfacial layer on the electrical properties of metal/Ge contacts. Metal/Si contacts show less FLP phenomena than Ge and Si has an electron affinity of 4.05 eV being the same as that of Ge (4.0 eV). Therefore, we expected suppressing FLP by the introduction of a Si thin layer into the metal/n-Ge interface without increase in the contact resistance unlike the introduction of an insulator interfacial layer.

After removing native oxide on Ge surface, we prepared some interfacial Si layers on Ge substrates; a 10.5 nm-thick epitaxial Si (epi-Si) layer grown at 300ºC, a 25 nm-thick amorphous Si (a-Si) layer deposited at room temperature, and stacked structure of a 0.5 nm-thick epi-Si and a 10 nm-thick a-Si layers. After the deposition of a Si layer, an Er layer was deposited with aforementioned method.

Figure 2 shows the cross-sectional transmission electron microscope (TEM) image of the Er/a-Si/epi-Si/Ge sample. An Er silicide layer with a thickness of 7 nm is formed at the Er/a-Si interface and an uniform 5 nm-thick Si layer remains between Er silicide and Ge. The SBHs were estimated from the *J-V* characteristics for various Er/Si/Ge samples and they are summarized in Table II. Contrary to our expectation, the SBHs estimated in this study stay at the value higher than 0.5 eV regardless of the

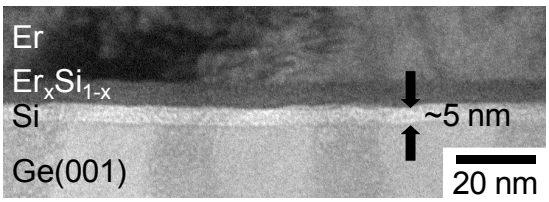

Fig. 2 The cross-sectional TEM image of the Er/a-Si(10 nm)/ epi-Si(0.5 nm)/Ge sample.

Table II. Summary of Schottky barrier heights estimated from *J-V* characteristics for various Er/Si/Ge contacts.

Contact structure	Schottky barrier height (eV)
Er/Ge [w/o Si]	0.52 ± 0.01
Er/epi-Si(10.5 nm)/Ge	0.61 ± 0.01
Er/a-Si(25 nm)/Ge	0.58 ± 0.03
Er/a-Si(10 nm)/epi-Si(0.5 nm)/Ge	0.50 ± 0.05

introduction of any Si layer, while reported values of SBH of Er_xSi_{1-x}/n-Si contacts are ranging between 0.28 and 0.4 eV [8]. This result means that the FLP cannot be resolved in Er/Si/Ge contacts. We deduce that the FLP occurs not at the Er silicide/Si interface but at the Si/Ge one, *i.e*. there are interface states causing the FLP are formed at the Si/Ge interface after the growth of Si on a Ge substrate.

4. Conclusions

We investigated the influence of the interfacial structure on electrical properties of metal/n-Ge Schottky contacts. The native oxide on Ge surface is not origin of FLP and the interfacial reaction between metal and Ge probably caused FLP. The introduction of Si inter layer was not effective to resolve the FLP of metal/Ge contacts. It is important to investigate the reaction and the crystalline structure at metal/Ge interfaces with atomic scale in detail to understand the FLP in the future.

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