Low-power High-speed Half-flux-quantum Circuits Driven by Low Bias Voltages

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Abstract

Half-flux-quantum (HFQ) circuits store and propagate half flux quanta. The basic circuit element is a 0-π SQUID, which is a superconducting quantum interference device with a conventional Josephson junction (0-junction) and a π-shifted ferromagnetic junction (π-junction). A 0-π SQUID achieves a small critical current in the absence of an external magnetic field, thus reducing power consumption. It is easy to set up 0-0-π SQUIDs with two 0-junctions and a π-junction which serves as a π phase-shifter. We simulated 0-0-π SQUID-based HFQ circuits driven by low bias voltages, referred to as LV-HFQ circuits. In these circuits, shunt resistors are not required for switching junctions because there is no hysteresis in the current-voltage characteristics of 0-0-π SQUIDs. We estimated the power consumption and maximum operating frequency of an HFQ Josephson transmission line (JTL) based on 0-0-π SQUIDs. When operating at 43.5 GHz, the power dissipation of a single element composed of a 0-0-π SQUID and a bias resistor fell to about 0.165 nW when biased at 60 μV. The LV-HFQ circuit is potentially more power-efficient than all other currently available superconducting logic circuits.

Keywords: 0-0-π SQUIDs, HFQ, RSFQ, power consumption, power efficiency

1. Introduction

Superconductor rapid single-flux-quantum (RSFQ) circuits [1] have attracted a great deal of attention over the past few decades because of their high-speed operation and low power consumption. Superconducting logic circuits are the most promising candidates to construct exascale supercomputers; conventional semiconductor technology would require several hundreds of megawatts to achieve the same performance [2]. A 4-bit bit-parallel microprocessor was successfully operated at 32 GHz; the power efficiency was high compared to that of semiconductor microprocessors [3]. The readouts of cryogenic sensor arrays require strict thermal budgets at low temperatures [4, 5]. Thus, low-power and/or high-speed superconducting logic circuits amenable to very large-scale integration (VLSI) are urgently required. The switching element like a Josephson junction with a periphery should have a power consumption below 1 nW and clock period of less than 100 ps.

However, most of the power is dissipated by the bias resistors used to distribute the bias currents to the switching elements in the RSFQ circuit. Typically, a bias resistor consumes over 10 nW, which is at least 10 times as much power as consumed by the junction. Several energy-efficient circuits have been developed to overcome the drawbacks of the RSFQ circuit [6]. Reciprocal quantum logic (RQL) [7], energy-efficient ERSFQ [8] and eSFQ [9] circuits aim to eliminate power dissipation by bias resistors. The basic power consumption of a Josephson junction is determined by $I_c\Phi_0 f$, where I_c is the critical current of the Josephson junction, Φ_0 is the single-flux-quantum, and f is the operating frequency. However, the power consumption remains at about 10 nW when operating at several tens of GHz. As the basic power

consumption of a Josephson junction reflects the phase jump during a switching event, use of an adiabatic quantum flux parametron (AQFP) [10] can lower the phase change speed and reduce the energy consumed during a single switch of a logic gate to the order k_BT [11], where k_B and T are the Boltzmann constant and operating temperature, respectively. In a low-voltage RSFQ (LV-RSFQ) circuit [12, 13], the bias current provided to the Josephson junction acts as a driving force, decreasing only during the switching event. The speed of the phase change is thus reduced to some extent and the basic power consumption is lowered. Note that in all energy-efficient circuits, there is a trade-off between power consumption and operating frequency.

The most direct way to reduce basic power consumption is to decrease I_c. The minimum I_c in an actual circuit is determined by the balance between the critical current density J_c and the size of the junction area, which in turn depends on the fabrication technology of the integrated circuits. Currently, the minimum I_c ranges from 50 to 100 μA when the J_c is 10 kA/cm^2.

Several institutes have reported that ferromagnetic Josephson junctions exhibit π phase-shifts in the current-phase relationship [14-20]. These junctions are referred to as π-junctions. A 0-π SQUID is a superconducting quantum interference device composed of a conventional Josephson junction (0-junction) and a π-junction [21]. A 0-π SQUID has a smaller critical current (hereafter, the nominal critical current, $I_{nominal}$) than the $2I_c$ in the absence of an external magnetic field [22].

Previously, we proposed a half-flux-quantum (HFQ) circuit that utilized $I_{nominal}$ to reduce basic power consumption and provide a phase jump of π, rather than 2π, during a switching event [23]. Experimentally, we showed that there is no hysteresis in the current-voltage characteristics of 0-0-π SQUIDs [24]. Thus, HFQ circuits can be operated over a wide bias voltage range without any need for shunt resistors parallel to the junctions. A further reduction in basic power consumption can be expected if the HFQ circuit is driven by low voltages. Here, we developed a novel low-voltage HFQ (LV-HFQ) superconducting logic circuit. The power consumption and operating frequency were calculated and compared to those of other superconducting logic circuits.

2. Half-flux Quantum Circuit

2.1. 0-π SQUID

In 2001, a controllable π SQUID (dc-SQUID) was proposed, in which the magnitude and sign of the critical current of the individual Josephson junctions can be tuned, however, an additiaonal voltage probes are required to change the electron energy distribution [25]. A superconducting loop interupted by π-junction (RF-SQUID) can result in half integer flux quantization, but can't act as a switching element for logical operation [26].

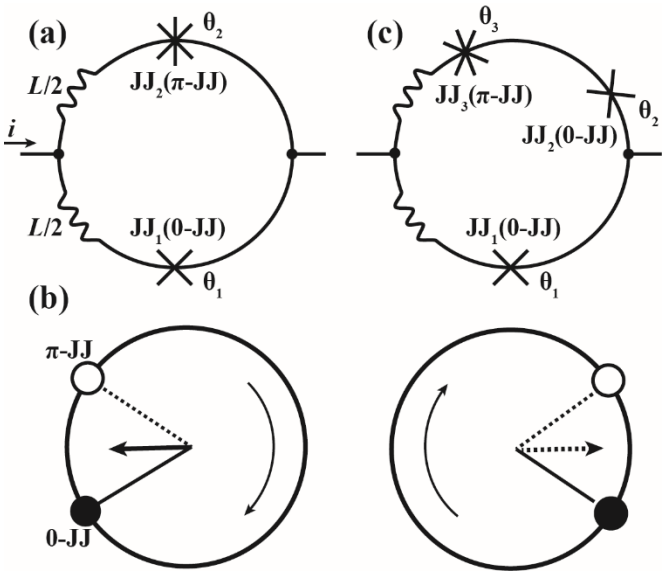

Figure 1. (a) Schematic of a 0-π SQUID. (b) A pendulum model of the bi-stable states of a 0-π SQUID. The white pendulums represent the π-junctions under upward gravity and the black pendulums represent the 0-junctions under downward gravity. The solid and dotted arrows indicate that the phase of the 0-π SQUID and total phase change between the bi-stable states is π. (c) Schematic of a 0-0-π SQUID.

Most logic gates in an HFQ circuit can be constructed by replacing the Josephson junctions of RSFQ gates with 0-π SQUIDs. Figure 1(a) shows a schematic of a 0-π SQUID. The 0-junction (JJ_1) and the π-junction (JJ_2) have the same critical current and plasma frequency. The π-junction serves as a switching and phase-shifting element. Given the π phase-shift in a 0-π SQUID, the 0-junction and π-junction cannot take their lowest energy states simultaneously; an intrinsic current circulates in the SQUID loop. When a pulse-shaped current i is provided to the SQUID, the two junctions switch alternately. The clockwise and anticlockwise circulating currents exhibit bi-stable states. Figure 1(b) shows the pendulum model of a 0-π SQUID. The black pendulums represent the state of a 0-junction under downward gravity and the white pendulums represent the state of a π-junction under upward gravity. The total phase change of the 0-π SQUID between the two stable states is π, as shown by the phase change between solid and dotted arrows.

2.2. Currently Available HFQ Circuits

Regarding actual HFQ circuits, the abovementioned requirements of both junctions pose a major challenge for the

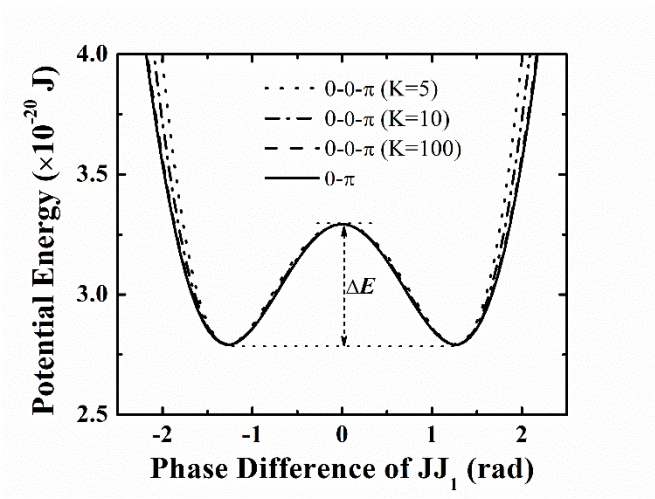

Figure 2. The potential energy of 0-π and 0-0-π SQUIDs as a function of the phase difference of JJ_1. *K* is the critical current ratio of the π-junctions to the 0-junctions of 0-0-π SQUIDs with the same LI_c products ($0.1\Phi_0$)

fabrication process. Usually, π-junctions exhibit low plasma frequencies that may restrict the switching speed of HFQ circuits and it's difficult to maintain the same critical currents between 0-junction and π-junction. An alternative is to use 0-0-π SQUIDs instead of 0-π SQUIDs; a 0-0-π SQUID is formed by placing two 0-junctions and a π-junction in a superconducting loop, as shown in figure 1(c). The 0-0-π SQUID was demonstrated by Feofanov and incorporated in the conventional SFQ circuit, in which the π-junction merely acts as a phase shifter [27]. Of the 0-0-π SQUIDs studied here, the two 0-junctions serve as the switching elements and the π-junction as the phase-shifting element. The critical current of both 0-junctions is I_c, whereas that of the π-junction is KI_c. The condition $K > 1$ is imposed to allow phase-shifting by the π-junction. Use of a non-tunneling ferromagnetic junction with a superconductor/ferromagnet/superconductor (SFS) structure allows a large *K* to be easily achieved. Experimentally, *K* ranged from 100 to 1000 [24]. Even if the π-junction has a relatively small McCumber-Stewart parameter ($\beta_c << 1$), the operating frequency of the HFQ circuit is not affected.

$$U = E_j[(1 - cos\theta_1) + (1 - cos\theta_2) + K(1 - cos\theta_3) + \frac{\theta_L^2\Phi_0}{4\pi LI_c}] \quad (1)$$

We numerically analyzed the potential energy *U* to confirm that 0-π SQUIDs and 0-0-π SQUIDs with different *K* values behaved identically. The calculation is based on Eq. (1), where θ_1, θ_2, and θ_3 are the phase differences of the junctions and the suffixes correspond to the numbers shown in figure 1(c). E_j is Josephson coupling energy (expressed as $I_c\Phi_0/2\pi$) and θ_L is the phase change of the loop inductance which can be caluclated with the quantization condition ($\theta_1 + \theta_2 + \theta_3 + \theta_L = 2n\pi$, n is an integer). The energy store in the loop inductance is $E = \left(\frac{\theta_L\Phi_0}{2\pi}\right)^2/2L = E_j\frac{\theta_L^2\Phi_0}{4\pi LI_c}$. We set I_c and the LI_c product to 50 μA and $0.1\Phi_0$, respectively, because these values are easy to attain. Figure 2 shows the potential energy as a function of the phase difference of the 0-junction JJ_1. The loop inductance *L* is tuned to ensure that the sum of *L* and the kinetic inductance of the π-junction is constant. The kinetic inductance $L_{kinetic}$ can be approximated as $L_{\text{kinetic}} = \frac{\Phi_0}{2\pi KI_c cos\theta_3}$ which can be ignored when $K \geq 100$.

Symmetric double potential wells (with respect to the vertical axis) can be seen in figure 2. Thus, the bi-stable states can be obtained in the absence of any external field or current. The height of the potential barrier ΔE and phase difference corresponding to the potential minimum are the same in the 0-π and 0-0-π SQUIDs. The most important parameter, $I_{nominal}$, is determined by the abovementioned phase difference, and is represented by the steepest slopes at the potential barrier located between the two minima. $I_{nominal}$ is independent of *K* when $K > 10$.

2.3. Nominal Critical Current

In a 0-0-π SQUID, $I_{nominal}$ is dependent on the SQUID loop inductance *L*, while the critical current of a conventional SQUID is given by the sum of the critical currents of the two junctions. We examined the *L* dependence of $I_{nominal}$ by numerical simulation of the dynamic behavior of 0-0-π SQUIDs [figure 1(c)]. An analog circuit simulator (PJSIM) was used [28]. All circuit and junction parameters are chosen to meet the Advanced Industrial Science and Technology (AIST) High-speed Standard Process (HSTP) [29]. We assumed that the critical current density of both the 0- and π-junctions was 10 kA/cm^2. The smallest junction area was 0.71 × 0.71 μm^2 and the lowest critical current was 50 μA. The junction had a normal resistance R_n of 32 Ω, a subgap resistance R_{sg} of 200 Ω, and a capacitance C of 32 fF. The typical characteristic voltage (V_c~$I_cR_{s\pi}$) of π-junction is much smaller than that of 0-junction, so we placed a shunt resistance $R_{s\pi}$ parallel to the π-junction to imitate an SFS junction with $I_cR_{s\pi}$ of 50 μV. Throughout the simulation, *K* was held at 100.

$I_{nominal}$ was independent of the initial conditions (clockwise or anticlockwise circulating current). Figure 3 shows the simulated value of $I_{nominal}$ as a function of LI_c/Φ_0. When $LI_c/\Phi_0 = 0.1$, $I_{nominal}$ was 15.7 μA, which is much smaller than the maximum critical current of 100 μA.

3. Low-voltage Half-Flux Quantum Circuit

3.1. Dynamic Behavior of the Voltage and Current

We used an HFQ Josephson transmission line (JTL) to

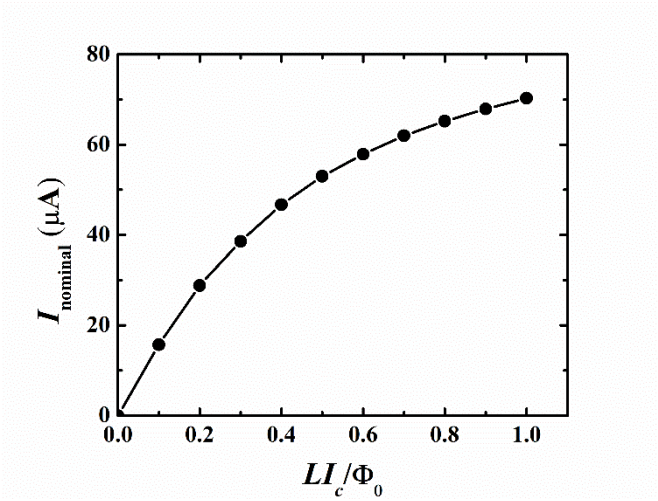

Figure 3. The nominal critical current dependence on the LI_c product normalized by Φ_0 for 0-0-π SQUIDs according to the simulation. The critical current of 0-junction and K value are 50 μA and 100, respectively.

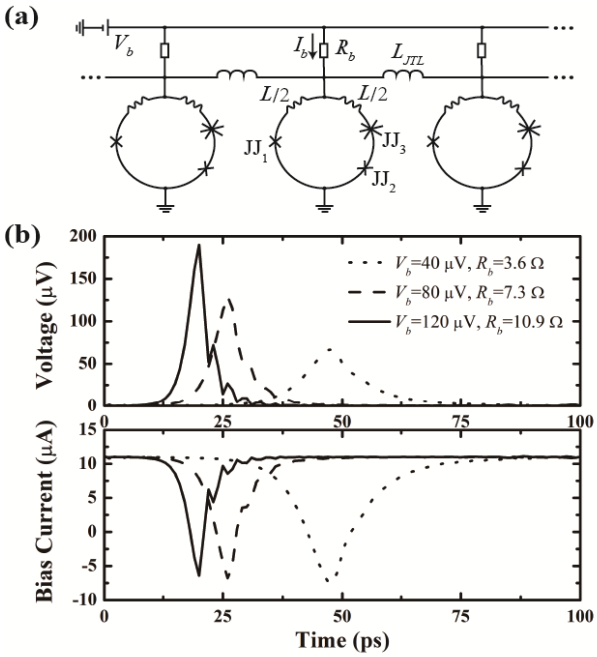

Figure 4. (a) Schematic of a JTL with HFQ circuit based on 0-0-π SQUIDs, in which JJ_1 and JJ_2 are 0-junctions and JJ_3 is a π-junction with $K > 1$. (b) The waveforms of voltages generated across the 10th 0-0-π SQUID and bias currents flowing in the bias resistor R_b for different bias voltages V_bs.

analyze the characteristics of the HFQ circuit using PJSIM. A JTL is useful because the maximum operating frequency (f_{max}) of a delay flip-flop (the essential element of an RSFQ or HFQ circuit) is almost the same as that of a JTL. Figure 4(a) shows a schematic of part of an HFQ JTL with 20 0-0-π SQUIDs. JJ_1 and JJ_2 are the switching 0-junctions, respectively, and JJ_3 is the phase-shifting π-junction. For simplicity, the shunt resistor of JJ_3 is ignored. We set LI_c/Φ_0 to 0.1 and assumed that the inductance of the L_{JTL} between adjacent 0-0-π SQUIDs was 10 pH.

As described in the introduction, hysteresis of *I-V* characteristics disappears or is very small for a 0-0-π SQUID. Thus, the 0-junctions (the switching elements) no longer require shunt resistors because the bias resistors serve in that capacity. In other words, the HFQ circuit inherently operates in a low-voltage regime. As described in [30], low-voltage regimes adopt a bias voltage $V_b < I_cR_s$, where R_s satisfies the McCumber-Stewart parameter $\beta_c = 2\pi I_cCR_s2/\Phi_0 = 1$. R_s was supposed to be 15.5 Ω to maintain the unity of β_c in the present study.

In the initial state, when there was no HFQ pulse traveling in the JTL, an identical bias current $I_b = V_b/R_b$ was supplied to each 0-0-π SQUID. R_b is the bias resistance used to distribute the desired current when the bias voltage is applied. We set I_b to a constant 0.7 $I_{nominal}$, which is identical design guideline to a conventional RSFQ circuit. The magnitude of I_b is 11 μA, which is only 22% of the minimum critical current of the smallest single junction. This lowers the power consumption of the bias resistor directly.

Figure 4(b) shows the waveforms of a voltage generated across the 10th 0-0-π SQUID (from left to right) and a bias current flowing through the corresponding bias resistor at different V_b or R_b values (40 μV/3.6 Ω, 80 μV/7.3 Ω, and 120 μV/10.9 Ω). An HFQ pulse propagates from left to right. With decreasing V_b, the height of the voltage pulse decreases linearly, and the width increases in a near-linear manner. The time integral of the voltage pulse is equal to half of the quantum flux. Thus, the signal energy is the same as that of the half-flux quantum, even in a low-voltage regime. The bias current decreases during switching of the 0-0-π SQUID, thus reducing power consumption by the bias resistors further.

3.2. Maximum Operating Frequency

We estimated the operating frequency and power consumption of LV-HFQ circuits. The f_{max} is determined by the inverse of the minimum T (T_{min}). We input a continuous pulse train of period T, which was subsequently decreased. If all 0-0-π SQUIDs switched with the same period, the JTL was considered to be functioning appropriately.

Figure 5 shows the V_b dependence of f_{max}. We examined two LI_c products of 0-0-π SQUIDs: $LI_c = 0.1\Phi_0$ and $0.2\Phi_0$. f_{max} was almost independent of the LI_c product if the SQUIDs were biased at the same initial state. In addition, f_{max} was limited by $f = 2V_b/\Phi_0$, and was roughly proportional to V_b. In the voltage

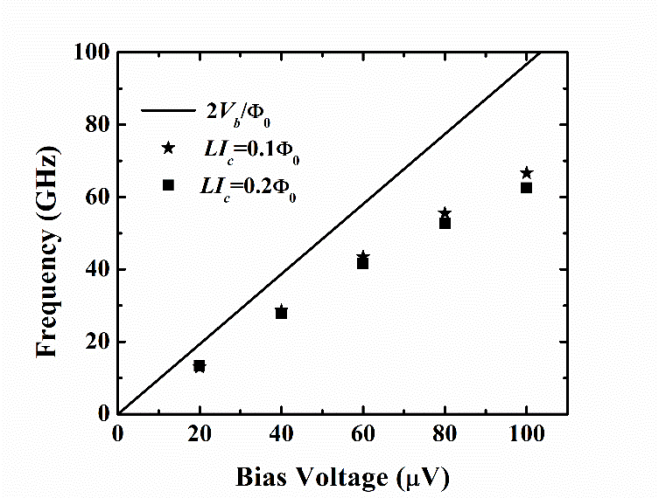

Figure 5. Maximum operating frequency as a function of bias voltage for different LI_c products in a JTL with LV-HSQ circuits. The solid line indicates the upper limit of f_{max} (expressed as $2V_b/\Phi_0$).

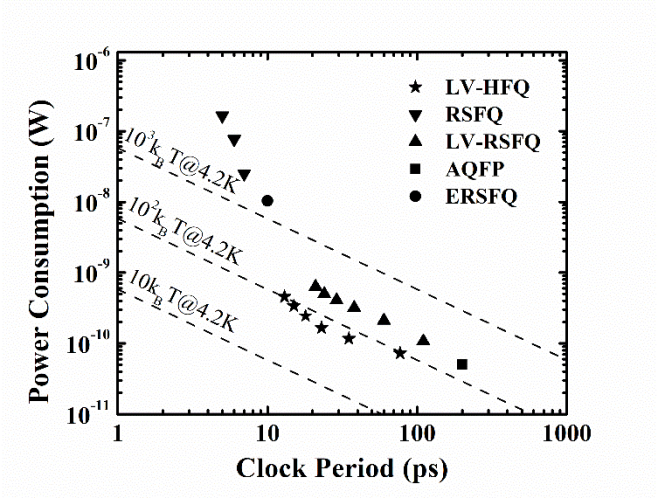

Figure 6. Power consumption of various superconducting logic circuits. The bias voltages of the LV-RSFQ and LV-HFQ circuits are 20, 40, 60, 80, 100, and 120 μV (from right to left). The RSFQ circuit is biased at 1, 2.5, and 5 mV (from right to left) and the ERSFQ circuit (without feeding JTLs) is biased at 0.5 mV. All plots were obtained by analog simulation at 10 kA/cm^2 with a minimum critical current of 50 μA, except for the AQFP which was demonstrated with 2.5 kA/cm^2 process [10].

region from 20 to 100 μV, the bias resistance ranged from 1.8 to 9.1 Ω for $LI_c = 0.1\Phi_0$ and 0.8 to 4.0 Ω for $LI_c = 0.2\Phi_0$. These resistances are much smaller than the parallel value of two subgap resistances. The total resistance R_t determines f_{max} if $R_t << R_s$. The R_t is composed of the bias resistance and the two subgap resistances. In fact, f_{max} decreased for $LI_c = 0.2\Phi_0$ compared to $LI_c = 0.1\Phi_0$ in the higher voltage range (> 80 μV), where R_b = 3.2 Ω for $LI_c = 0.2\Phi_0$, i.e., 1/30th of the value of the parallel array.

3.3. Power Consumption

The averaged power consumption of a single element in the HFQ JTL is calculated using Eq. (2). The first term within the square brackets is the power consumed by the 0-junctions and the π-junction. The second term is the power consumed by the bias resistor. The first sum is divided by 18 to calculate the average power consumption of each switching element without boundary cells (i.e., with the 1st and 20th SQUIDs excluded).

$$P = \frac{1}{18}\sum_2^{19}[\sum_1^3 \int_0^T (I_{sg}^2 R_{sg} + I_s^2 R_s)dt + \int_0^T I_b^2 R_b dt] \qquad (2)$$

Figure 6 shows the clock period dependence of the power consumption of several superconducting logic circuits. The clock period is the inverse of f_{max}. The power consumption of conventional RSFQ, ERSFQ, LV-RSFQ, and LV-HFQ circuits was simulated by PJSIM, assuming that they were all fabricated based on the same technology (I_c = 50 μA and J_c = 10 kA/cm^2). The stars indicate the simulation results of a JTL with LV-HFQ circuits based on 0-0-π SQUIDs (without shunt resistors) biased at 20, 40, 60, 80, 100, and 120 μV (from right to left). At 60 μV, the total power consumption of a switching element in LV-HFQ JTL was 0.165 nW at an f_{max} of 43.5 GHz. The power consumption and f_{max} values can meet the requirements for superconductor VLSIs, that is, below 1 nW/element over 10 GHz [31]. The simulated power consumption and maximum operating frequency are the best for LV-HFQ circuit under the presented condition.

Using the same junction parameters and bias voltages, the power efficiency (an optimization of power consumption and operating frequency of circuit) of the LV-HFQ JTL circuit was almost three-fold that of the JTL LV-RSFQ circuit. The 0-junctions of the LV-RSFQ circuit had no shunt resistors in this comparison. At the same V_b, the LV-RSFQ circuit required a lower R_b, in turn leading to a small R_t and f_{max}. In an LV-RSFQ circuit, a larger voltage drop is generated across the bias resistor; the switching element consumes considerable power. When biased at 2.5 mV, the power consumption of an RSFQ JTL circuit is about 76 nW, of which 98% is dissipated at the bias resistor. The power consumption of the ERSFQ JTL circuit remains an order of magnitude higher than that of the LV-HFQ JTL circuit. Although an AQFP can operate adiabatically with a power consumption of 0.05 nW [10], this means that the operating frequency is sacrificed. The power-delay product of an LV-HFQ JTL circuit, which is an important quality parameter, is 3.9 × 10^{-21} J, which corresponds to 70 k_BT at 4.2 K; the HFQ circuit signal energy

($I_{\text{nominal}}\Phi_0/2$) is about 200 k_BT. The difference reflects the reduced basic power consumption of a low-voltage regime.

4. Conclusion

We have discussed LV-HFQ circuits from the viewpoint of the f_{max} and power consumption. We used 0-0-π SQUIDs rather than 0-π SQUIDs in the LV-HFQ circuits. These circuits reduce basic power consumption for two reasons. First, the critical currents (I_{nominal} values) are small compared to those of single Josephson junctions, being as low as 15.7 μA when using existing VLSI superconductor fabrication technology, although I_{nominal} depends on the loop inductance of a 0-0-π SQUID. Such small currents reduce power consumption by the bias resistor. Second, the circuits operate in low-voltage regimes, wherein the bias resistance is much smaller than the parallel value of subgap resistances that serve as shunt resistors in 0-0-π SQUIDs. In such regimes, the speed of the change in the superconducting phase difference is reduced and currents flowing in the resistors are small. Numerical calculations for HFQ JTL circuits revealed that the power consumption of a single element (a 0-0-π SQUID and the bias resistor) was 0.165 nW at an f_{max} of 43.5 GHz when biased at 60 μV. Thus, this circuit is more power-efficient than all other currently available superconducting logic circuits.

Acknowledgments

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