IEICE TRANSACTIONS

on Fundamentals of Electronics, Communications and Computer Sciences

VOL. E104-A NO. 11
NOVEMBER 2021

The usage of this PDF file must comply with the IEICE Provisions on Copyright.
The author(s) can distribute this PDF file for research and educational (nonprofit) purposes only.
Distribution by anyone other than the author(s) is prohibited.

A PUBLICATION OF THE ENGINEERING SCIENCES SOCIETY
The Institute of Electronics, Information and Communication Engineers
Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3 chome, Minato-ku, TOKYO, 105-0011 JAPAN

IEICE TRANS. FUNDAMENTALS, VOL.E104–A, NO.11 NOVEMBER 2021

PAPER *Special Section on Circuits and Systems*

A Synthesis Method Based on Multi-Stage Optimization for Power-Efficient Integrated Optical Logic Circuits*

Ryosuke MATSUO[†a)], ***Nonmember***, **Jun SHIOMI**[†], **Tohru ISHIHARA**[††], ***Members***, **Hidetoshi ONODERA**[†], ***Fellow***, **Akihiko SHINYA**[†††,††††], ***and*** **Masaya NOTOMI**[†††,††††], ***Nonmembers***

SUMMARY Optical logic circuits based on integrated nanophotonics attract significant interest due to their ultra-high-speed operation. However, the power dissipation of conventional optical logic circuits is exponential to the number of inputs of target logic functions. This paper proposes a synthesis method reducing power dissipation to a polynomial order of the number of inputs while exploiting the high-speed nature. Our method divides the target logic function into multiple sub-functions with Optical-to-Electrical (OE) converters. Each sub-function has a smaller number of inputs than that of the original function, which enables to exponentially reduce the power dissipated by an optical logic circuit representing the sub-function. The proposed synthesis method can mitigate the OE converter delay overhead by parallelizing sub-functions. We apply the proposed synthesis method to the ISCAS'85 benchmark circuits. The power consumption of the conventional circuits based on the Binary Decision Diagram (BDD) is at least three orders of magnitude larger than that of the optical logic circuits synthesized by the proposed method. The proposed method reduces the power consumption to about 100 mW. The delay of almost all the circuits synthesized by the proposed method is kept less than four times the delay of the conventional BDD-based circuit.

key words: *binary decision diagram, logic circuit, optical circuit*

1. Introduction

Today's highly advanced information society would not be realizable without LSI (Large Scale Integration) technologies and optical communication technologies. Although the LSI technologies have made remarkable progress since their emergence, the effective resistivities of local level wires increase rapidly due to size effects at ultra-scaled dimensions [2]. Post-layout analysis using predictive technology models [3] shows that interconnect performance degradation may dominate over the device speed improvement in a 22 nm technology node and below. As a result, the reduction of the total delay per gate saturates around 10 ps [2]. Optical communication technologies also have been rapidly growing over the past decades. With recent advances in nanophotonics, the optical communication technologies have gradually migrated into ever-shorter distances and moved onto silicon chips as on-chip optical interconnects [4]. More recently, integrated optical circuits using nanophotonic devices attract significant interest due to its ultra-high-speed nature. The delay of an optical gate based on a nanophotonic directional coupler is on the order of a few hundreds of femtosecond [5], which is more than 10 times faster than that of the CMOS logic gates.

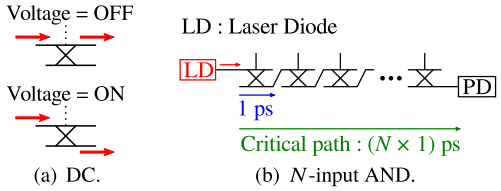


Fig. 1 Optical logic circuit using directional couplers (DC).

Many existing synthesis methods for the integrated optical circuits use a directional coupler as a basic building block. The directional coupler (DC in the following) has one voltage-control input, two optical inputs and two optical outputs. The optical routing from inputs to outputs is digitally controlled by the voltage-control signal, as shown in Fig. 1(a). Like the pass transistor logic, the Boolean logic can be constructed by serially connecting the DCs. Once the input voltage is given, the latency of the DC is determined by only the speed of the light passing through the DC. In the optical circuit for N-input AND operation, as shown in Fig. 1(b), the latency is N picoseconds (1 ps delay per DC in this paper). Note that the photodetector (PD) in Fig. 1(b) receives the light from the laser diode (LD) if and only if all the voltage-inputs are the ON state. Therefore the optical circuit in Fig. 1(b) operates as an N-input AND gate. In order to implement general and larger-scale logic functions, automated design methods exploiting the ultra-high-speed nature of the DC are proposed based on various schemes such as directed logic (DL) [6], virtual gates [7] and Binary Decision Diagram (BDD) [8]–[11]. However, optical logic circuits synthesized by these methods suffer from power explosion. This is because light signals from a laser source exponentially attenuate as they propagate through optical devices. As a result, the power dissipation of typical optical logic circuits is exponential to the number of inputs of the target logic functions, which may limit the scalability of optical logic circuits. To address this issue, the design method for signal restoration using Optical-to-Electrical (OE) converters is proposed

Manuscript received November 24, 2020.
Manuscript publicized May 18, 2021.
[†]The authors are with Graduate School of Informatics, Kyoto University, Kyoto-shi, 606-8501 Japan.
[††]The author is with Graduate School of Informatics, Nagoya University, Nagoya-shi, 464-0814 Japan.
[†††]The authors are with NTT Nanophotonics Center, Atsugi-shi, 243-0198 Japan.
[††††]The authors are with NTT Basic Research Laboratories, Atsugi-shi, 243-0198 Japan.
*This work was partly presented in the conference [1].
a) E-mail: matsuo.ryosuke.25r@st.kyoto-u.ac.jp
DOI: 10.1587/transfun.2020KEP0018

Copyright © 2021 The Institute of Electronics, Information and Communication Engineers

[12]. Although this method largely reduces the signal power attenuation, insertion of OE converters leads to an increase of delay since the OE conversion delay is considerably larger than the light propagation delay of DCs.

In this paper, we propose a synthesis method for power-efficient and high-speed optical logic circuits based on the signal restoration using OE converters. The proposed synthesis method divides a target function to multiple sub-functions. As a result, the proposed synthesis method enables to reduce the power consumption to a polynomial order of the number of inputs of the target logic function. Moreover, our method can mitigate the OE converter delay overhead by parallelly excuting the sub-functions. The proposed method thus exponentially reduces the power consumption without sacrificing the high-speed property of light.

This paper is an extension of our previous work [1]. In [1], we proposed a synthesis method for multi-stage BDD-based optical logic circuits. In this paper, we add a design method of BDD-based optical logic circuits for reducing the power consumption to the synthesis flow proposed in [1]. Moreover, we numerically demonstrate that our method reduces the power consumption to a polynomial order of the number of inputs of the target logic functions with practical benchmark sets.

The rest of this paper is organized as follows. Section 2 presents related works and our contribution. Section 3 shows a basic concept of a multi-stage BDD-based optical logic circuit. The synthesis method for reducing the power consumption considering the tradeoff between the delay and the power consumption is also presented in Sect. 3. Section 4 shows the experimental results obtained using ISCAS'85 benchmark circuits. Section 5 concludes this paper.

2. Related Work

This paper uses a DC as a basic building block. There are two ways to connect DCs: serial-connection and cascade-connection. In the serial-connction, once the input voltages are given, the latency is determined by the speed of the light passing through the serially connected DCs. In the cascade-connection, on the other hand, the OE conversion based on a PD is required in order to control the direction of the light passing through the DCs. The OE conversion delay is much larger than the light propagation time in the serial-connection. For example, the serial connection delay of the DC presented in [13] is 1 ps per DC, while the OE conversion delay is 25 ps [14]. In order to exploit the light speed, conventional design methods thus mainly use the serial-connection. However, one of the biggest issues in the serial-connection is a large insertion loss of the final output since the attenuation of the final output signal power is exponential to the number of DCs connected in series. If the intensity of the output optical signal is not sufficiently large, the signal detection time may increase and the circuit may result in failure of detection due to noise. This issue can be mitigated by inserting cascade-connection. Cascade-connection largely reduces the signal power attenuation since

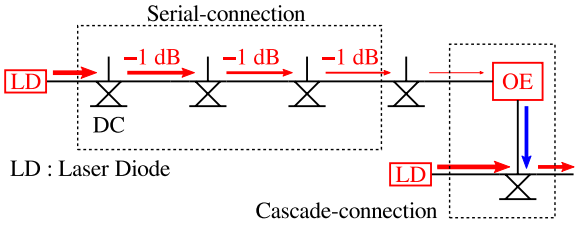


Fig. 2 Serial-connection and cascade-connection.

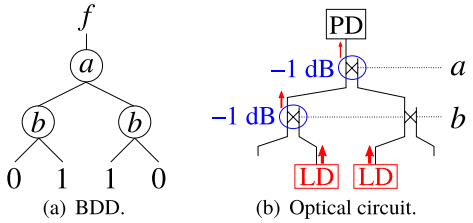


Fig. 3 Single-stage optical logic circuit.

it repeats the light signal as shown in Fig. 2 [15].

Let us define an optical logic circuit consisting of serial-connection only as a single-stage optical logic circuit. Single-stage optical logic circuits have a high-speed characteristic but have a power-consuming characteristic. Optical logic circuits based on BDD or DL are single-stage optical logic circuits. Figure 3(a) shows the BDD representing $f = (\neg a \wedge b) \vee (a \wedge \neg b)$. f operates as an exclusive-or (XOR) function. Figure 3(b) shows the circuit based on the BDD shown in Fig. 3(a). In BDD-based designs [8]–[11], we consider a root and leaves as an optical output and optical sources, respectively. If the i-th terminal node value is 1, a light is given as the optical source of the circuit. In the optical implementation of BDD, we use a DC as the BDD node. The electrical inputs of the logic function are fed into DCs corresponding to the BDD nodes in order to control the direction of the lights. Although the speed of the BDD-based circuit is very fast as it is determined by the speed of the light passing through serially connected DCs, the power dissipation is exponential to the number of inputs (1 dB per DC in this paper). The strategy of the node elimination based on BDD reduction rules can effectively reduce the number of DCs. However, it is hard to avoid the explosion of the power consumption [10].

The cascade-connection can reduce the power dissipation of the laser source. In the best case, the latency can also be improved [15]. Let us define an optical circuit which has cascade-connection on its critical path as a multi-stage optical logic circuit. Figure 4 shows the multi-stage optical logic circuit for 16-input AND operation. In a single-stage optical logic circuit, the number of DCs connected in series is 16. On the other hand, in the circuit shown in Fig. 4, the number of DCs connected in series is 4, which exponentially reduces the power consumption. The power dissipated by a laser source in the single-stage optical logic circuit is 355 μW while the total power dissipated by the five laser sources in the multi-stage optical logic circuit is 97.7 μW. Note that the

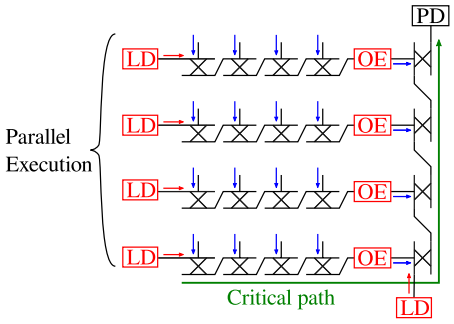


Fig. 4 Multi-stage optical logic circuit (16-input AND operation).

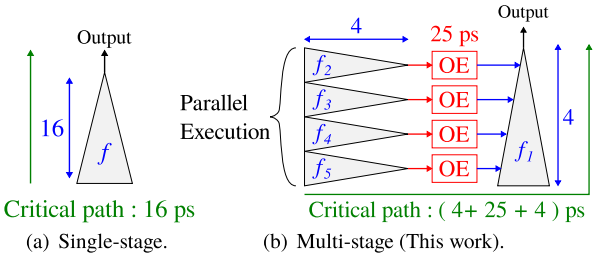


Fig. 5 Concept of BDD-based multi-stage optical logic circuit.

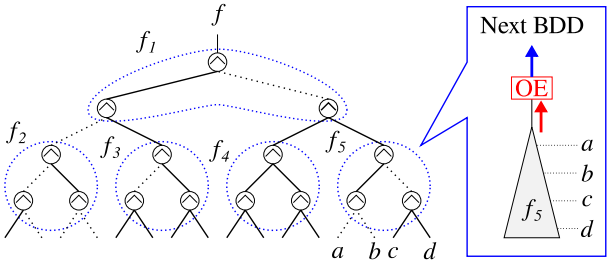


Fig. 6 Example of division of AIG.

minimum detectable optical power at PDs is assumed to be 10 μW in this example. Moreover, since the OE conversion delay can be mitigated by parallel execution of sub-circuits, in the best case, delay of a multi-stage optical logic circuit is also reduced compared to that of a single-stage optical logic circuit [15]. Synthesis methods for the optimization of multi-stage optical logic circuits are proposed in [15]. In this paper, "multi-stage optimization" is defined as the optimization of multi-stage optical logic circuits. However, the target logics of the synthesis method proposed by [15] are limited to simple logic functions such as AND, OR, and XOR.

To solve this problem, this paper proposes a synthesis method of optical logic circuits for general and complex functions. Our contributions are summarized below.

- This paper proposes a synthesis method for multi-stage optical logic circuits for any logic functions. Our synthesis method reduces the power consumption of optical logic circuits from an exponential order of n to a polynomial order of n, where n is the number of inputs of the target logic function. The proposed method also reduces the delay in the best case compared to the single-stage optical logic circuits.
- Experimental results obtained using the ISCAS'85 benchmark circuits show our method exponentially reduces the power consumption of all benchmark circuits. For example, in the circuit for c6288 (16×16 mltiplier), the power consumption is reduced by seven orders of magnitude. Our synthesis enables to design optical logic circuits with an acceptable power consumption for practical use, even if the target function has a large number of inputs. Moreover, in some benchmark circuits, the delay is also reduced. In the worst case, however, the delay is increased by one order of magnitude. Finally, we numerically demonstrate that our method reduces the power consumption to a polynomial order of the number of inputs of the target logic function with a c7552 benchmark circuit.

3. BDD-Based Multi-Stage Optical Circuit

3.1 Concept

The concept of a BDD-based multi-stage optical logic circuit is shown in Fig. 5. Figure 5(a) shows a BDD-based single-stage optical logic circuit. The circuit corresponds to the function f with 16 inputs. In the BDD-based multi-stage optical logic circuit, as shown in Fig. 5(b), the original 16-input BDD is divided into multiple 4-input BDDs in order to avoid an explosion of the power consumption since the power dissipation of optical circuits is exponential to the number of inputs. In each sub-circuit corresponding to the sub-functions f_1, f_2, f_3, f_4 and f_5, four DCs are serially connected. The attenuation in the power of the light signals is largely reduced compared to a BDD-based single-stage optical logic circuit. The optical output signals of the divided BDDs (f_2, f_3, f_4, and f_5) are converted using OE converters. The converted electrical signals are then fed into the directional couplers in the successor BDD (f_1) as shown in Fig. 5(b). The state-of-the-art integrated OE converter achieves a 25 ps conversion latency [14]. However, the 25 ps latency is still much larger than the light propagation time. This paper assumes the directional coupler propagation delay is 1 ps per DC [13]. The proposed synthesis method can mitigate this OE converter delay overhead by parallelizing the divided BDDs as shown in Fig. 5(b). In the best case, the propagation delay of the circuit based on the proposed design is smaller than that of the BDD-based single-stage circuit. For example, if the function f is a 64-input AND operation, the original 64-input BDD can be divided into multiple 8-input BDDs. The delay of the circuit based on the proposed design is 8 + 25 + 8 = 41 ps, which is smaller than that of the 64-input BDD-based circuit.

In the rest of this subsection, this paper presents the overview of the synthesis method for multi-stage optical logic circuits. Initially, we apply a logic optimization based on And-Inverter Graph (AIG) to the target function f. Figure 6 shows the AIG represents target function f. An AIG

is expressed as a directed acyclic graph (DAG) in which each node except for leaves has two children and operates as AND function of the two children. The edges with a dotted line represent logical negation. Primary inputs are given to leaves. For example, f_5 shown in Fig. 6 represents $(\neg a \wedge \neg b) \wedge \neg(c \wedge d)$. Then, we divide the AIG into several sub-graphs corresponding to sub-functions f_1, f_2, f_3, f_4 and f_5 with blue dotted curves in Fig. 6. Finally, each sub-function is implemented by a BDD-based optical logic circuit. The optical output signal of a sub-circuit is fed into the directional coupler in the successor sub-circuit since the optical routing from inputs to outputs at a DC is controlled by the electrical signal. The BDD labeled as f_5 in Fig. 5(b) is obtained by the above procedure. The rest of this section discusses a synthesis method for reducing the power consumption considering the tradeoff between the delay and the power consumption.

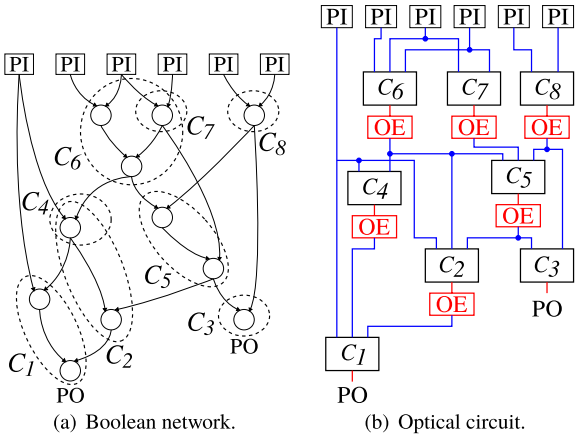
3.2 Synthesis Method

The synthesis flow is summarized below.

1. Apply an AIG-based logic optimization to the target function.
2. Divide the AIG to multiple sub-functions.
3. Implement a single-stage optical logic circuit to several sub-functions.

Firstly, this paper discusses an optimization method for dividing the AIG. Let us define this optimization problem as the partition mapping problem. This paper gives a precise problem formulation and some preliminaries. AIG can be represented as a DAG called Boolean network where each node represents a logic element. A directed edge (i, j) exists if the output of logic element i is an input of logic element j. A primary input (PI) node has no incoming edge and a primary output (PO) node has no outgoing edge. We use $input(v)$ to denote the set of nodes which are fanins of logic element v. Given a sub-graph H of the Boolean network, $input(H)$ denotes the set of distinct nodes outside H which supply inputs to the logic element in H. For a node v in the network, a *cone* at v, which is simply denoted by C_v, is a sub-graph, which consists of v and its predecessors, such that there exist paths connecting from any node in C_v to v. The *level* of a node v is the length of the longest path from any PI node to v. The level of a PI node is zero. The *depth* of a network is the largest node level in the network. In the Boolean network shown in Fig. 7(a), the depth is 6.

In the proposed method, each sub-circuit in a multi-stage optical circuit is a BDD-based optical circuit that can operate as any Boolean function. Thus, any cone of a Boolean network can be implemented with single-stage BDD-based optical circuits. The partition mapping problem for multi-stage optical circuits is defined as the problem to cover a given Boolean network with cones. A partition mapping solution S is a DAG where each cone is replaced with a node. A directed edge (C_u, C_v) exists if there is a edge between the two cones. In Fig. 7(a), dotted curves show the

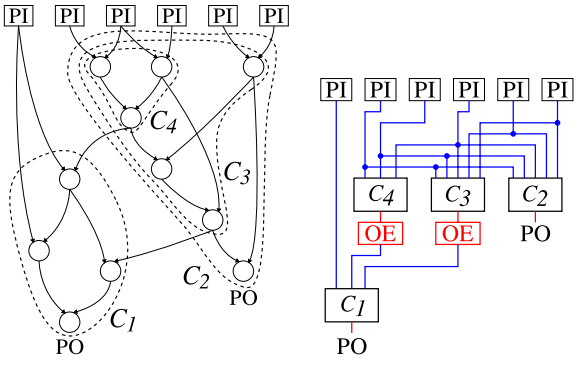


(a) Boolean network. (b) Optical circuit.

Fig. 7 Partition mapping solution and implementation by optical circuit.

example of the mapping solution, where the depth is 4 and the number of cones is 8. Let us explain the procedure to generate a mapping solution. Let L be the set of nodes. A cone C_v ($v \in L$) is to be mapped. Initially, L contains all the PO nodes. We process the nodes in L one by one. We remove a node v from L and map the C_v, then insert the nodes $u\,(\in input(C_v))$ to L. When a node u has been already inserted, we do not insert a node u to L. We iterate this manipulation. This procedure ends when L consists of only PI nodes of the original network.

Figure 7(b) shows the circuit based on the mapping solution shown in Fig. 7(a). Each cone is implemented by a BDD-based optical circuit and each edge is implemented by a cascade-connection in BDD-based multi-stage optical logic circuits. The delay of a BDD-based multi-stage optical logic circuit is determined by two factors: the delay in sub-circuits and the delay in the interconnection paths (i.e., the OE conversion delay). Each BDD-based sub-circuit has a constant delay of n ps (where n is the number of inputs) which is independent of original target function. Each edge in the mapping solution corresponds to a constant delay of 25 ps since each edge is implemented with a cascade-connection. Note that this paper assumes that the OE conversion delay is 25 ps [14]. In this case, the delay largely depends on the depth of the mapping solution. The power consumption of a BDD-based multi-stage optical logic circuit is determined by two factors: the number of sub-circuits and the power consumption in sub-circuits. Intuitively, a large number of sub-circuits cause the increase of the power consumption. Since the power consumption of a BDD-based optical circuit is exponential to the number of inputs, we limit the number of inputs of cones in the mapping solution in order to avoid the exponential power explosion. Therefore, the primary objective of our method is to find a mapping solution that satisfies the constraint of the number of inputs in a cone. The secondary objective is to reduce the depth and the number of cones in the mapping solution. A LookUp-Table-based (LUT-based) Field-Programmable Gate Array (FPGA) technology mapping algorithm is suitable for this optimization. Therefore, we use the mapping algorithm in the synthesis

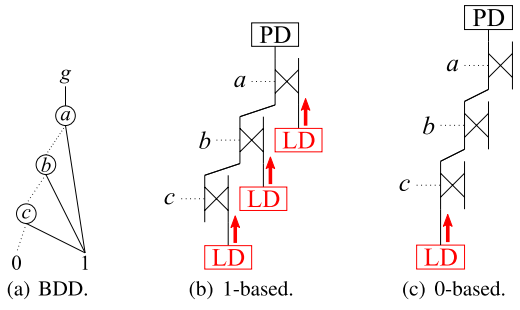


(a) Boolean network. (b) Optical circuit.

Fig. 8 Partition mapping solution and implementation by optical circuit in which the constraint of the number of inputs of an LUT is relaxed.

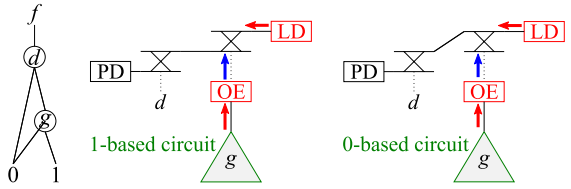
flow. Synthesis results largely depend on a constraint of the number of inputs in a cone, which corresponds to the number of inputs of an LUT in FPGA technology mapping. The delay and the power consumption are reduced and increased as the number of inputs of an LUT increases, respectively. The mapping solution, as shown in Fig. 7(a), satisfies the constraint that the number of inputs in a cone is 3. Fig. 8(b) shows the circuit based on the mapping solution shown in Fig. 8(a), in which the constraint is relaxed to 5. In the circuit shown in Fig. 8(b), the number of OE conversions on the critical path and the number of sub-circuits are reduced compared to the circuit shown in Fig. 7(b). When LUTs can have a larger number of inputs, the depth of the mapping solution may be reduced, which reduces the number of time-consuming OE conversions on the critical path. However, the number of inputs in each sub-circuits increases. This may lead to a significant increase in the power consumption since the power consumption of each sub-circuit is exponential to the number of its inputs. Therefore, it is very important to consider the tradeoff between the delay and the power consumption.

In the proposed method, the sub-graphs obtained by the above procedure are implemented by the BDD-based design method. In Sect. 2, we explained that the 1-terminal nodes corresponded to the optical source. However, in some cases, we can reduce the power consumption by using the 0-terminal nodes as the optical source. Consider the example of 3-input OR function $g = a \vee b \vee c$ shown in Fig. 9(a). The edges with a solid(dotted) line represent 1(0)-edge. Figs. 9(b) and 9(c) show the two circuit design in which an optical source is located at the leaf corresponding to the 1-terminal node and the 0-terminal node, respectively. Let us define these two circuit design as 1-based circuit design and 0-based circuit design, respectively. The 1-based circuit design shown in Fig. 9(b) has three paths from the output to the optical source. On the other hand, since the 0-based circuit design shown in Fig. 9(c) has a single path from the output to the optical source, the power consumption of the 0-based circuit design is smaller than that of the 1-based circuit design. Therefore, we compare the power consumption of the 1-based circuit design with the 0-based circuit design, then



(a) BDD. (b) 1-based. (c) 0-based.

Fig. 9 Implementation of BDD g.



(a) BDD. (b) 1-based. (c) 0-based.

Fig. 10 Implementation of BDD f.

adopt the circuit design that has smaller power consumption. When we mix these two circuit designs for implementing sub-graphs, the connection between a BDD and its subsequent BDDs should be modified. This is because the output optical signal is inverted if we use 0-based circuits. In this paper, we propose the design method to address this issue. The DC has two optical inputs and two optical outputs. Let us define the optical input corresponding to a 1(0)-edge in a BDD as 1(0)-edge input, and the optical output on the side of 1(0)-edge input as 1(0)-edge output. Taking an example of the DC corresponding to the node labeled by b in Fig. 9(b), the lower left port is a 0-edge input. The lower right port is a 1-edge input. The upper left port is a 0-edge output. The upper right port is a 1-edge output. Consider the example of the multi-stage BDD-based optical logic circuit for the logic function $f = d \wedge g$ ($g = a \vee b \vee c$) shown in Fig. 10(a). When we adopt the 1-based circuit design, we connect the downside optical output (0-edge output) of the DC corresponding to the node labeled by g (DC labeled by g in the following) to the DC corresponding to the node labeled by d (DC labeled by d in the following) in the next circuit as shown in Fig. 10(b). When $a = 1, b = 0, c = 0, d = 1$ ($f = 1$), an electrical signal is given to the DC labed by g and the input light of the next circuit passes through that DC, then the light is detected at the PD. On the other hand, when we adopt the 0-based circuit design, we connect the upside optical output (1-edge output) of the DC labeled by g to the DC labeled by d as shown in Fig. 10(c). When $a = 0, b = 0, c = 0, d = 1$ ($f = 0$), an electrical signal is given to the DC labeled by g and the input light of the next circuit does not pass through that DC, then the light is not detected at the PD. In summary, we connect the 0(1)-edge output of the DC controlled by 1(0)-based circuit design to the DC corresponding to the parent node in a next BDD-based circuit. The proposed design method can

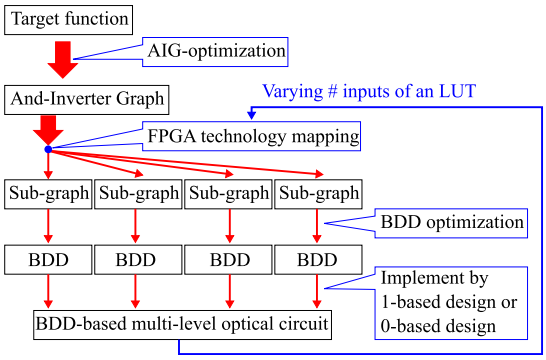


Fig. 11 Synthesis flow.

reduce the power consumption while maintaining a correct output value of a multi-stage optical logic circuit.

In summary of this section, we show the synthesis flow in Fig. 11. Initially, we apply a logic optimization based on AIG to the target function. Then we divide the AIG into several sub-graphs using an LUT-based FPGA technology mapping algorithm. Next, we convert each sub-graph to a BDD. We compare the power consumption of the 1-based circuit design with the 0-based circuit design, then adopt the circuit design that has smaller power consumption. In oreder to obtain the tradeoff between the delay and the power consumption, we vary the number of inputs of an LUT in the mapping algorithm.

4. Performance Evaluation Based on ISCAS'85 benchmark

In this section, the proposed synthesis method is applied to the ISCAS'85 benchmark circuits [16]. In order to evaluate the performance of optical logic circuits, this paper assumes that the propagation delay of a light passing through a DC is 1 ps [13]. The delay of the OE conversion is assumed to be 25 ps [14]. We assume that the power attenuation in a DC is -1 dB [13]. The minimum optical power which the PD can detect is assumed to be 10 μW. In this paper, we assume that the energy overhead of the OE conversion is negligible compared to the power dissipation of the laser source.

4.1 Comparison between Single-Stage Circuits with Multi-Stage Circuits

In our synthesis method, we use the AIG-optimization and the LUT technology mapping algorithm provided by "ABC" [17]. In BDD-based multi-stage optical logic circuits, we utilize "CUDD" [18] by building BDDs corresponding to each sub-graph. The circuit specifications of ISCAS'85 benchmark are summarized in Table 1. The PI/PO value is the total number of PIs/POs in the benchmark circuits. A target circuit has multiple POs. Each logic function corresponding to each PO is individually implemented by one optical logic circuit. For example, since c432 has 7 POs, 7 optical logic circuits are required to design c432. In Tables 2 and 3, the "Delay (single)" values represent the delay

Table 1 Specification of ISCAS'85 benchmark circuits.

Circuit	Function	PI / PO	Max input
c432	27-channel interrupt controller	36 / 7	36
c880	8-bit ALU	60 / 26	45
c1355	32-bit SEC circuit	41 / 32	41
c1908	16-bit SEC/DED circuit	33 / 25	33
c2670	12-bit ALU and controller	223 / 140	122
c3540	8-bit ALU	50 / 22	50
c5315	9-bit ALU	178 / 123	67
c6288	16×16 multiplier	32 / 32	32
c7552	32-bit adder/comparator	207 / 108	194

Table 2 Synthesis result of ISCAS'85 benchmark circuits (small set).

Circuit name	c432	c880	c1355	c1908	c2670
Power (Multi) [mW]	13.8	15.2	58.8	26.0	19.8
Delay (Multi) [ps]	145	107	74	135	103
Delay (Single) [ps]	36	45	41	33	122

Table 3 Synthesis result of ISCAS'85 benchmark circuits (large set).

Circuit name	c3540	c5315	c6288	c7552
Power (Multi) [mW]	84.3	43.1	79.6	68.4
Delay (Multi) [ps]	150	135	635	135
Delay (Single) [ps]	50	67	32	194

of benchmark circuits based on single-stage BDD. The delay is less than or equal to (# PIs) $\times$ 1 ps since not all PIs are necessarily given to the optical circuits corresponding to each PO. For example, although c880 has 60 PIs, the delay is 45 ps. Benchmark circuits based on single-stage BDD have huge power consumption compared to CMOS logic circuits. For example, the power consumption of c6288 based on single-stage BDD is on the order of megawatts. Although the circuit size of c432 is small compared to other benchmark circuits, the power consumption is expected to be on the order of kilowatts.

The proposed synthesis method based on the LUT technology mapping algorithm is applied to the ISCAS'85 benchmark circuits, varying the number of inputs of an LUT from 2 to 10 in the partition mapping phase. The synthesis results are summarized in Tables 2 and 3. The specification of the circuits based on the proposed synthesis method corresponds to the first row and the second row in Tabels 2 and 3. The "Power (multi)" values represent the total power dissipated by the laser sources in the multi-stage optical logic circuits. In this paper, we compare a 1-based circuit design and a 0-based circuit design based on a BDD built by "CUDD" for implementing each sub-graph. An ordering algorithm provided by "CUDD" makes each BDD compact, which reduces the power consumption of BDD-based optical circuits. Therefore, the power consumption of multi-stage optical logic circuits is smaller than the results in our previous work [1]. The "Delay (multi)" values are estimated by total delay of sub-circuits and the number of OE conversions, on the critical path. The delay value shown in Tables 2 and 3 is the smallest among synthesis results under a power constraint of a 100 mW. The proposed synthesis method reduces the power consumption to under 100 mW. The delay

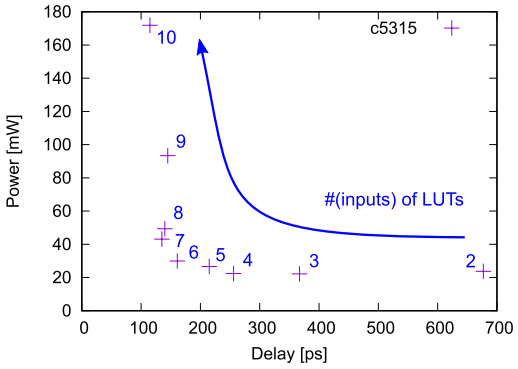


Fig. 12 Characteristics of delay and power consumption (c5315).

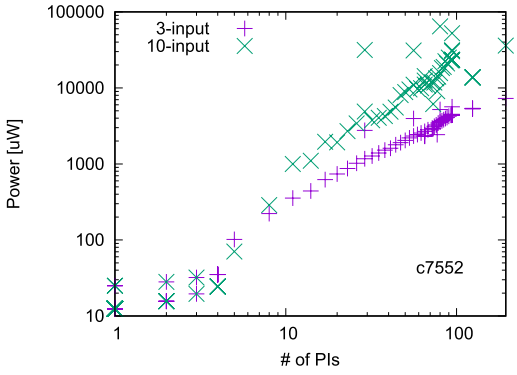


Fig. 13 Characteristics of power consumption and # PIs.

Table 4 Partition mapping solution (c5315).

Max # input	Depth	# cones	Average # inputs
2	26	1389	1.98
3	14	768	2.66
4	9	501	3.29
5	8	362	3.95
6	6	304	4.32
7	5	273	4.89
8	5	237	5.06
9	5	236	5.56
10	4	228	5.89

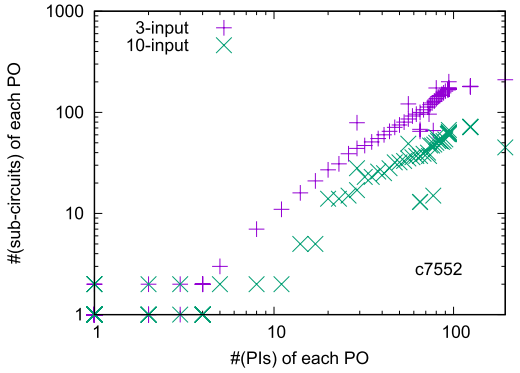


Fig. 14 Characteristics of # sub-circuits and # PIs.

of the circuits synthesized by the proposed method is kept less than about four times the delay of the single-stage circuits except for c6288. Especially, in the circuits for c2670 and c7552, our method reduces the delay and power simultaneously since the strategy of parallelizing the sub-circuits works well. In the circuit for c6288, although the proposed method increases the delay by 20 times, it reduces the power consumption by seven orders of magnitude. Note that the primary goal of this paper is providing new approaches to improve the power consumption of optical logic circuits to the level of practical values without sacrificing the ultra-high-speed characteristic. If we simply design c6288 based on single-stage optical logic circuits, the power consumption is on the order of megawatts which is not an acceptable value for practical use. The proposed method thus can resolve the scalability issue in terms of the power explosion.

4.2 Tradeoff between the Power Consumption and the Delay

Figure 12 and Table 4 show synthesis results obtained by varying the number of inputs of an LUT from 2 to 10 in the partition mapping phase. The values of partition mapping solutions are also summarized in Table 4. "Max # inputs" represents the maximum number of inputs of an LUT in the partition mapping phase. "Average # inputs" represents the average number of inputs of a cone in the mapping solution. Figure 12 and Table 4 show the synthesis results for c5315. Experiments for other benchmark circuits also show a similar characteristic in terms of the delay and the power consumption. It is observed that the delay is reduced and the power consumption is exponentially increased as the number of inputs of an LUT in the partition mapping phase increases. Note that the proposed method can reduce the power consumption of optical circuits considering the tradeoff between the delay and the power consumption, which helps designers optimize the circuit depending on their design goals and constraints.

4.3 Polynomial Relationship between the Power Consumption and the Number of Inputs

We demonstrate that our method reduces the power consumption to a polynomial order of the number of inputs of the target logic functions. It is hard to see the relationship between the number of inputs and the power consumption from the number of PIs and the power consumption of benchmark circuits in Table 1. This is because the logic complexity and the number of POs are considerably different between benchmark circuits. Therefore, we focus on one benchmark circuit. Logic functions corresponding to each PO in one benchmark circuit are separately extracted. We consider the relationship between the number of PIs and the power consumption in each PO. For this experiment, we use the c7552 benchmark circuit since c7552 has a variety number of PIs associated with each PO compared with other benchmark circuits. Figures 13, 14, and 15 show the results obtained by mapping 3-input LUTs to c7552 and the results obtained by mapping 10-input LUTs to c7552, respectively. Note that

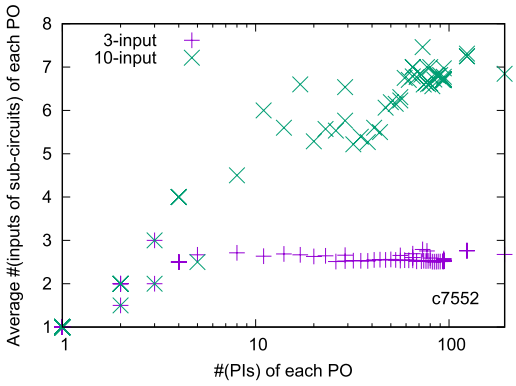


Fig. 15 Characteristics of average # inputs and # PIs.

the proposed optimization method is allowed to use smaller LUTs than 3-/10-input LUTs. The smaller LUTs are typically utilized for functions which are not on a critical path. Experiments for other benchmark circuits also show a similar characteristic. Figure 13 shows characteristics of the power consumption and the number of PIs associated with each PO in a log-log graph. The power consumption is a polynomial of the number of PIs in both two cases since they are on a straight line in a log-log plot. Fig. 14 shows characteristics of the number of sub-circuits and the number of PIs given to each PO in a log-log graph. Fig. 15 shows characteristics of the average number of inputs of sub-circuits and the number of PIs given to each PO in a semi-log graph. First, we consider the results obtained by mapping 3-input LUTs. The two graphs shown in Figs. 13 and 14 have almost the same slope. It is observed that the average number of inputs of sub-circuits does not depend on the number of PIs from Fig. 15. Since the power consumption of BDD-based optical circuits is dominated by the number of inputs, the average power consumption of sub-circuits also does not depend on to the number of PIs. Therefore, the power consumption of multi-stage optical logic circuits increases with the same slope in a log-log plot as the number of sub-circuits increases. On the other hand, in the results obtained by mapping 10-input LUTs, the average number of inputs of sub-circuits increases as the number of PIs increases from Fig. 15. This is because the ABC uses small LUTs for sub-circuits on non-critical paths. This makes the slope in Fig. 13 steeper than the 3-input LUT design, since power-hungry large sub-circuits are utilized more than small sub-circuits. The above discussion shows that the power consumption of logic functions is reduced to the polynomial order of the number of their inputs.

5. Conclusion

Existing synthesis methods for optical logic circuits result in an explosion of the power consumption. To address this issue, this paper proposed the power consumption reduction method based on multi-stage optimization using OE converters while exploiting the high-speed nature of optical logic circuits. The proposed synthesis method can mitigate the OE converter delay overhead by parallelizing sub-circuits. Experimental results obtained using ISCAS'85 benchmark circuits demonstrated that our method reduces the power consumption of optical logic circuits to a polynomial order of the number of inputs of the target logic function. without sacrificing the ultra-high-speed characteristic. It also offers designers the tradeoff between the delay and the power consumption. Our future work will be focused on developing algorithms which optimize the optical circuit based on their design goals and constraints.

Acknowledgments

This work is partly supported by JST CREST Grant Number JPMJCR15N4 and MEXT/JSPS KAKENHI Grand Number 20H04155.

References

[1] R. Matsuo, J. Shiomi, T. Ishihara, H. Onodera, A. Shinya, and M. Notomi, "A synthesis method for power-efficient integrated optical logic circuits towards light speed processing," 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp.488–493, 2020.
[2] A. Ceyhan, M. Jung, S. Panth, S.K. Lim, and A. Naeemi, "Impact of size effects in local interconnects for future technology nodes: A study based on full-chip layouts," Proc. IEEE Interconnect Technology Conference/Advanced Metallization Conference, pp.345–348, May 2014.
[3] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm early design exploration," IEEE Trans. Electron Devices, vol.53, no.11, pp.2816–2823, Nov. 2006.
[4] Y. Vlasov, "Silicon photonics for next generation computing systems," Proc. European Conference on Optical Communications, pp.1–2, Sept. 2008.
[5] N. Yamamoto, T. Ogawa, and K. Komori, "Photonic crystal directional coupler switch with small switching length and wide bandwidth," Opt. Express, vol.14, no.3, pp.1223–1229, Feb. 2006.
[6] J. Hardy and J. Shamir, "Optics inspired logic architecture," Opt. Express, vol.15, no.1, pp.150–165, Jan. 2007.
[7] C. Condrat, P. Kalla, and S. Blair, "Logic synthesis for integrated optics," Proc. Great lakes symposium on VLSI, pp.13–18, May 2011.
[8] R. Wille, O. Keszocze, C. Hopfmuller, and R. Drechsler, "Reverse BDD-based synthesis for splitter-free optical circuits," Proc. Asia-South Pacific Design Automation Conference, pp.172–177, Jan. 2015.
[9] Z. Zhao, Z. Wang, Z. Ying, S. Dhar, R.T. Chen, and D.Z. Pan, "Logic synthesis for energy-efficient photonic integrated circuits," Proc. Asia-South Pacific Design Automation Conference, pp.355–360, Jan. 2018.
[10] R. Matsuo, J. Shiomi, T. Ishihara, H. Onodera, A. Shinya, and M. Notomi, "BDD-based synthesis of optical logic circuits exploiting wavelength division multiplexing," Proc. Asia-South Pacific Design Automation Conference, pp.355–360, Jan. 2019.
[11] Z. Zhao, D. Liu, Z. Ying, B. Xu, C. Feng, R.T. Chen, and D.Z. Pan, "Exploiting wavelength division multiplexing for optical logic synthesis," 2019 Design, Automation Test in Europe Conference Exhibition (DATE), pp.1567–1570, March 2019.
[12] Z. Zhao, J. Gu, Z. Ying, C. Feng, R.T. Chen, and D.Z. Pan, "Design technology for scalable and robust photonic integrated circuits: Invited paper," 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp.1–7, Nov. 2019.
[13] H.C. Nguyen, N. Yazawa, S. Hashimoto, S. Otsuka, and T. Baba, "Sub-100 μm photonic crystal Si optical modulators: Spectral, athermal, and high-speed performance," IEEE J. Sel. Topics Quantum

Electron., vol.19, no.6, pp.127–137, June 2013.
[14] K. Nozaki, S. Matsuo, T. Fujii, K. Takeda, A. Shinya, E. Kuramochi, and M. Notomi, "Femtofarad optoelectronic integration demonstrating energy-saving signal conversion and nonlinear functions," Nature Photonics, vol.13, pp.454–459, July 2019.
[15] T. Egawa, T. Ishihara, H. Onodera, A. Shinya, S. Kita, K. Nozaki, K. Takata, and M. Notomi, "Multi-level optimization for large fan-in optical logic circuits using integrated nanophotonics," IEEE International Conference on Rebooting Computing, pp.43–50, Nov. 2018.
[16] B.F. and F.H., "A neural netlist of ten combinational benchmark circuits and translator in fortran," Int. Symp. Circuits and Systems (ISCAS), pp.663–698, June 1985.
[17] Berkeley Logic Synthesis and Verification Group, ABC: A System for Sequential Synthesis and Verification, available online.
[18] F. Somenzi, "CUDD: CU decision diagram package," available online.

Ryosuke Matsuo received his B.E. degree in electronic engineering, the M.E. degree in communications and computer engineering from Kyoto University, Kyoto, Japan, in 2018 and 2020, respectively. He is currently working toward the Ph.D. degree at the communications and computer engineering from Kyoto University. His research interests include optical circuit architecture and design methodologies for optical circuits.

Jun Shiomi received the B.E. degree in electrical and electronics engineering, the M.E. degree in communications and computer engineering, and the Ph.D. degree in Informatics from Kyoto University, Kyoto, Japan, in 2014, 2016 and 2017, respectively. From 2016 to 2017, he was a Research Fellow of the Japan Society for the Promotion of Science. Since 2017, he has been an Assistant Professor with the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University. His research interests include modeling and computer-aided design for low power and low voltage system-on-chips.

Tohru Ishihara received his B.E., M.E., and Dr.E. degrees in computer science from Kyushu University in 1995, 1997 and 2000 respectively. From 1997 to 2000, he was a Research Fellow of the Japan Society for the Promotion of Science. For the next three years he worked as a Research associate in VLSI Design and Education Center, the University of Tokyo. From 2003 to 2005, he was with Fujitsu Laboratories of America, Inc. as a member of research staff. For the next five years, he was with System LSI Research Center, Kyushu University as an Associate Professor. From 2011 to 2018, he was with Kyoto University as an Associate Professor in the Department of Communications and Computer Engineering. In October 2018, he joined Nagoya University where he is currently a Professor in the Department of Computing and Software Systems. His research interests include low power design and methodologies for embedded systems.

Hidetoshi Onodera received the B.E., M.E., and Dr. Eng. degrees in Electronic Engineering from Kyoto University, Kyoto, Japan, in 1978, 1980, and 1984, respectively. He joined the Department of Electronics, Kyoto University, in 1983, and currently a Professor in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University. His research interests include design technologies for Digital, Analog, and RF LSIs, with particular emphasis on low-power design, design for manufacturability, and design for dependability. Dr. Onodera served as the Program Chair and General Chair of ICCAD and ASP-DAC. He was the Chairman of the IPSJ SIG-SLDM (System LSI Design Methodology), the IEICE Technical Group on VLSI Design Technologies, the IEEE SSCS Kansai Chapter, and the IEEE CASS Kansai Chapter. He has served as the Editor-in-Chief of IEICE Transactions on Electronics and IPSJ Transactions on System LSI Design Methodology. He is an IEEE Fellow, an IEICE Fellow, and a Member of Science Council of Japan.

Akihiko Shinya received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tokushima University in 1994, 1996, and 1999, respectively. He joined NTT Basic reseach laboratories in 1999 and has been engaged in reseach on the photonic crystal nanodevices. He is a member of the Japan Society of Applied Physics (JSAP).

Masaya Notomi received B.E., M.E., Ph.D. degrees in applied physics from University of Tokyo in 1986, 1988, and 1997, respectively. After joined NTT laboratories in 1988, his research interest has been photonic nanostructures for novel devices. He is entitled as Senior Distinguished Scientist in NTT, a director of NTT Nanophotonics Center, heading Photonic Nanostructure Research Group in NTT Basic Research Laboratories, and a guest professor of physics in Tokyo Institute of Technology. He received IEEE/LEOS Distinguished Lecturer Award (2006), Japan Society for Promotion of Science Prize (2009), Japan Academy Medal (2009), and the Commendation by Japanese Minister of Education, Science and Technology (2010). IEEE Fellow since 2013.