Thesis for Doctor of Philosophy

Toward high performance of micro-LEDs via sidewall engineering for next-generation display

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Toward high performance of micro-LEDs via sidewall engineering for next-generation display

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Abstract

Because of the emerging demand for ultra-high pixel per inch (PPI) display which will play a key role in augmented reality (AR) / virtual reality (VR) applications, called near-eye display, III−nitride based micro-light emitting diodes (μLEDs) that can realize small pixel are attracting strong attention. For the fabrication of μLEDs arrays, top-down process by shaping each pixel with inductive coupled plasma reactive ion etching (ICP-RIE) allows us to realize ultra-small pixel (typically $< 10 \times 10$ μm^2). ICP-RIE dose not seriously degrade the performance of traditional large size LEDs ($> 300 \times 300$ μm^2). However, it makes μLEDs to encounter the sidewall damage, which becomes more and more serious as μLEDs size shrinks, thus leading low external quantum efficiency (EQE). Decreasing EQE with shrinking pixel size makes it difficult to realize high performance and high PPI of μLED display. In this thesis, the influence of sidewall conditions on the performance of μLEDs is systematically investigated. In addition, I propose the solutions how to overcome lowering EQE of μLEDs with shrinking size in this thesis.

Because the sidewall is formed by ICP-RIE etching, the dry etching conditions of ICP-RIE was most important and thus investigated. With high-bias power etching condition, an ion-bombardment is dominant, which makes the plasma induced damage on the etched surface including sidewall. However, it was reported that chemical reaction between Cl_2 etching gas and GaN layer is dominant under low-bias power etching. This chemical reaction not only suppressed the plasma induced damage but also improved the leakage current and ideality factor that are indirectly related to Shockley-Read-Hall (SRH) non-radiative recombination. Moreover, chemical reactions created the rough sidewall through dislocations, increasing the light extraction efficiency via sidewall. Therefore, the LED pixel made by the low etching bias shows high EQE than the LED pixel made by high

etching bias. Given that etching by low-bias power is dominantly chemical reactions in ICP-RIE system, it is suitable for realizing high performance μLED and fabricating ultra-small μLED via less etching damage.

For better luminous efficiency, current display system uses various pixel designs such as circular, square, and stripe. Regarding such demand in the display system, variously designed III−nitride μLEDs were quantitatively investigated in this work. Although the mesa size is fixed, the peripheral length can be controlled depending on the μLED design. To clarify the relationship between the peripheral length and sidewall damage, the current density at peak EQE (J_{peak}) was investigated. J_{peak} offered the information of SRH non-radiative recombination since J_{peak} is proportional to it. It was quantitatively confirmed that if the peripheral length of the pixel becomes longer, the J_{peak} and SRH non-radiative recombination rate becomes higher. Usually, LEDs having high SRH non-radiative recombination rate shows low EQE. However, in this experiment, LED having the longest peripheral length showed the highest EQE; This behavior was further investigated by separately analyzing IQE and light extraction efficiency. Undoubtedly, IQE decreased with increasing the peripheral length. On the other hand, light extraction efficiency increased with increasing the peripheral length. This behavior is attributed to the fact that light extraction occurs not only from the top and the bottom but also to the sidewall, indicating that sidewall light emission increased total light extraction efficiency. Consequently, increasing light extraction efficiency not only compensates decreasing IQE but also increases peak EQE. Furthermore, it was confirmed that tetramethylammonium hydroxide (TMAH) treatment removed the lattice distortion that was observed by transmission electron microscopy at the sidewall. Correspondingly, the surface recombination rate is reduced by reducing carrier trap site that is part of SRH non-radiative recombination center, which improved peak EQE.

By systematically and quantitatively investigating the sidewall condition, this thesis guides the pathway how to realize high performance μLED for next-generation display.

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Chapter 1

Introduction

1.1 History of III−nitride

There were attempts of fundamental research for properties of gallium nitride (GaN) by several researchers before 1980s. Maruska et al. firstly demonstrated that GaN has a direct energy bandgap of 3.39 eV in 1969 [1]. Pankove et al. showed that GaN electroluminescence of 2.6 eV by Zn-doped GaN layer in 1971 [2]. Monemar et al. explained the fundamental energy gap of GaN by photoluminescence excitation spectra in 1974 [3]. Although aforementioned studies demonstrated that GaN is one of the candidates for optoelectronic device, lack of GaN growth techniques led that the researcher withdrew the research of GaN. Hopefully, in 1986, Amano et al. invented high crystal quality and transparent GaN using low temperature AlN buffer layer by metal organic vapor-phase epitaxy (MOVPE) shown in **Figure 1.1**a [4]. Additionally, they world firstly demonstrated Mg-doped p-type GaN by using low-energy electron beam irradiation (LEEBI) and showed the UV emission with holes injection into the undoped n-GaN film shown in Figure 1.1b [5]. Their work opened up the possibility of applying III−nitride materials to light source. Following them, Nakamura et al. reported GaN buffer layer on sapphire substrate which can lead to not only high quality GaN layer but also better hall mobility of n-type GaN [6]. In addition, they found that hydrogen (H^+) is the source of passivation of as-grown Mg-doped GaN and demonstrated that over 700 ºC annealing is a solution for activating p-GaN layer by removing H^+ in 1992 shown in Figure 1.1c [7]. A few years later, they further demonstrated that blue light emission at 450 nm wavelength by InGaN/AlGaN double heterostructure [8]. Important findings

for GaN were made in the late 80s and early 90s, and GaN related reports began to rapidly increase afterwards as shown in Figure 1.1d [9]. And naturally, the flow of compound semiconductor research moved from ZnSe to GaN, which reflected the excellent performance of GaN such as toughness, wide and direct bandgap, and non-toxicity [9]. As the fundamental research is continuously conducted, nitride semiconductors and their devices with excellent performances are being studied steadily and applied in various fields, such as LEDs, power devices, etc.

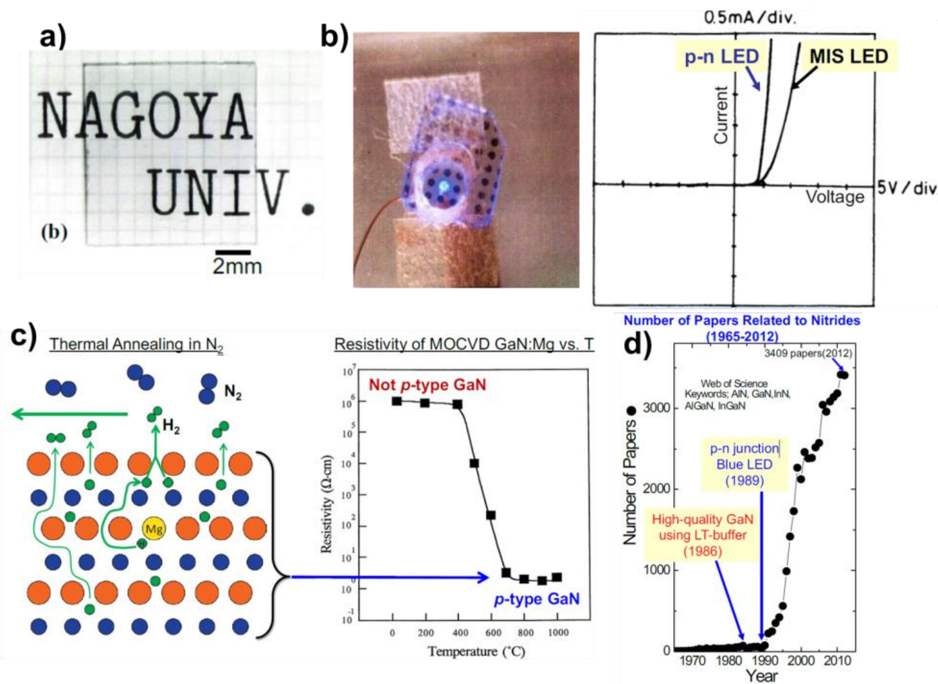


Figure 1.1. Introduction of III−nitride materials history. a) World first invented single crystal and transparent GaN by low temperature AlN buffer layer. b) UV emitted GaN p-n diode via LEEBI technique. c) Thermal annealing for activating p-type GaN layer. d) Number of papers related to the III−nitride. Since 1990s, it rapidly increased [9].

1.2 Properties of III−nitride semiconductor

III−nitride is a compound semiconductor based on the group III element such as Aluminum (Al), Gallium (Ga), and Indium (In), with nitrogen as the group V element. The alloy system between group III elements and nitrogen makes various structures such as zinc blende, rock-salt, and wurtzite structure. A stable crystal structure of hexagonal close-packed wurtzite can be obtained under proper growth conditions. Based on this alloy system, III−nitrides have many outstanding properties for optoelectronic devices. The properties of several optical semiconductors are compared in **Table 1.1**. Relatively high electron mobility, thermal conductivity, relatively low refractive index can guarantee III−nitride GaN material is more suitable for light emitting diodes (LEDs) compared to II-VI and III-V direct bandgap materials. More importantly, III−nitride can fully cover not only visible range (380 ~ 750 nm), but also ultraviolet (< 380 nm) and infrared (> 750 nm) range by alloying AlN and InN with GaN ($Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$) [10] as described in **Figure 1.2.** The bandgap of organic light emitting didoes (OLEDs) is also tunable by controlling the conjugation length, which also allows the emission of visible light; however, electron mobility and thermal conductivity are extremely low compared to III−nitride [11-12] (The weakness of OLEDs will be explained in chapter 1.3, and 1.4). Therefore, III−nitride based light source is suitable and replaceable light source for next-generation display system.

Table 1.1. Comparison of properties of various optical semiconductors.

	Alq_3 (OLED)	ZnSe (II-VI)	InP (III-V)	GaN (III-N)
Bandgap (eV)	Tunable	2.71	1.344	3.4
Electron mobility($cm^2 V^{-1} S^{-1}$)	10^{-6}	600	5400	900
Thermal conductivity ($W\ cm^{-1} K^{-1}$)	0.00107	0.18	0.68	1.3
Refractive index (400 – 700 nm)	1.8-1.7	2.9-2.5	4.8-3.3	2.5-2.3

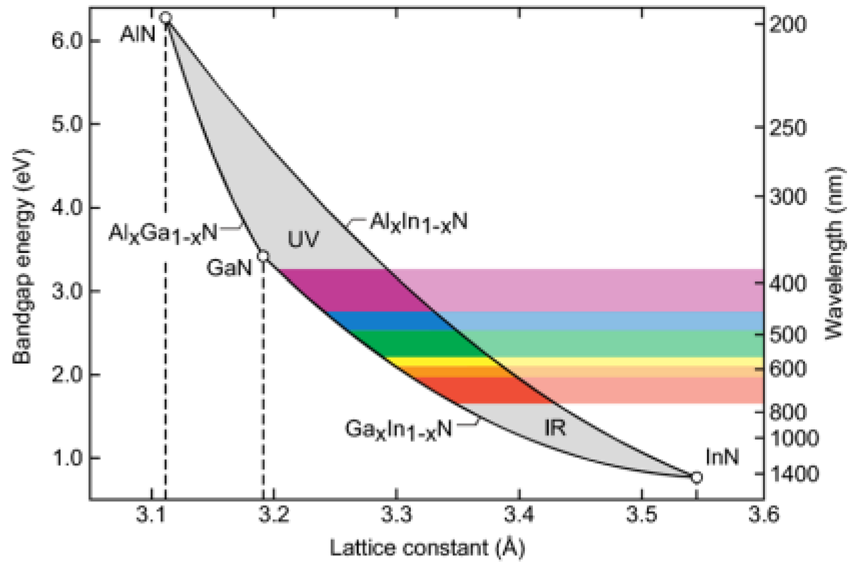


Figure 1.2. Bandgap energy and wavelength as a function of lattice constant in c-plane. By alloying AlN-GaN or InN-GaN, emitting wavelength can be controllable in theory from UV to IR [10].

1.3 The history of display technology

The display technology has come a long way and it is still evolving. The display technology plays an important role in human life, which allows us to approach substantial information and human can see what is happening in the world through the display. A cathode-ray tube (CRT), which is first display technology, was invented since 1897 [13] and occupied display market by the 1990s. Basically, CRT consists of electron gun including cathode, anode and control grid. Since the electron from electron gun is accelerated by anode voltage and its speed is approximately 10% of the speed of light, CRT can have fast response time. However, cathode and control grid should be set in an ultra-high vacuum atmosphere to create the image with electron moving. To keep ultra-high vacuum with safety, anode and control grid should be made by strong and thick glass, which leads heavy and bulky display. In addition, electron guns require high power consumption, leading to a waste of energy. Hence, since 1990s, liquid crystal display (LCD) had been attracting attention and led the display market until 2010. LCD basically operates with liquid crystal that controls the light emission from back light unit to front plane. Because liquid crystal can be controlled by thin film transistor (TFT), thus forming the active-matrix display, which brought high resolution and high-quality images on the display screen. However, back light unit still makes thick panel including color filter and limits application field due to inflexibility. Furthermore, the low contrast ratio due to the liquid crystal remains critically a hurdle to realize perfect white and black. Meanwhile, organic light-emitting diode (OLEDs), which was firstly invented in 1987 [14], have grown rapidly by display companies. Unlike LCD, OLEDs is self-emissive display through electron and hole recombination in the emission layer, meaning that it does not require back light unit and can approach an infinite contrast ratio in theory. Because of their superior properties, OLEDs display technology is widely used in human life such as large screen TVs, smartphones,

and laptops. However, OLEDs is basically composed of organic materials, so it has disadvantages that its properties are not excellent. For example, burn-in, leaving an afterimage when used for a long time, perfect encapsulation because vulnerable to moisture, difficulty of ultra-high resolution due to limitations in the emission layer deposition method, and short lifetime, which all remain as the hurdle. The drawbacks of previous displays are described in **Figure 1.3**. Therefore, another light source that can overcome the drawbacks of pervious displays should be invented. One of the candidates that can displace a current display technology is III−nitride based micro-LEDs display.

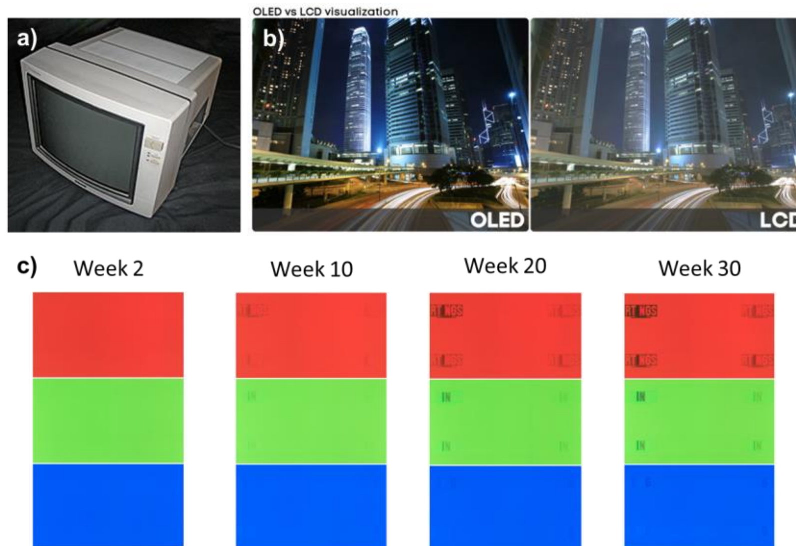


Figure 1.3. Disadvantage of past displays. a) Heavy and bulky CRT monitor. It shows CRT is not suitable for next generation display of thin and light. b) Revealing low contrast ratio of LCD display due to the liquid crystal system. Typically, contrast ratio of LCD is around 1000; however, self-emitting display such as OLEDs and micro-LEDs have contrast ratio of infinity in theory. c) OLEDs LG B6 TV burn-in test. As OLEDs display turn on time increases the image quality becomes bad due to the short lifespan of OLEDs [15].

1.4 III−nitride micro-LEDs: Importance and issues

Since 1962, III–V compounds light emitting diodes (LEDs) have been demonstrated their outstanding properties and developed by many researchers. In turn, the world is now becoming brighter via this technology. [16-17] With developing III–V compounds' LEDs, currently, the mankind is now seeing artificially made all visible color, which opened a chance we share substantial information via display. As display technology has been evolved, the requirements such as high pixel per inch (PPI), long lifetime, and stability gradually become increasing for better performance. Compared with previous display technologies such as LCD and OLEDs, III−nitride micro-LEDs display have excellent physical and material properties as described in **Figure 1.4**, which can overcome the problems of current display and lead to realize next-generation display [18-20]. Below is summery of advantages of micro-LEDs.

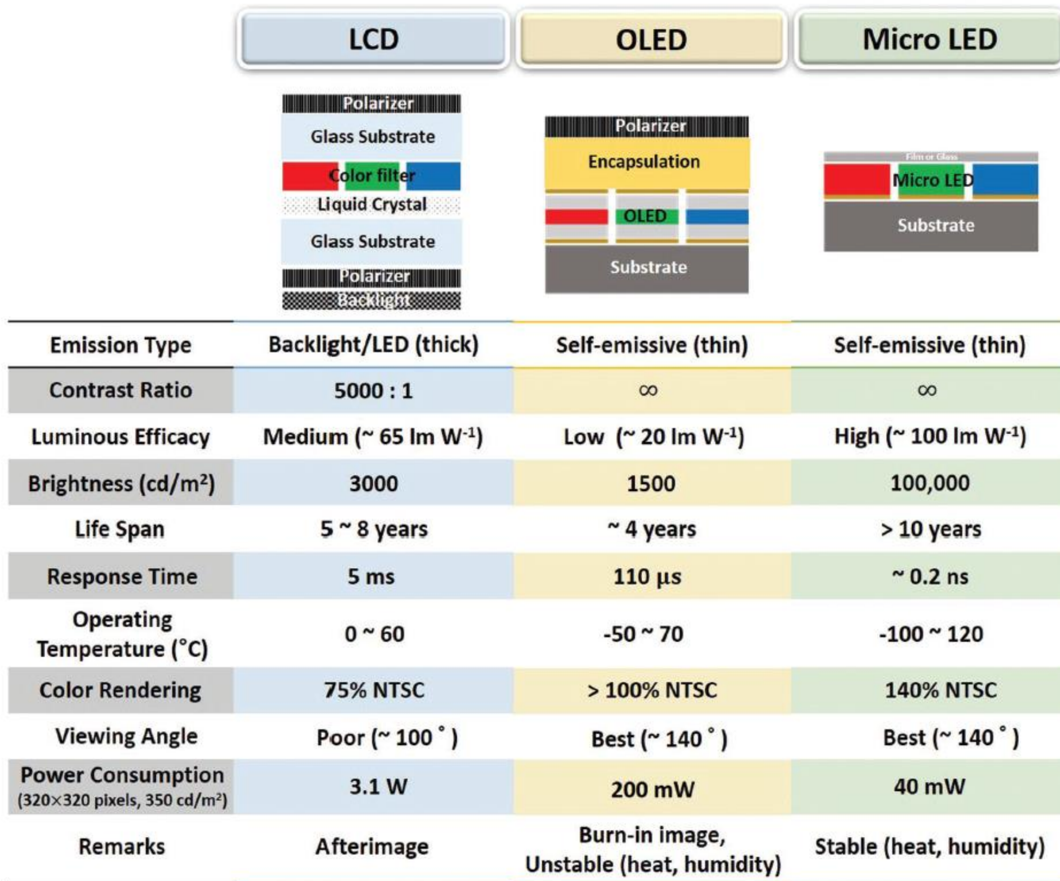
-Self-emissive: Compared to LCD, micro-LEDs are self-emissive, leading the back light free, ultra-thin display, and infinity contrast ratio (perfect black). Typically, LCD has the contrast ratio of 1000.

-Lifetime: Because micro-LEDs are based on the nitride semiconductor, it is very stable on any place even moisture and high and low temperatures thereby it has long lifetime, which is comparable to OLEDs technology.

-Stability: Because OLEDs are based on the organic material, it is very weak and sensitive in a water, oxygen, and temperature change. However, III–V based micro-LEDs are stable under the harsh conditions and thus not required perfect encapsulation process.

-Response time: Since micro-LEDs have crystal structure, the mobility of micro-LEDs is higher than OLEDs at least 10^4 times, which enhances the response time.

-High resolution: Since high PPI (> 2000 PPI) is required for near eye display such as argument reality (AR) and virtual reality (VR), micro-LEDs is suitable for next generation displays because it can be controlled in a very small size even less than 10 μm unlike OLEDs.



	LCD	OLED	Micro LED
Emission Type	Backlight/LED (thick)	Self-emissive (thin)	Self-emissive (thin)
Contrast Ratio	5000 : 1	∞	∞
Luminous Efficacy	Medium (~ 65 lm W^{-1})	Low (~ 20 lm W^{-1})	High (~ 100 lm W^{-1})
Brightness (cd/m^2)	3000	1500	100,000
Life Span	5 ~ 8 years	~ 4 years	> 10 years
Response Time	5 ms	110 μs	~ 0.2 ns
Operating Temperature (°C)	0 ~ 60	-50 ~ 70	-100 ~ 120
Color Rendering	75% NTSC	> 100% NTSC	140% NTSC
Viewing Angle	Poor (~ 100˚)	Best (~ 140˚)	Best (~ 140˚)
Power Consumption (320×320 pixels, 350 cd/m^2)	3.1 W	200 mW	40 mW
Remarks	Afterimage	Burn-in image, Unstable (heat, humidity)	Stable (heat, humidity)

Figure 1.4. Comparison of current display technology (LCD and OLEDs) and upcoming display technology (Micro-LEDs). [18]

Current display technologies, such as smartphone, have less than 500 PPI. However, as displays become closer to the human eye such as VR and AR called near eye display, high PPI (> 2000 PPI) display technology is required. If the distance between the display and eye becomes too far, the eye cannot distinguish high resolution. **Figure 1.5**a shows the relationship between viewing distance and pixel density [21]. As viewing distance decreases (i.e., closed to eye), the high PPI is essential, meaning that ultra-small pixel for ultra-high PPI is key point to realize next generation display [22]. It is already demonstrated that OLEDs technology has better performance than LCD such as contrast ratio and color reproduction. However, OLEDs are not suitable for ultra-high PPI due to the deposition of organic layer. As shown in Figure 1.5b, a fine metal mask (FMM) is used to create OLEDs pixel. In the FMM process, unintended shadow area also proceeds due to the fine oscillation of shadow mask, which makes it difficult for the OLEDs to realize high PPI display [23-25]. In this regard, III−nitride based micro-LEDs display is further attracting attention due to good controllability of pixel size by ICP-RIE. For example, Smith et al. demonstrated 1 μm diameter blue and green III−nitride micro-LEDs using ICP-RIE process, which would translate to around 20,000 PPI as shown in **Figure1.6** [26-27]. Particularly, this result suggests that III−nitride based micro-LEDs is suitable for ultra-high PPI display accompanying excellent physical and material properties.

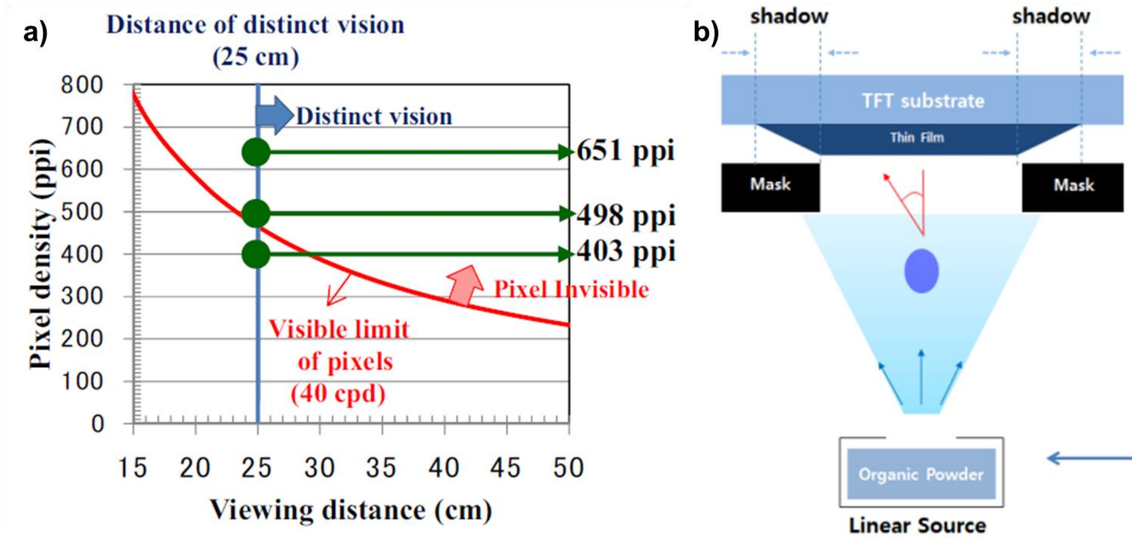


Figure 1.5. a) Pixel density verse viewing distance. As distance becomes small, high PPI is required [21]. b) The problem of OLEDs FMM process. Because of shadow effect, it is difficult to reach high PPI OLEDs display [23].

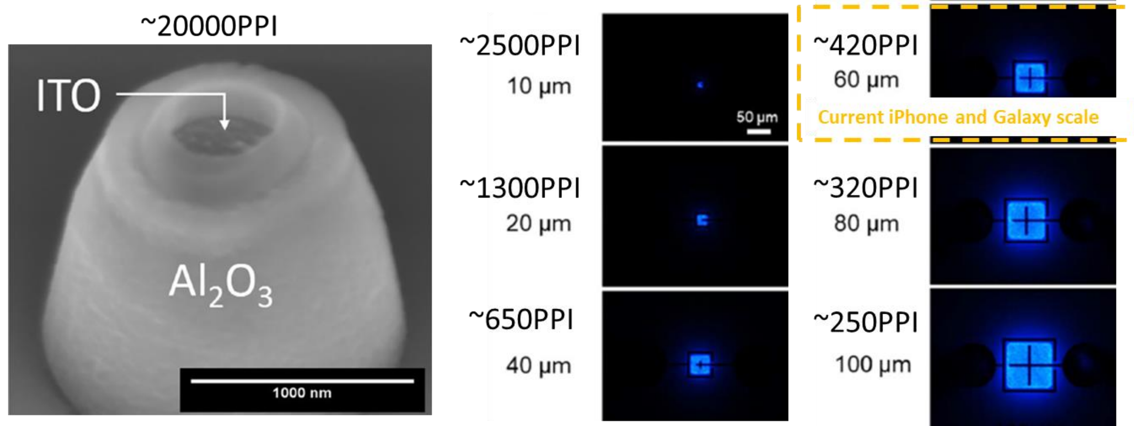


Figure 1.6. Showing the easily controllable micro-LEDs size. Small-sized LEDs are essential due to requiring high PPI display [26-27].

Typically, traditional III–V LEDs (e.g., > 300 × 300 μm^2) have high external quantum efficiency (EQE) than OLEDs. However, as LED size goes down to a few μm scale, EQE of LED significantly decreases as shown in **Figure 1.7**a due to increasing Shockley-Read-Hall (SRH) non-radiative recombination (Figure 1.7b) [28-29]. This serious decreasing of EQE is mainly caused by a top-down process via plasma induced ICP-RIE that creates a damaged surface including dangling bond. The dangling bond (or surface disorder) occurs approximately a few nm widths at the sidewall. However, it needs to be considered the carrier diffusion length. For example, David et al. found that most of the generated carriers move within a few micrometers [30]. Finot et al. reported that the carrier lifetime starts to decrease 1 μm away from the sidewall [31]. Boussadi et al. also showed that the carrier lifetime decreased over a range of several micrometers [32]. Therefore, ICR-RIE induced sidewall damage makes the surface disorder, which provides the carrier recombination as non-radiatively due to the carrier diffusion. Recently, Park et al. found that J_{peak} (current density at peak EQE) that is proportional to SRH non-radiative recombination increases with increasing the peripheral length of mesa [33]. This result further suggests that the exposed damage area at the sidewall mainly decides the SRH non-radiative recombination, therefore, the damage at the sidewall should be suppressed to realize high performance micro-LEDs.

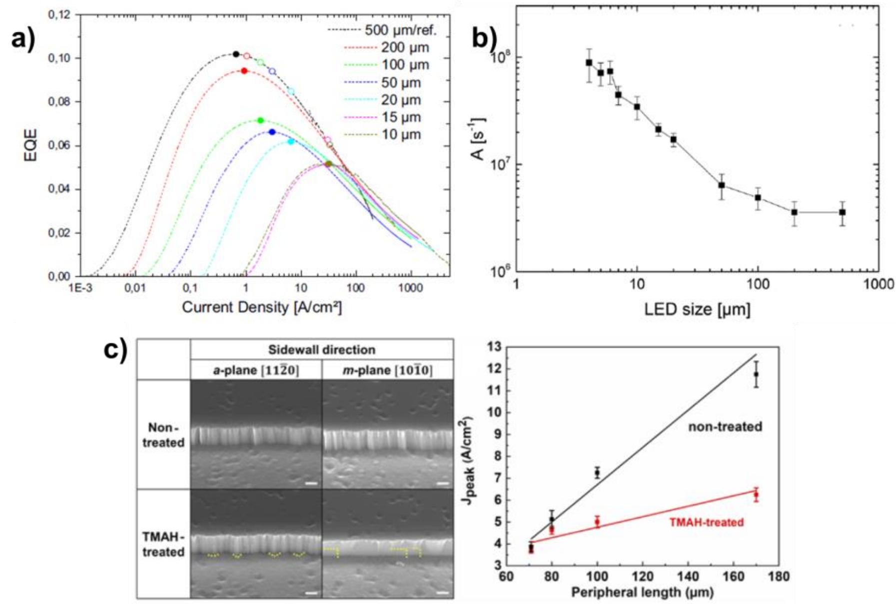


Figure 1.7. a) Size dependent EQE behavior of blue micro-LEDs [28]. b) Increasing SRH non-radiative recombination with decreasing LED size, leading low EQEs [29]. c) J_{peak} as a function of the peripheral length of micro-LEDs mesa [33].

Meanwhile, operation current density for display is different depending on the display type such as TV (relatively large screen), smart phone, VR, and AR as described in **Figure 1.8a**, which is related to the brightness. For example, smartphone requires 1000 Cd/m^2 corresponding to a few A/cm^2. AR micro-LED displays requires 10,000 Cd/m^2 corresponding to a few ten A/cm^2 for typical blue LED; the operation current density can be different depending on the emission color due to the luminous efficiency as shown in Figure 1.8b [34-36].

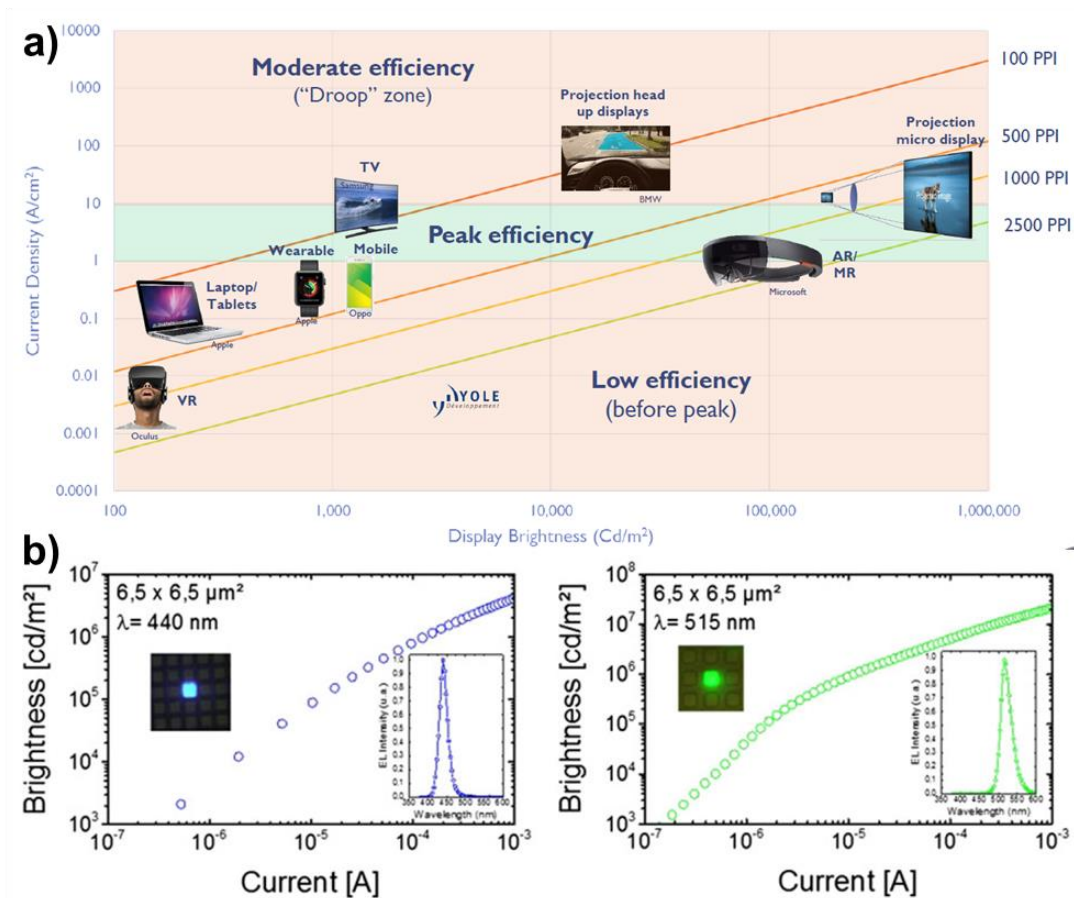
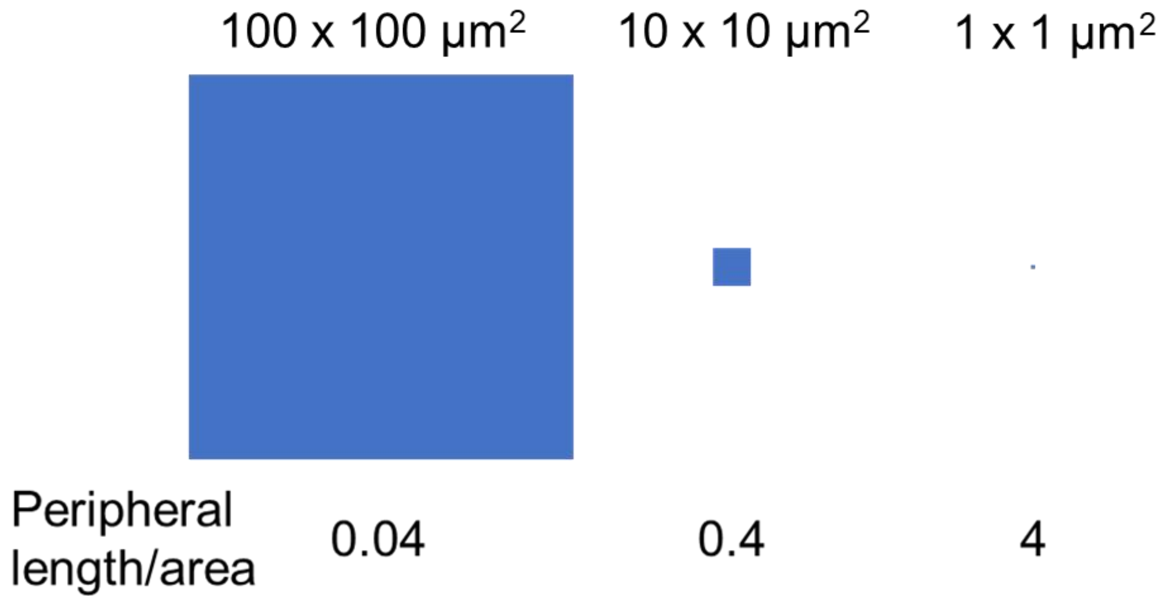


Figure 1.8. a) Requiring brightness for etch display type. [35]. b) 6.5 x 6.5 µm^2 scale micro-LED brightness [36].

Regarding VR micro-LED display, since it operates in the dark space, does not require high brightness. However, high PPI is needed because VR and AR operate close to the human eye. Typically, J_{peak} of micro-LED varies from 0.1 to a few ten A/cm^2 depending on the size as shown in Figure 1.7a. Ideally, the display should operate at J_{peak} for the highest efficiency. However, as discussed above, requiring the brightness is different by display type, which means that operation current density is different. Therefore, it needs to be developed that the micro-LED has high

efficiency at the low current density region. Such low current density region is directly related to the SRH non-radiative recombination, surface recombination.

Although the top-down process allows reaching ultra-small pixel and ultra-high PPI, the encountering decreasing EQE should be overcome to realize high performance and high PPI micro-LEDs display. Because III–V materials are rigid and chemically stable, use of high energy induced etching process (e.g., plasma) for micro-LEDs fabrication is inevitable. The etched surface exposed by plasma, especially called sidewall damage, critically increases SRH non-radiative recombination rate accompanying surface recombination resulting in decreasing EQE of micro-LEDs [37-38]. In case of conventional LEDs, the surface recombination is not critical because the ratio of peripheral length and area is negligibly small. However, as LED size enters a few µm scale (i.e., decreasing area), the ratio of peripheral length and area dramatically increases as described in **Figure 1.9**, which increases the ratio of surface recombination velocity (SRV) resulting in decreasing IQE because IQE is inversely proportional to the SRH non-radiative recombination that includes SRV [39-40]. Since SRV is related to the band bending at the sidewall, although the sidewall damage depth (i.e., surface disorder, even a few nm scale) is small, the carriers move into the sidewall damaged area and recombine as non-radiatively.



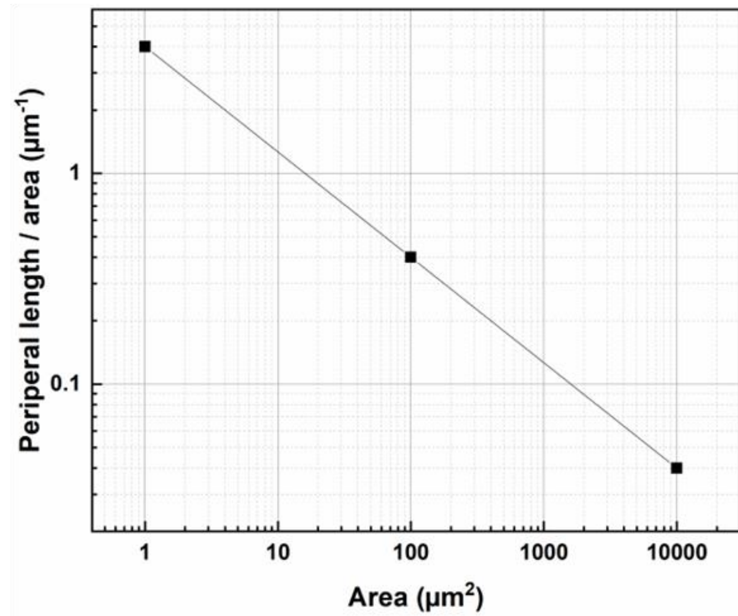


Figure 1.9. The ratio of peripheral length and area. As size decreases, the ratio increases, which leads to high SRV because SRV directly proportional to the ratio of peripheral length and area.

As discussed above, increasing SRV is a critical issue on the performance of micro-LEDs. Since SRV is not critical to large size LEDs, therefore, still not many solutions have been reported yet.

After spotlight micro-LEDs recently, the several methods to solve the decrease in EQE have been reported in recent five years. A familiar method is to cover the sidewall with SiO_2 or Al_2O_3 using plasma free atomic layer deposition (ALD), which concept firstly was invented by Wong et al. [41-42]. They showed that ALD passivation process effectively improves EQE of blue-micro-LEDs (< 20 μm scale) caused by the suppressed SRH non-radiative recombination, which was further supported by leakage current and ideality factor. Traditional method such as chemical treatment is good solution by removing surface defects [43-44]. Jung et al. reported that HF chemical treatment effectively removed the sidewall defect resulting in improving EQE [45]. Although both methods care the sidewall damage, it may not perfectly remove the sidewall damage because the sidewall surface state decides the band bending, if the sidewall surface is not perfect likes bulk, the band bending should occur, which is points the carriers recombine as non-radiatively. Therefore, it could be concluded that both methods can alleviate the sidewall damage; however, it does not remove the sidewall damage perfectly. The remained the sidewall damage (i.e., disorder or defect) will be the non-radiative point defects because the carrier diffusion length is usually over 1 μm [31].

The solution attaining high EQE of micro-LEDs is enhancing the light extraction efficiency. Because EQE is a production of IQE and light extraction efficiency, it is important to improve both. Where IQE of micro-LEDs is mainly decided by SRV while light extraction efficiency is independent parameter from SRV, the sidewall damage [38-40]. Ley et al. recently investigated that peak EQE increases even though the micro-LED size shrinks, namely, high SRV, which is caused by the enhancing light extraction efficiency with decreasing size [46]. This result suggests that the light extraction efficiency takes a large portion of the EQE as LED size decreases.

Therefore, enhancing the light extraction efficiency may be more effective to enhance EQE, which compensates decreasing IQE with decreasing size.

Another solution avoiding the sidewall damage leading low EQE is III–nitride nanoroad growth called the bottom-up method. Since the bottom-up does not require ICP-RIE etching, it can avoid the plasma induced sidewall damage. Moreover, nano scale pixel size can have several advantages such as high PPI and high light extraction efficiency. Although III–nitride nanoroad has many advantages and more competitive than top-down method, there are still some hurdles to overcome to apply to the micro-LED display. First, III–nitride bottom-up sufferers to the color mixing. Because of their growth mechanisms by MOVPE, the indium composition is different depending on the plane orientations [47-49]. For example, the indium composition at the top of nanoroad is higher than the side of nanorod, making it difficult to approach pure color emission. The growth mechanism of molecular beam epitaxy (MBE) differs from MOVPE, which allows the color purity of MBE grown nanoroad LED [50-51]. However, because of technical difficulty of MBE such as ultra-high vacuum process, it is not suitable candidate to apply to micro-LED display in terms of mass production. In addition, a nano-patterning process is required, which is more complicated than the top-down process. The bottom-up process by MOVPE is promising way to approach ultra-high PPI display in future; however, it should overcome the several drawbacks.

1.5 Thesis organization

As it is described in the last section, micro-LEDs are now encountering a trade-off between the PPI and the EQE. In this thesis, the reason why EQE decreases with shrinking size and how to overcome the problem of decreasing EQE are mainly focused and discussed.

Chapter 1 introduces the history of III–nitride semiconductor and display technology. Following current issues of display technology, it is described that why micro-LEDs display is necessary for realizing next generation display such as VR and AR, especially called "near-eye display". Moreover, what problem micro-LEDs encounters and how to overcome it are discussed.

Chapter 2 investigates the effect of ICP-RIE dry etching conditions on the surface state. The experimental results demonstrate that the etching mechanism changes from the physically to chemically as etching bias decreases. Especially, it was found that the 2.5 W bias etching is based on the chemical reaction between Cl_2 etching gas and GaN layer resulting in the roughen sidewall and etched surface.

Chapter 3 mainly discusses the influence of low bias etching on the performance of micro-LEDs. The lowest etching bias yielded lowest leakage current and ideality factor, which may indicate the less etching damage on the surface. Moreover, the lowest etching bias showed the highest EQE, which is caused by combined effect of suppressed sidewall damage and enhanced light extraction efficiency via the sidewall enginnering. Additionally, the strategy through thin quantum barrier for small wavelength shift and small efficiency droop is discussed.

Chapter 4 discusses the effect of micro-LEDs structure and figures out the interplay of sidewall damage and light extraction efficiency. It was found that IQE and light extraction efficiency of micro-LEDs depends on the peripheral length of micro-LEDs. Especially, IQE decreased with increasing the peripheral length but, light extraction efficiency increased; This increasing light

extraction efficiency compensated decreasing IQE. By introducing J_{peak}, the surface recombination rate will be discussed. Finally, it is concluded that the peripheral length of mesa critically affects the performance of micro-LEDs.

Chapter 5, finally, summarizes all results explained in this thesis and discuss how to overcome the crosstalk between the pixels.

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Chapter 2

Dry etching condition dependent GaN surface behavior

2.1 Introduction

Dry etching via inductively coupled plasma-reactive ion etching (ICP-RIE) is a key process for III−nitride (InN, GaN, and AlN) based devices such as light-emitting diodes (LEDs), high-electron-mobility transistor (HEMT), and power device [1-3]. As well described in **Figure 2.1**, ICP-RIE system is based on two power supply, ICP power and bias power. The ICP power strongly accelerates the electrons via high radio frequency (13.56 MHz rotating electric field) and creates the high plasma density. On the contrary, the bias power makes the ion-bombardment into the sample. Because ICP-RIE is based on the high plasma density, it allows to etch a chemically stable III−nitride materials. However, ion-bombardment caused by high bias power significantly induces the surface damage accompanying the surface disorder [4]. Particularly, in recent year, it was reported that the leakage current of n-GaN Schottky diode can increase after ICP-RIE etching because ICP-RIE makes the point defects related to nitrogen and gallium vacancies caused by bad atomic arrangements on the surface [5]. In addition, it was further discovered that high bias etching on ICP-RIE system makes a lot of nitrogen vacancies on the p-GaN surface due most likely to high ion energies at high bias; therefore, electric performance of p-GaN became poor after high bias etching [6]. Therefore, it is expected that if plasma induced etching damage is suppressed, the fabricated device will have best performance. Focusing on this issue, Samukawa et al. suggested that the top-down etching via neutral-beam etching (NBE) technique, which is a novel defect-free etching for III−nitride materials [7]. Because the placing carbon plate under the chamber, it helps

to yield the lowest sputtering and does not contaminate the device. As a result, the NBE process can suppress the defects on the surface. Therefore, it is concluded that the etching condition seriously affect the performance of III−nitride device.

In this chapter, we introduce the surface behavior with various etching bias power of ICP-RIE system for III−nitride dry etching. The effect of low bias power is systematically investigated. Compared with normal etching condition (i.e., high bias power), the low bias power shows not only suppressing etching damage but also creating rough surfaces even at the sidewall, which could lead to enhance light extraction efficiency of micro-LEDs.

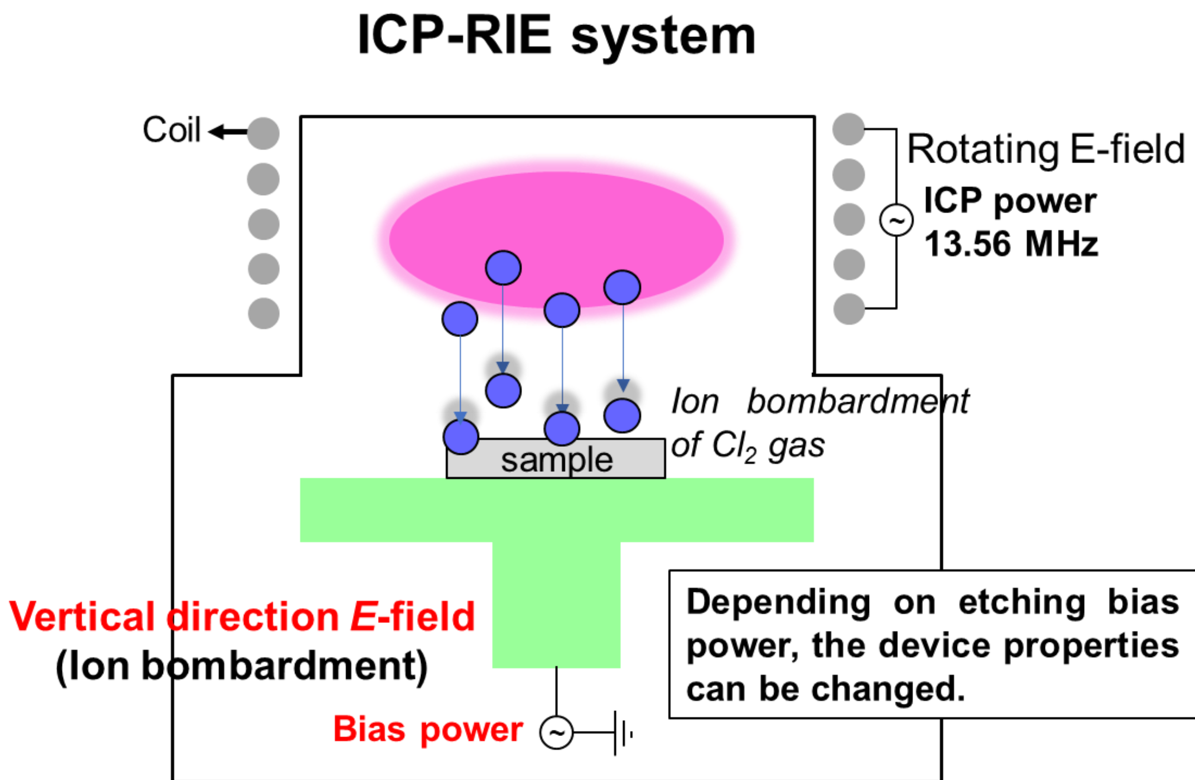


Figure 2.1. Schematic of ICP-RIE system. Most of III−Nitride material can be etched by Cl_2 gas.

2.2 Effect of etching bias power on the etched surface

Because the performance of micro-LEDs is affected by the sidewall damage, it is important to suppress the ICP-RIE etching induced-sidewall damage. One solution overcoming the plasma induced damage is to control the etching bias power. In this session, we confirm the effect of ICP-RIE etching bias power on the etched GaN surface. Consequently, we discuss the mechanism of the low etching bias and why the low etching bias power is chemical based etching in the next session. To investigate the effect of bias power on GaN surface, the thin GaN LED wafer was used. This wafer has 80 nm p-GaN, 50 nm p-AlGaN for electron blocking, 7 pairs InGaN/GaN multiple quantum well (MQW, total thickness 60 nm), and 1.3 μm n-GaN as described in **Figure 2.2**. Before evaluating the surface, the etching rate was investigated as shown in **Figure 2.3**, where the ICP power, Cl_2, and pressure were fixed to 150 W, 30 sccm, and 2.0 Pa. It was confirmed that as an etching bias power decreases, the etching rate also decreases. This decreasing etching rate is caused by the reduced ion-bombardment that is proportional to bias power. At a bias power of 1 W, there was no etching, thus, the minimum etching bias was 2.5 W to reduce the etching damage.

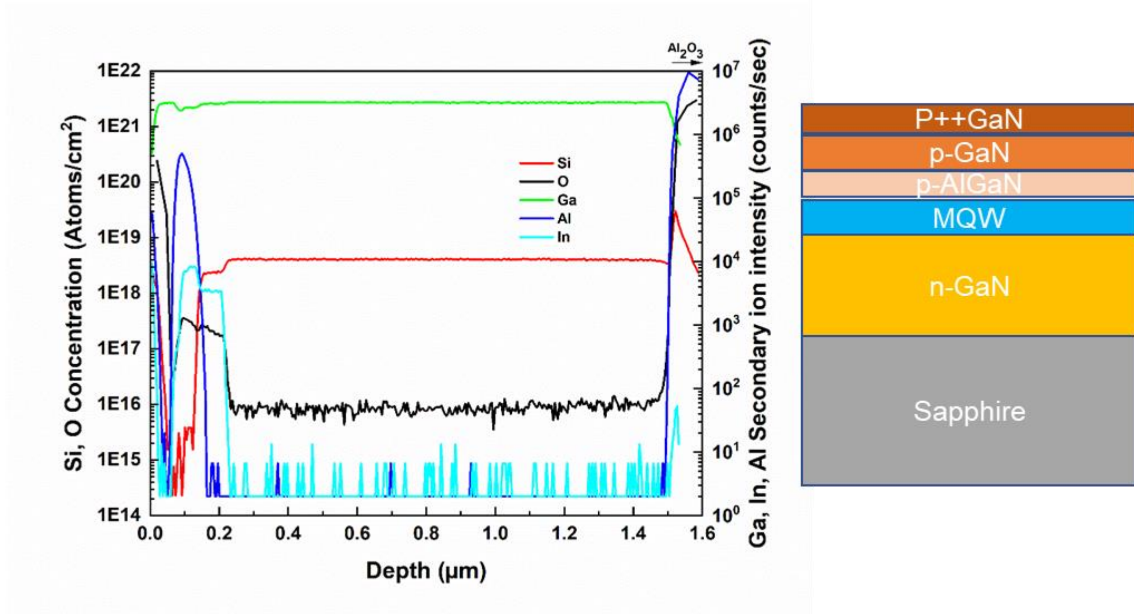


Figure 2.2. SIMS data for the epi wafer used in this study. The data indicate p-GaN, p-AlGaN, InGaN/GaN-based quantum well, n-GaN, and sapphire.

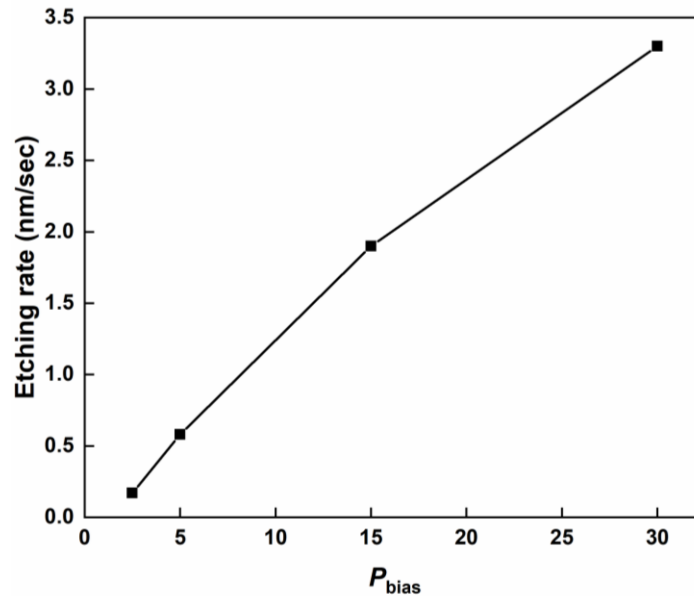


Figure 2.3. Bias power dependent etching rate, where ICP bias is fixed as 150 W**.**

Since we controlled the etching bias, it is speculated that the etched surface could be affected by the etching bias because ion bombardment depends on the etching bias [4-6]. To confirm the effect of etching bias on the etched surface, we observed the surface morphology by atomic force microscopy (AFM, NanoNavi IIs SII Nano-Technology). **Figure 2.4a** shows the revealed etched n-GaN surface with various bias power. The target etching depth was around 600 nm, meaning that the top of p-GaN, p-AlGaN, and MQW were fully etched. To evaluate the effect of bias power, 2.5 W, 5 W, 15 W, and 30 W were chosen. AFM images with a size of $5 \times 5\ \mu m^2$ were observed after etching. For the samples etched with 15 W and 30 W, the surface roughness (root mean square, RMS) was no significant differences, and both were quite smooth although the bias power was two times different. This result indicates that if the bias power increases more than a certain amount, it can be seen as dry etching based on the ion-bombardment. Interestingly, the surface roughness was very different under 5 W compared with 15 W and 30 W. This behavior can be attributed to ion-bombardment. The schematic in Figure 2.4 describes the effect of bias power on the etched surface. Basically, ICP-RIE is based on ion-bombardment with a vertical electrical field (e.g., bias power). Therefore, dry etching with ion-bombardment leads a smooth surface; however, as bias power becomes small, it turns to the chemical reaction between the etching gas and the devices. For example, Figure 2.4b shows the dramatically increasing the surface roughness when the ion-bombardment is insufficient under 5 W of bias power, the surface was very rough especially, 2.5 W showed 5.43 nm RMS roughness, which is comparable to the roughness of 30 W (0.7 nm).

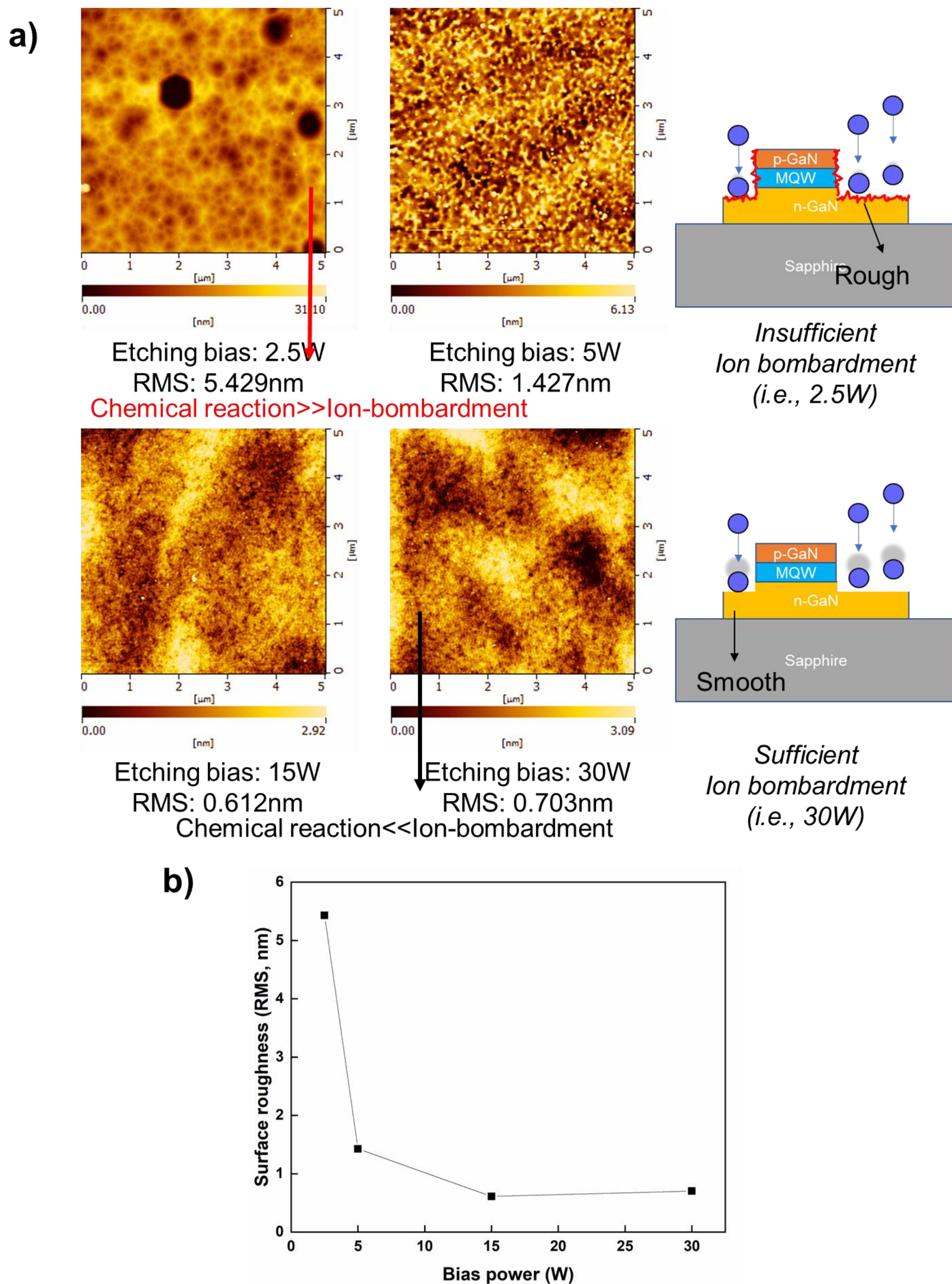


Figure 2.4. a) AFM images of the etched GaN LED surface. The surface roughs as the bias power decreases. b) the surface roughness (RMS) as a function of the etching bias power.

2.3 Chemical reaction between GaN and Cl2 etching gas

Meanwhile, Liu et al. reported that surface chemical reactions between the GaN and Cl radicals make a roughened surface than plasma etching [8]. **Figure 2.5** describes the various morphology states. After chlorine based radical expose, the surface became very rough compared with initial stage, which is quite similar to the 2.5 W etched surface as shown in Figure 2.4. This behavior could be occurred because of the chemical reaction between the GaN and the Cl radical. Thus, ion bombardment was not enough with 2.5 W of bias power due to low vertical electrical field. Rather, low bias power led to a chemical reaction between GaN and Cl_2 etching gas and thus the roughen surface on n-GaN was generated with low plasma damage.

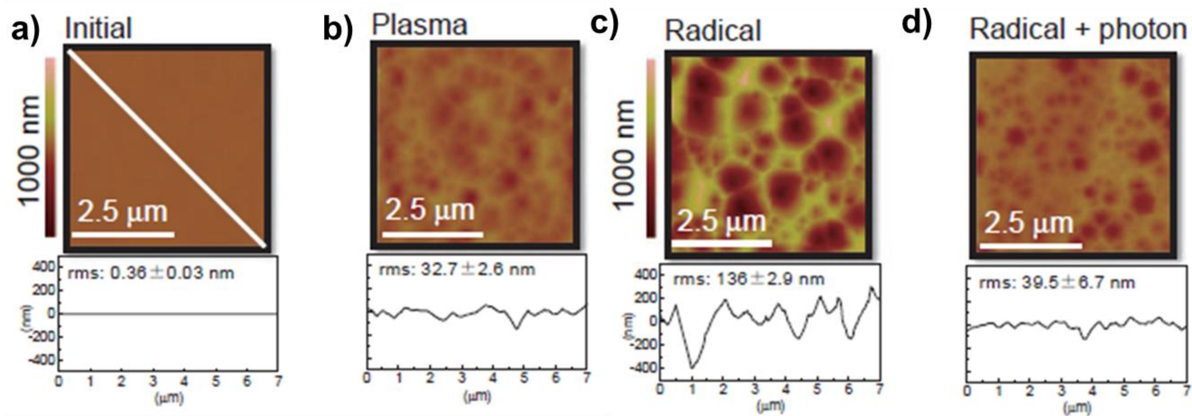


Figure 2.5. AFM images and line profiles of the GaN surface a) initial state, b) plasma etched, c) Chlorine based radical exposed, and d) after simultaneous irradiation of photons and radicals. [8]

Since the rough surface was observed after low bias power etching, the sidewall morphology should be further observed. To observe the sidewall morphology, scanning electron microscopy (SEM, SU-9000 Hitachi) was used. **Figure 2.6** shows the bias power dependent sidewall

morphology. Interestingly, above 15 W, the sidewalls were very smooth, which smoothness agreed well with the etched n-GaN surface shown in Figure 2.4, which is a result of the dominant ion-bombardment. However, as bias power becomes small, especially under 5 W, the sidewall morphology is roughing shown in Figure 2.6a.

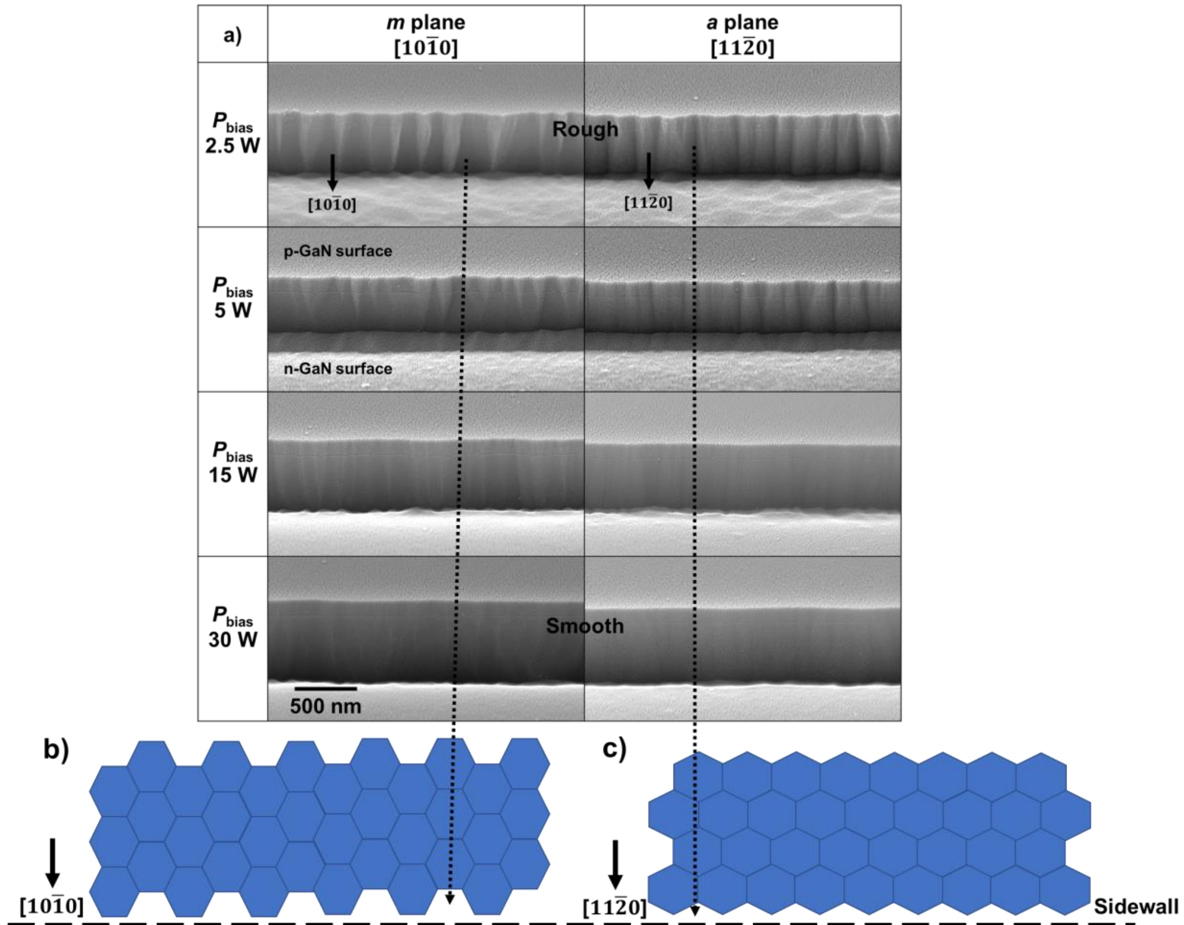


Figure 2.6. a) SEM images of the sidewall with various bias power and the sidewall direction.

Moreover, it was observed that the sidewall morphologies with low bias power were clearly different by the sidewall direction. For example, [10$\bar{1}$0] m-plane direction image is similar to the GaN hexagonal structure along with [10$\bar{1}$0] direction as described in Figure 2.6b. In addition,

$[11\bar{2}0]$ a-plane direction image is also similar to the $[11\bar{2}0]$ direction as described in Figure 2.6c. To verify that the effect of low bias power on the sidewall morphologies is found on other substrates, an additional GaN on sapphire was tested with same etching condition. (i.e., 2.5 W of bias power). **Figure 2.7** shows the sidewall and surface morphologies of GaN on sapphire after 2.5 W bias power. This observation is consistent with Figure 2.6a, which shows the roughen sidewall and surface after 2.5 W bias power. In Figure 2.7, it is further clearly shown that the sidewall morphology follows the hexagonal pit direction, which could be found on the etched surface as marked the write lines. When the GaN etched by low bias power, the surface was rough, and the sidewall morphology differed depending on the direction.

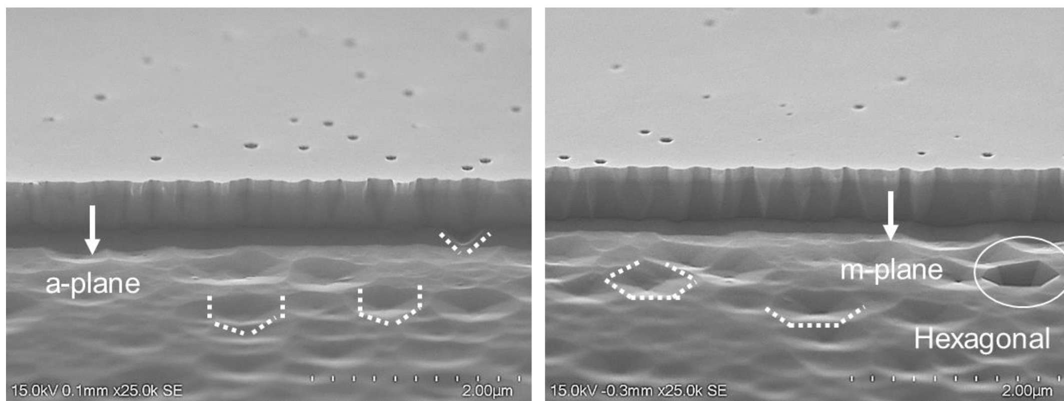


Figure 2.7. SEM images of the sidewall with bias power of 2.5 W and the sidewall direction. The white lines indicate a hexagonal of GaN.

Because the hexagonal pits were observed on the etched surface as shown in Figure 2.7, it is possible that the dislocation could react with the etching gas of Cl_2 chemically when 2.5 W of bias power is applied. To demonstrate the mechanism of a rough surface induced by the combine effect between 2.5 W bias power and the dislocation, the cathodoluminescence (Gatan MonoCL with

Hitach SEM S4300) under an acceleration voltage of 5 kV on the various substrates that has different dislocation density. For this, n-GaN substrate, undoped-GaN on sapphire, and GaN LED on sapphire (same as Figure 2.4) were etched with bias power of 2.5 W, where the ICP power, Cl_2, and pressure were fixed to 150 W, 30 sccm, and 2.0 Pa, respectively. **Table 2.1** shows the calculated dislocation density for each substrate via X-ray diffraction omega scans [9-11]. Where GaN LED on sapphire has quite high dislocation density, which is caused by no undoped GaN layer. The screw and edge dislocation density were calculated by Equation (1) and (2).

$$D_{screw} = \frac{\beta^2_{(002)}}{4.35 b^2_{screw}} \tag{1}$$

$$D_{edge} = \frac{\beta^2_{(102)} - \beta^2_{(002)} cos^2\varphi}{4.35 b^2_{edge} sin^2\varphi} \tag{2}$$

Where β is the FWHM of the XRD rocking curve, φ is the inclination angle of the (102) toward the (002) plane, and b is the Burgers vector length. b_{screw} is 0.5185 nm and b_{edge} is 0.3189 nm [11]. All dislocation density was calculated by the FWHM values of X-ray diffraction. **Figure 2.8** displays the SEM and panchromatic CL images. The panchromatic CL mode can figure out the dislocation density and position. All substrates were equally etched with same condition under bias power of 2.5 W for 3420 second. The etched n-GaN substrate surface was exceptionally smooth, unlike the other two samples. As marked yellow arrows, a few pits observed by SEM. Interestingly, the observed pits on n-GaN substrate were overlapped with the dark spots in the CL image, which indicates that the pits observed by SEM came from the dislocations.

Table 2.1. Dislocation densities of various substrates calculated by the FWHM values of X-ray diffraction omega scans [9-11].

	n-GaN substrate	GaN on sapphire	GaN LED on sapphire
Screw dislocation (cm^{-2})	5.36×10^6	1.06×10^8	7.59×10^5
FWHM (002)	51.70	230.08	19.44
Edge dislocation (cm^{-2})	5.01×10^6	4.90×10^8	2.35×10^9
FWHM (102)	36.72	288.3	582.5
Total dislocation (cm^{-2})	1.04×10^7	5.95×10^8	2.35×10^9

The dark spots were observed by CL image on the unetched area of undoped-GaN on sapphire resulting in the dislocations. However, it was observed that a lot of pits were on the etched surface of undoped-GaN on sapphire, and these were also overlapped with the dark spots of CL image, which agrees well the pits were from the dislocations. Therefore, these results confirm that bias power of 2.5 W reveals the dislocations via the chemical reaction. All of these observations indicate the evidence that the surface morphology is related to the dislocation. Further evidence can be found on GaN LED on sapphire sample. Because it has highest dislocation density (e.g., over $10^9 cm^{-2}$), the etched surface and sidewall were the roughest. In addition, substantial number of dark spots were observed by CL, which agrees well the surface roughing observed by SEM.

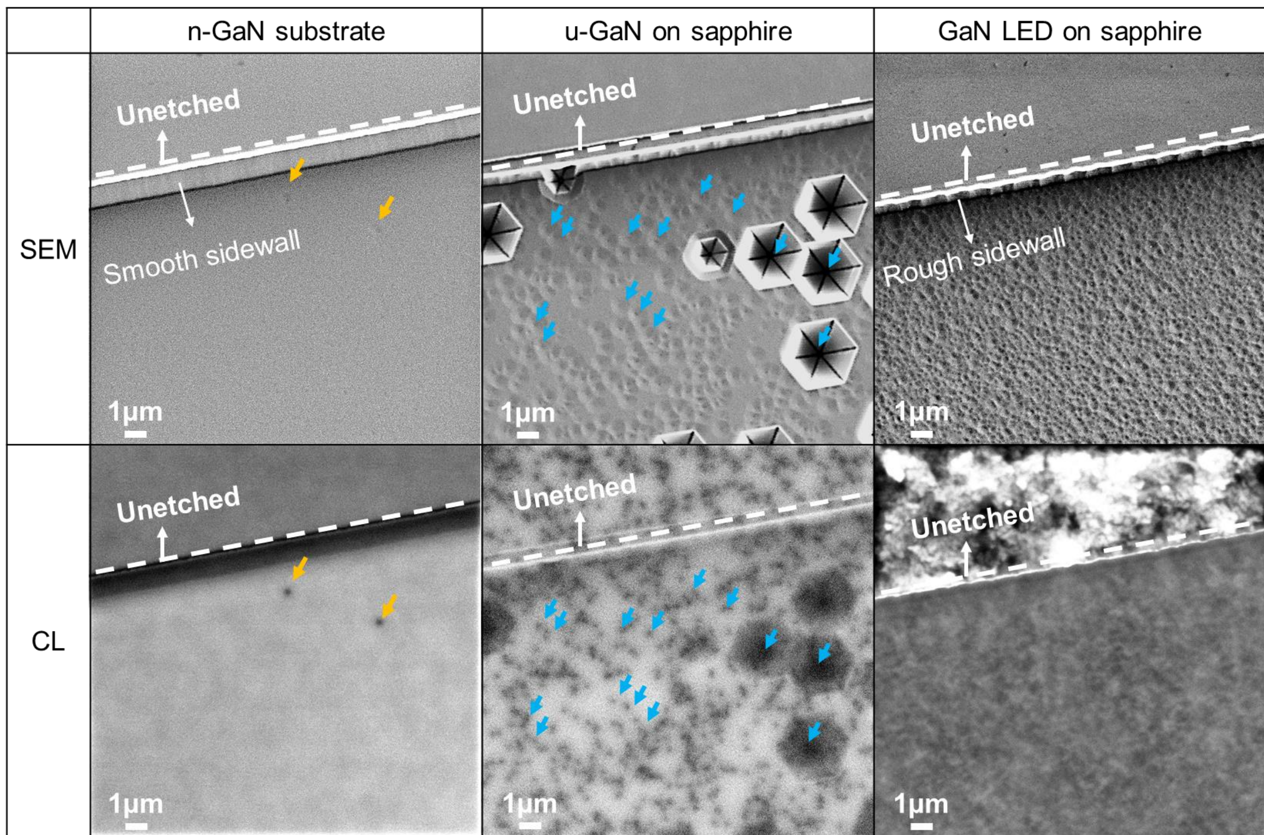
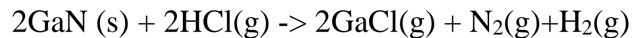


Figure 2.8. SEM and CL images of various substrates after etching process by bias power of 2.5 W. The revealed pits on the etched surface overlapped with CL dark spots.



Meanwhile, Hino et al. discovered that the hydrochloric acid (HCl) vapor-phase etching technique can reveal the dislocations on the epi surface via the chemical reaction between the HCl and GaN as below [12]:

$$2GaN (s) + 2HCl(g) \rightarrow 2GaCl(g) + N_2(g)+H_2(g)$$

Figure 2.9 shows the etched GaN surface after HCl etching technique. The observed surface morphology looks quite rough and there are many hexagonal pits on the surface, which seems the result of the revealed dislocation density via chemical reaction with chlorine.

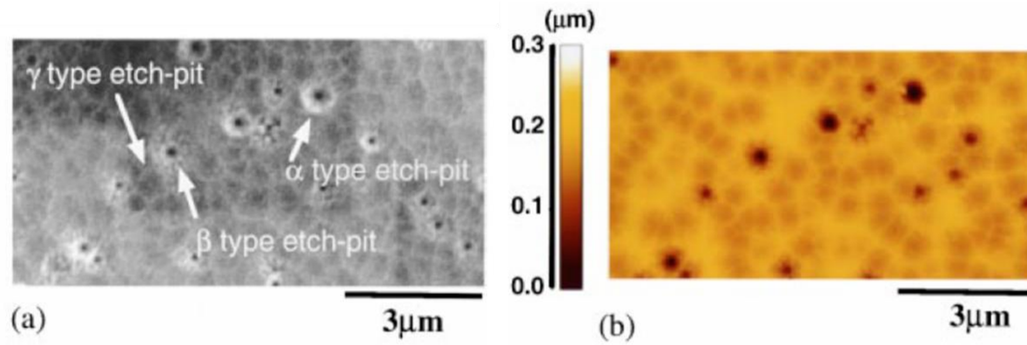


Figure 2.9. a) SEM image after HCl chemical reaction, and b) AFM image of the same area [12].

This roughness is quite similar to the etched surface by bias power of 2.5 W shown in Figure 2.4, which result supports that low bias power in ICP-RIE guarantees the chemical reaction between Cl_2 etching gas and GaN. The time-dependent etching by bias power of 2.5 W was further investigated. **Figure 2.10** shows the etched GaN surface for 1800, 3600, and 5400 seconds. All samples showed a lot of pits on the etched surface, which behavior is similar to the above discussed results. Although the etching time increased three times, only different thing was the pit size, indicating that the revealed pits were caused by chemical reactions between Cl_2 and GaN. Furthermore, the increasing pit size suggests that this bias power of 2.5 W should be based on the chemical reaction. Moreover, the various types of dislocations were observed shown in Figure 2.10. For example, black box, green box, and yellow box indicate edge dislocation, screw dislocation, and mixed dislocation, respectively [13]. Meanwhile, the smooth surface was observed by bias power of 30 W regardless of substrate types as shown in **Figure 2.11**. All etched surfaces looked quite smooth. For example, even though CL images display a lot of dark spots on GaN layer compared to Figure 2.10, the observed both substrate surfaces by SEM were smooth, indicating that there was no chemical reaction revealing dislocation.

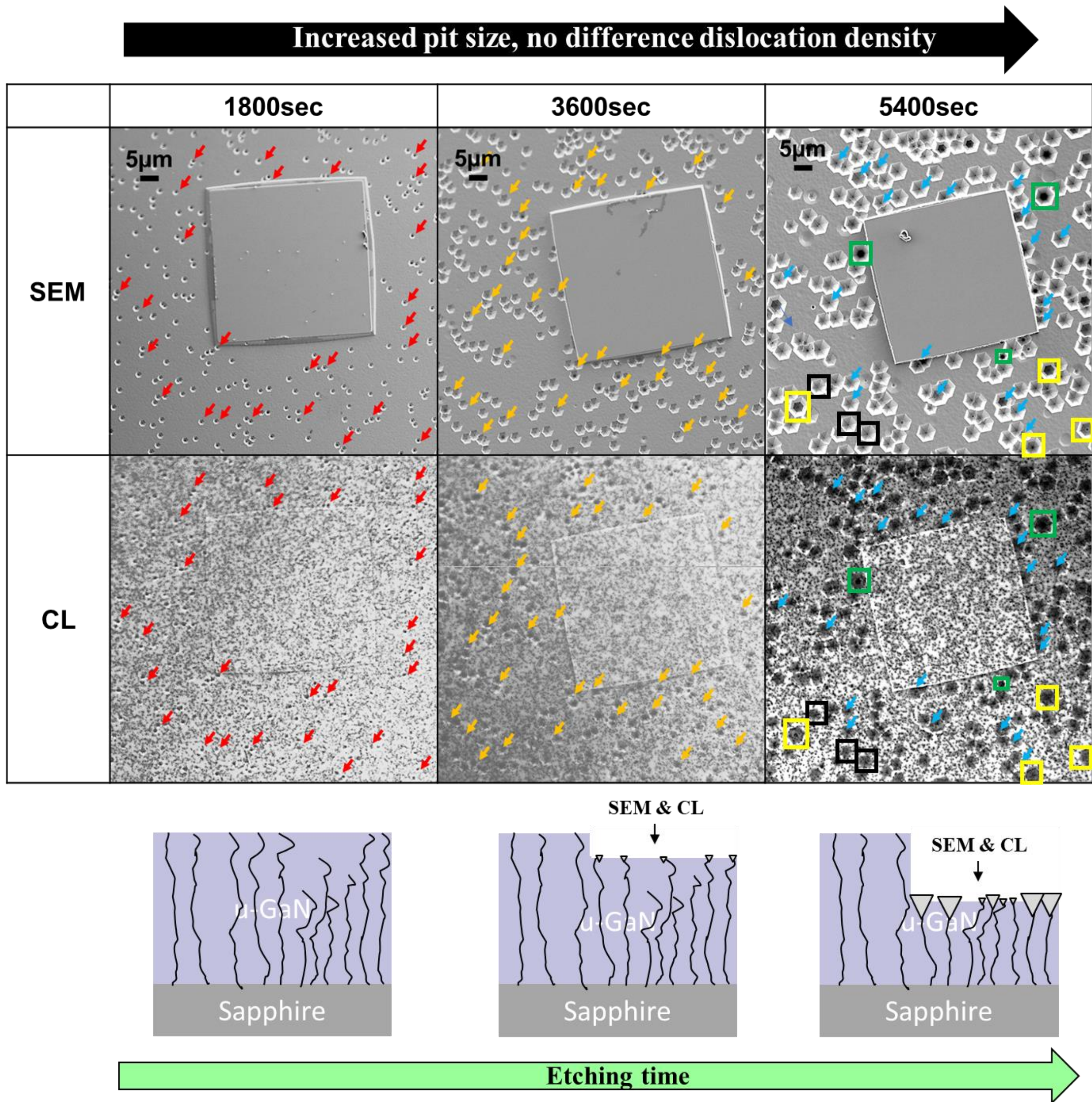


Figure 2.10. Etching time dependent surface behavior on the undoped GaN/sapphire under the bias power of 2.5 W.

However, as bias power becomes large, an etching behavior turns to physical etching (i.e., ion-bombardment), which may create etching damage on the surface [2,4-8].

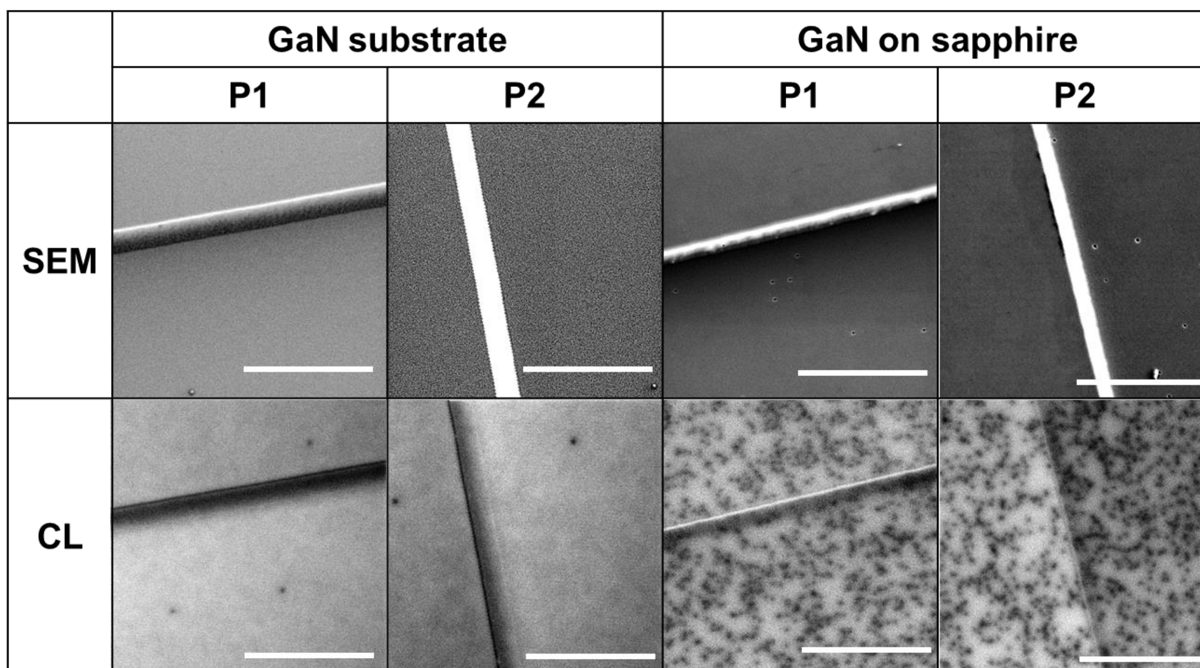


Figure 2.11. Revealing surface smoothness with 30 W bias power etching process. There are almost no pits on the etched surface (SEM images) compared to Figure 2.8 but, the dark spots of CL are clearly seen on the etched surface. Scale bars are 10 μm.

X-ray photoelectron spectroscopy (XPS) can analyze the surface status; therefore, XPS could be suitable method to confirm the surface damage. **Figure 2.12a** is the schematic of XPS measurement process. Each sample was etched by 2.5 W, 5 W, 15 W, 30 W bias power, respectively without any structure. Where ICP power, Cl_2 sccm, and pressure were fixed as 150W, 30 sccm, and 2.0 Pa, respectively, which allows us we compare the effect of etching bias power. Because Cl_2 gas was used as an etching gas, Cl intensity on the surface was firstly investigated as shown in Figure 2.12b. It was observed that Cl 2p intensity differed from the etching bias. As discussed above, the bias power of 2.5 W is basically chemical

etching process and high bias (>15 W) is physical etching based on the ion bombardment. Therefore, the highest intensity of Cl 2p with 2.5 W suggests again that the bias power of 2.5 W is based on the chemical reaction between Cl_2 gas and GaN layer, which led the high Cl intensity on the etched surface than higher bias results. Furthermore, the strongest intensities of Ga 3d and N 1s were observed the sample etched by 2.5 W as shown in Figure 2.12c, d. These results may suggest that the bias power of 2.5 W etches with less damage on the GaN surface and preserves the atomic structure due most likely to the chemical etching process. All of investigation for bias power on the ICP-RIE explains that the etching behavior can be controlled by a bias power, where low bias power guarantees a chemical reaction between etching gas and GaN layer due to insufficient ion-bombardment.

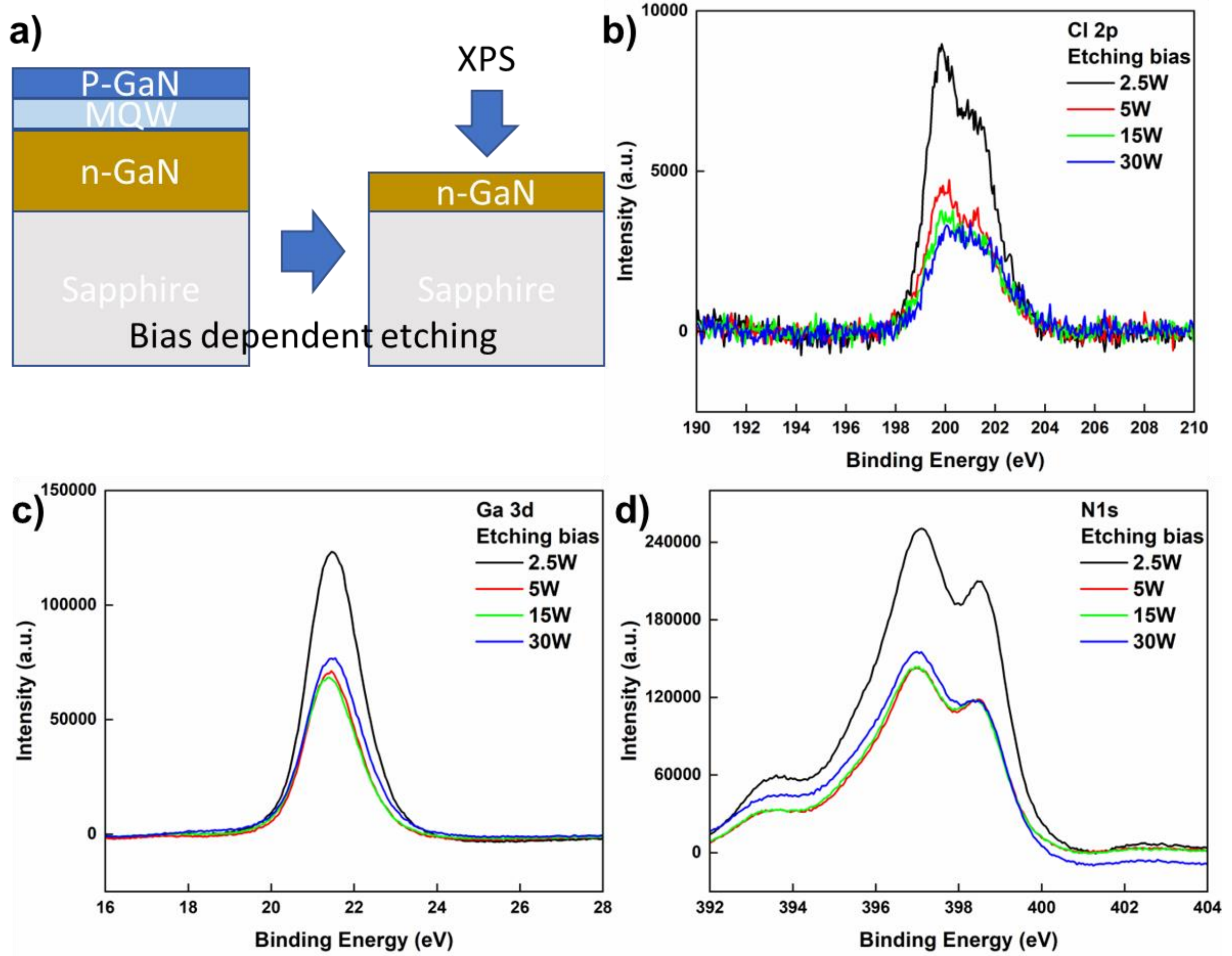


Figure 2.12. Investigation of effect of the etching bias on the nitride epitaxial layer by XPS. a) schematic of experiment. b) Cl 2p c) Ga 3d and d) N1s XPS spectra.

2.3 Summary

Etching bias power dependent etched GaN surface behavior is investigated via various substrates that have different dislocation density. As bias power decreases the surface and sidewall morphology becomes rough; however, with high bias power both morphologies are smooth. This surface roughening is mainly caused by the reaction between etching gas and substrate. If bias power is too low, the chemical reaction is dominant, results in roughed surface. When etching bias power is large enough, the physical etching process is dominant because high ion-bombardment from strong vertical electric field. It is worth noting that GaN substrate that had the lowest dislocation density showed a smooth surface even though it was etched by bias power of 2.5 W. The reason why rough surface occurrence was further demonstrated by SEM and CL images. The surface roughness by bias power of 2.5 W could be decided by the dislocation density. Therefore, the wafer that had highest dislocation density showed the roughest surface and sidewall.

2.4 References

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Chapter 3

The effect of dry etching conditions on the performance of micro-LEDs

3.1 Introduction

Although micro-LEDs have many potential benefits realizing next generation display such as virtual reality (VR), augmented reality (AR), and near eye display, it is still challenging with high efficiency. For example, such kinds of displays require high PPI, which is consistent with small pixel size (usually, VR and AR require over 2000 PPI). However, the smaller LED, more suffer from the sidewall damage that degrades internal quantum efficiency (IQE) [1-4]. To mitigate the sidewall damage, there have been various report over the past few years. The deposition of passivation layer at the sidewall with silicon dioxide [5], aluminum oxide [6], and aluminum nitride [7] by using atomic layer deposition. This technique could reduce not only the leakage current but also increase the external quantum efficiency (EQE) by alleviating sidewall defects and surface recombination that is induced by plasma induced ICP-RIE process. In addition, the traditional method of chemical etching at the sidewall by using hydroxyl-based etchants, such as tetramethylammonium hydroxide and potassium hydroxide, were adopted to etch III−nitride sidewall surface to remove a plasma induced damage and to improve the light extraction efficiency via rough surface [8-10]. Above two methods suggest that sidewall engineering is key factor in high-performance micro-LEDs. Therefore, the damage control of sidewall is the way for realizing high performance of micro-LEDs.

Recent consumer electronics such as smartphones, TVs, and laptops those technologies are based on the liquid crystal display or organic light-emitting diodes operate around 100 ~ 1,000 nits, which is not so bright under the sunlight. Because of their limitation of performance, it is quite difficult to realize ultrahigh brightness display. Meanwhile, AR and projection displays, which can be realized by micro-LEDs technology, require ultrahigh brightness display (e.g., > 1,000,000 nits) to operate in a bright place [11-12]. Moreover, the human eye is less sensitive to the blue or red color than the green color due to the human eye's luminous efficiency, which means the blue or red emission output should be larger than the green color to make same brightness. For instance, the yellowish green color with a wavelength of 555 nm that has maximum luminous efficiency has 16.67 and 3.77 times high luminous efficiency than the blue color with a wavelength of 470 nm and the red color with a wavelength of 630 nm [13]. Thus, blue and red colors are required higher light output for high brightness than the green LED. However, commercialized blue LEDs, even micro-LEDs, has the maximum EQE at the low current region (e.g., under 20 A/cm^2), and it cannot avoid the efficiency droop at the high current region, meaning that commercialized LEDs epi structure is not efficient in the high-current region for realizing ultrahigh light output and brightness. It was reported that 6.5 x 6.5 μm^2 blue micro-LEDs had approximately 1,000,000 nits at 500 A/cm^2 [14]. This current is higher than green micro-LEDs due to the luminous efficiency. Moreover, this current is in the efficiency droop regime. Therefore, it is important to make that micro-LED operates at the high current density with high efficiency for high brightness display.

In this chapter, we aim that improving the performance of micro-LEDs through suppressing sidewall damage. First, the influence of the etching bias power, firstly investigated in Chapter 2, on micro-LEDs will be discussed. To evaluate the impact of ICP-RIE etching bias power, the leakage current and ideality factor, indicating I-V characteristics were investigated. Because the

surface morphology decides the light extraction efficiency, finite-difference time-domain (FDTD) simulation was studied to clarify the enhancement of light extraction efficiency via rough sidewall morphology. Second, to realize high brightness display at high current regime, we investigated the specially designed epitaxial wafer that has thin quantum barrier. It was found that micro-LEDs with a thin quantum barrier have less efficiency droop, small electroluminescence (EL) shift, and maximum EQE at the high current region, which is caused by less polarization effect on the quantum well than commercial LED. Therefore, micro-LED that has thin quantum barrier is suitable for realizing high brightness display with less efficiency droop at high current regime.

3.2 Device structure and fabrication process

First, a blue color emitting epi wafer was grown on c-plane sapphire without undoped GaN layer by metal-organic vapor-phase epitaxy method. Around 30 nm AlN buffer layer deposited on c-plane sapphire. 4×10^{18} cm^{-3} silicon doped n-GaN was grown on buffer layer. After that, 7 pair multiple quantum well (InGaN/GaN = 3.5/3 nm) was grown. To prevent electron overflow, p-$Al_{0.25}Ga_{0.75}N$ layer was grown. Finally, p and p++ GaN layers were grown with Mg 2×10^{19} cm^{-3} and 2×10^{20} cm^{-3} doping concentration, respectively. The epi structure was confirmed by secondary ion mass spectrometry (SIMS) as shown in **Figure 3.1**a. Detail quantum well structure is available in Figure 3.14a. Prior to fabrication device, emission wavelength firstly confirmed by the photoluminescence (PL) spectrum at room temperature; the peak wavelength was around 440 nm as shown in Figure 3.1b.

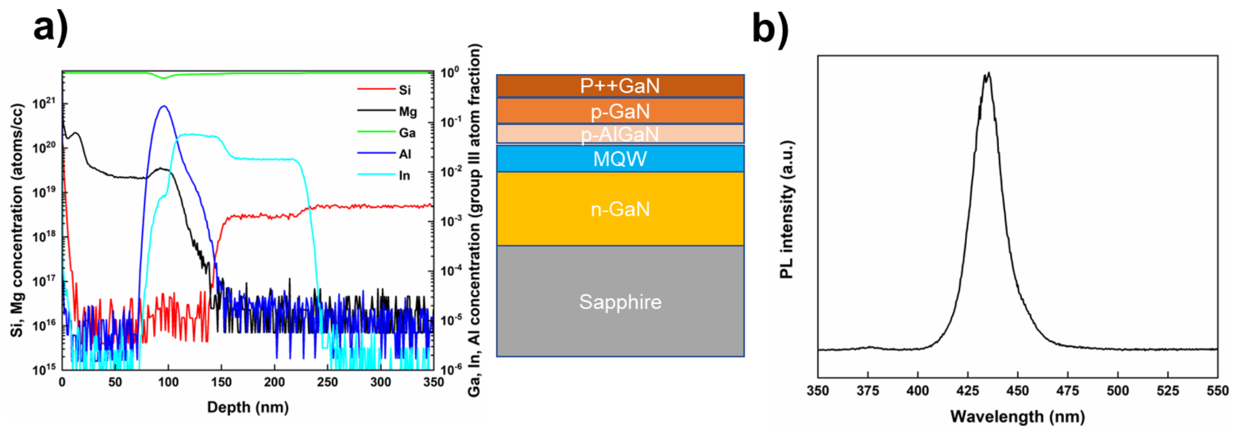

Figure 3.1. a) SIMS data for confirming doping concentration each layer. b) PL spectrum of used epi wafer in this work. Peak wavelength was around 440 nm, indicating a blue color LED.

A passivation layer is usually deposited on the micro-LEDs device to form an electrode. According to Wong et al. the performance of micro-LEDs could be affected by what kind of passivation layer is deposited on the sidewall of micro-LEDs [5]. To avoid the effect of passivation layer and accurately demonstrate the influence of etching bias power, any passivation layer was not deposited on the device.

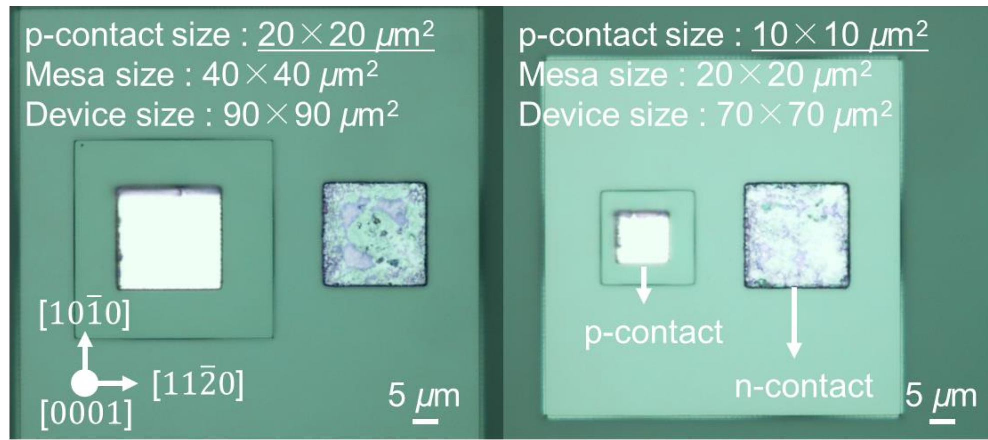

Figure 3.2. Optical microscopy image of the designed micro-LEDs.

Figure 3.2 shows the designed micro-LEDs structures in this work. The large sample had 20 × 20 μm^2 p-contact and 40 × 40 μm^2 mesa structure. The small sample had a p-contact with a size of 10 × 10 μm^2 and mesa with a size of 20 × 20 μm^2. Both samples had same n-contact size as 20 × 20 μm^2. Before process, the epi wafer firstly was annealed at 700 ℃ for 10 min to activate the p-GaN layer [15]. All devices were subjected to same isolation etching process to reveal sapphire. The condition of isolation was 150 W of ICP power, 15 W of etching bias power, 30 sccm of Cl_2, and 2.0 Pa by ICP-RIE system. After that, mesa etching was performed to each sample with different etching conditions. The ICP power, Cl_2, and pressure were fixed at 150

W, 30 sccm, and 2.0 Pa, respectively. Only difference is the etching bias power. 2.5, 5, 15, and 30 W bias power, determining the power of ion bombardment, were adopted to investigate the etching damage, where etching time was 3420, 985, 300, and 175 second, respectively. The target mesa depth of all devices was around 600 nm. For ohmic contact, Ti/Al/Ti/Au (20/100/30/200 nm) were deposited on the n-GaN with annealing at 650 ℃ for 5 min in N_2 ambient [16] and Ni/Au (20/300 nm) were deposited on the p-GaN with annealing at 525 ℃ for 5 min in O_2 ambient [17]. Metal deposition and annealing process were proceeded by electron-beam evaporation and rapid thermal annealing (RTA), respectively. All process is well described in **Figure 3.3**.

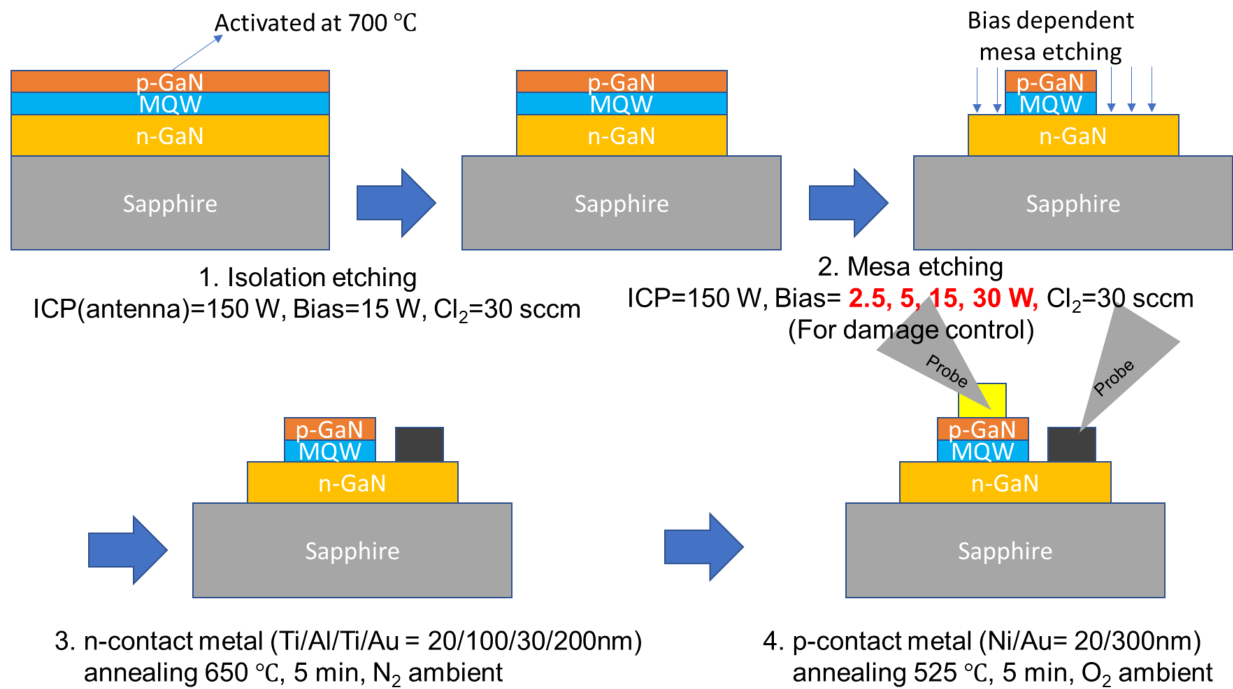

Figure 3.3. Schematic of illustration for micro-LEDs fabrication process.

3.3 Current-voltage characteristic with various etching bias

The effect of etching bias has been demonstrated according to the current-voltage (I-V) characteristics. The 10 × 10 μm^2 and 20 × 20 μm^2 size of p-contact devices with various etching bias were applied the bias from -20 V to 7 V.

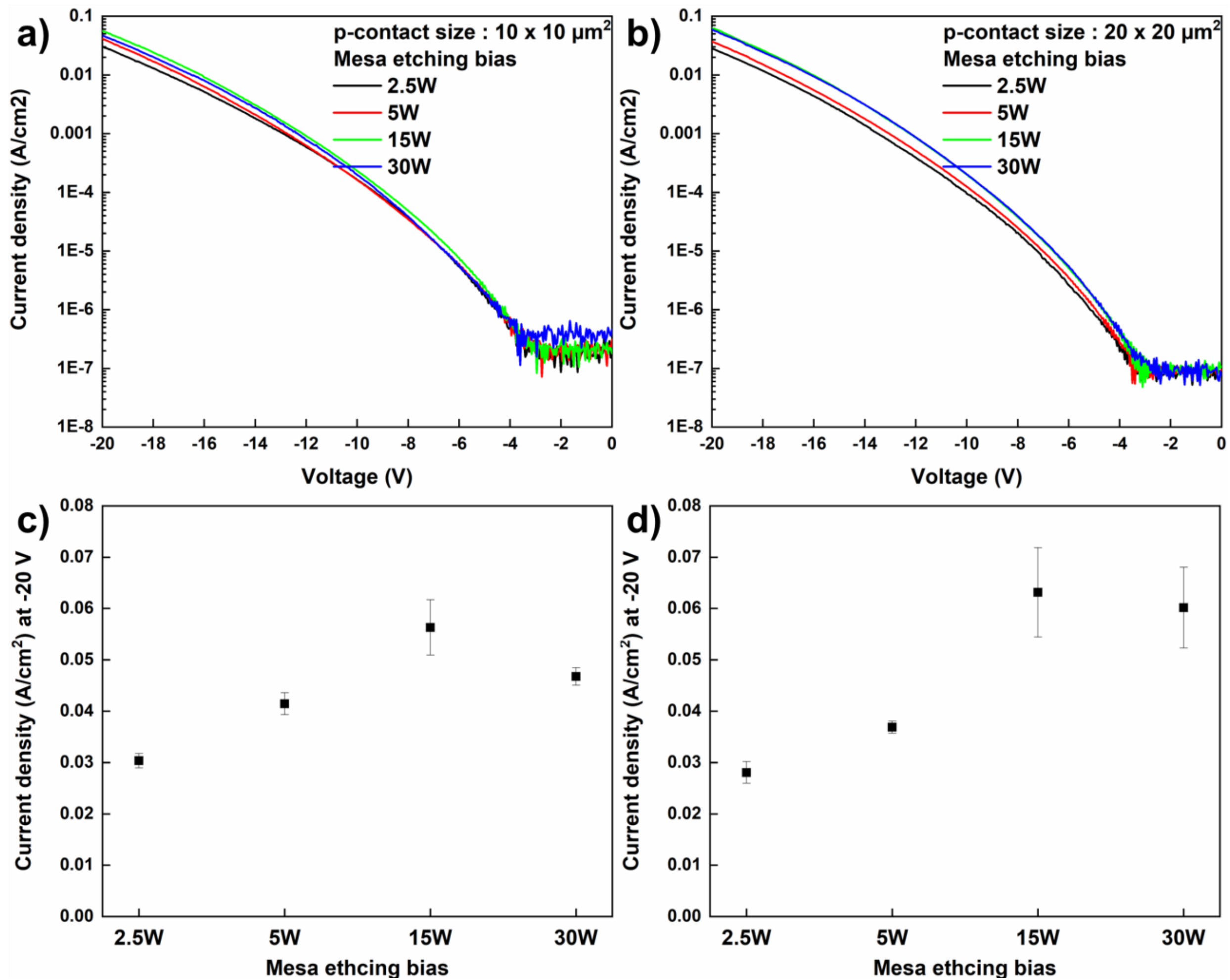

Figure 3.4. I-V characteristics of designed micro-LEDs with a size of a) 10 × 10 μm^2 and b) 20 × 20 μm^2 p-contact under reverse voltage. Etching bias dependent leakage current density at -20 V c) 10 × 10 μm^2 and d) 20 × 20 μm^2 p-contact size.

Figure 3.4a and b show the I-V curves under the reverse voltage for 10 × 10 μm^2 and 20 × 20 μm^2 p-contact size, respectively. All samples showed that the leakage current density dramatically increased under -4 V but from -4V to 0V was comparatively similar regardless of mesa etching bias power. However, it was clearly seen that 10 × 10 μm^2 and 20 × 20 μm^2 sample had approximately ~3 × 10^7 A/cm^2 and ~10^7 A/cm^2 from -4V to 0V, respectively. In addition, overall, 10 × 10 μm^2 of current density was higher than 20 × 20 μm^2, meaning that the smaller size LED, the higher leakage current density. This could be attributed to the increase in the leakage path due to the relatively large area of the sidewall as LED size shirking [18-19]. The observed leakage current density at -20 V tend to be decreased with decreasing etching bias power in both sizes as shown in Figure 3.4c and d, which could indicate the plasma induced surface damage was controlled by changing the etching bias. In addition, it was clearly seen that the device etched by lowest bias power etching (i.e., 2.5 W) had the lowest leakage current in both sizes, which further demonstrates that the chemical reaction between etching gas and GaN layer was dominant rather than ion bombardment. Lee et al. demonstrated that a double sidewall passivation layer (i.e., ALD-Al_2O_3/PECVD-SiO_2) effectively reduce the plasma induced sidewall damage rather than single PECVD-SiO_2; thus, double sidewall passivation layer allows a relatively low leakage current [6]. In addition, Yamada et al. demonstrated that low bias power etching leads less lattice distortion of the sidewall surface, indicating reduced etching damage; thus, low leakage current was allowed in Schottky barrier diodes [20-21]. Therefore, it can be inferred that the lowest leakage current density with a lowest etching bias can be attributed to the reduced plasma damage on the etched surface even at the sidewall.

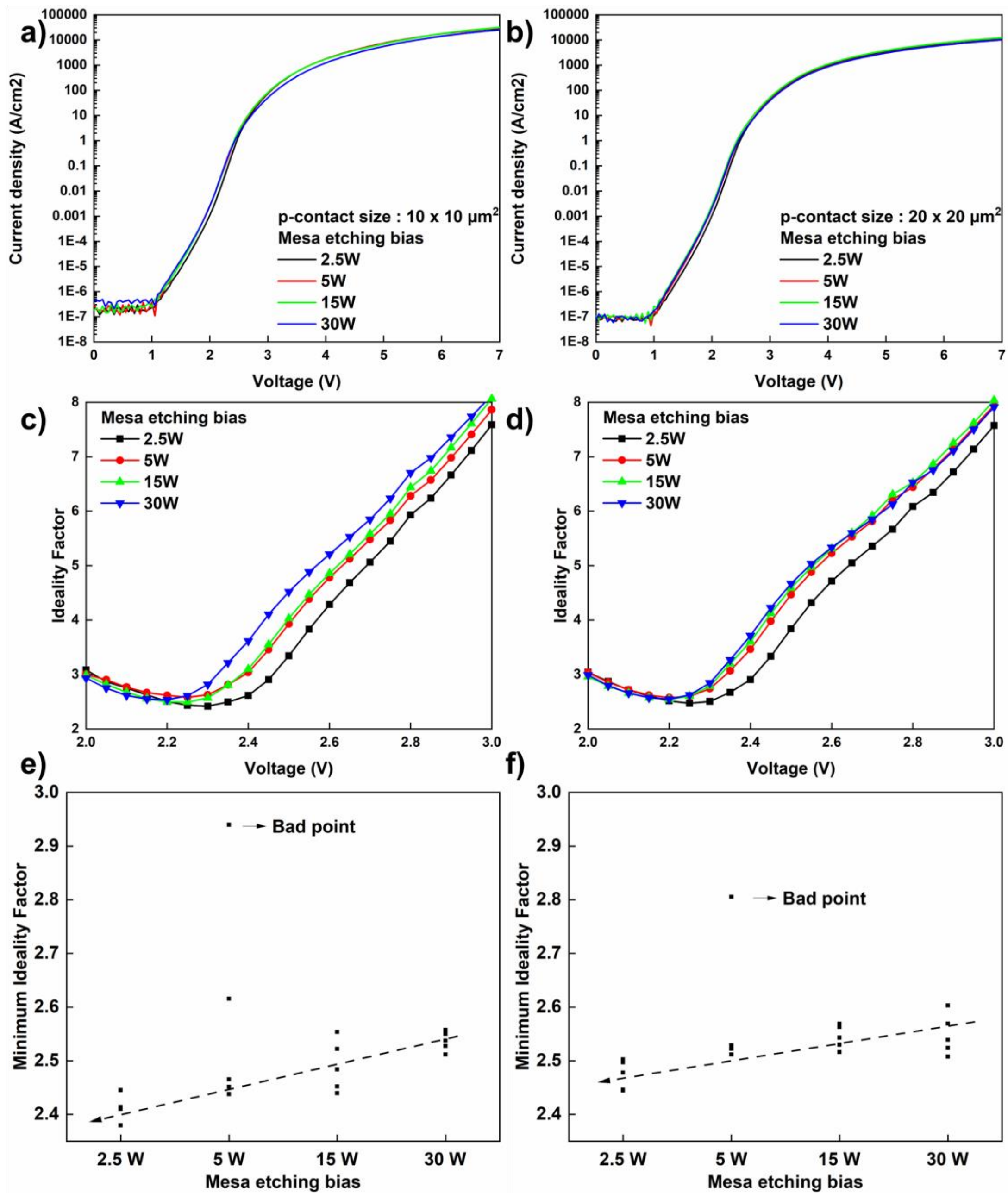

Figure 3.5. I-V characteristics of designed micro-LEDs with a size of a) 10 × 10 μm^2 and b) 20 × 20 μm^2 p-contact under forward voltage. Etching bias dependent ideality factor extracted from I-V curve from 2.0 to 3.0 V c) 10 × 10 μm^2 and d) 20 × 20 μm^2 p-contact size. Minimum ideality factor for each mesa etching bias e) 10 × 10 μm^2 and f) 20 × 20 μm^2 p-contact size.

Figure 3.5a and b show the I-V curves under the forward voltage for 10 × 10 μm^2 and 20 × 20 μm^2 p-contact size, respectively. One can see that the smaller LEDs had higher current density than the lager LEDs. For example, 10 × 10 μm^2 of current density at 7 V was around 25,000 A/cm^2; however, 20 × 20 μm^2 was around 10,000 A/cm^2. This behavior can be attributed to the size effect. As LED size decreases, better current spreading, better thermal distribution and less current crowding, resulting in better homogeneous carrier distribution [2,22]. The ideality factor is useful for understanding recombination mechanisms, such as Shockley-Read-Hall (SRH) nonradiative recombination, trap-assisted tunneling, and carrier leakage. Basically, depending on the value of the ideality factor, it has different meaning. For example, an ideality factor of 1.0 is associated with the band-to-band radiative recombination, an ideality factor of 2.0 indicates the SRH nonradiative recombination, and over 2.0 means defect-assisted tunneling phenomenon; low ideality factor indicates better device performance [3,23]. Therefore, the relationship between ideality factor and etching bias power needs to be investigated. The ideality factor was calculated by Equation (1) given by:

$$n_{ideality} = \frac{q}{kT}\left(\frac{\partial \ln I}{\partial V}\right)^{-1} \quad (1)$$

where q is the elementary charge, k is the Boltzmann constant, and T is the kelvin temperature. Since the I-V curve was measured at room temperature (i.e., 300 K), $\frac{kT}{q}$ was 0.0259. It was confirmed that the ideality factor increased with the increased applied voltage (from 2.2 to 3.0 V), which is related to the dominant series resistance [24]. Interestingly, the ideality factor decreased with decreasing the etching bias in both sizes as shown in Figure 3.5c and d. In addition, the lowest etching bias yielded the lowest ideality factor. Since the current started to

saturate above 2.3 V, it needs to be observed the minimum ideality factor near 2.3 V. Because the minimum ideality factor usually indicates the SRH nonradiative recombination. It was confirmed that minimum ideality factor as a function of mesa etching bias overall decreased as mesa etching bias decreased regardless of size as shown in Figure 3.5e and f. Because plasma damage degrades the device performance by providing defect points such as vacancies, implanted ions. Such kinds of defect points also increase the barrier height. Therefore, high etching bias leads the high ideality factor indicating the etching damage [25]. Meanwhile, Wong et al. reported that the KOH chemical treatment decreased the ideality factor in the $10 \times 10\ \mu m^2$ scale micro-LEDs due to the removing sidewall damage. Therefore, it can be inferred that the low bias power etching (2.5 W) also suppresses the plasma induced sidewall damage and thus, lowest ideality factor was observed in both sizes.

3.4 The effect of sidewall morphology on the light extraction

The light propagation and pattern are entirely affected by the refractive index of materials. For example, if the light comes out from the InGaN/GaN MQW to air, the light only can escape with limited angle. This angle so called the light escape cone between different materials can be calculated according to Snell's Law:

$$\theta \approx arcsin(\frac{n_{out}}{n_{in}}) \quad (2)$$

In Equation (2), n_{in} is the refractive index starting the light movement and n_{out} is the refractive index of material escaping light. Since refractive index of GaN is 2.5 in visible range and air is 1, the light escape cone is around 23.5 ° from GaN to air, meaning that the emitting light only can escape via 23.5 °. Again, the ratio of $\frac{n_{out}}{n_{in}}$ should be 1 to maximize the light escape cone. Like this, low escape cone between GaN and air prevents to reach high efficiency LED. To overcome this issue, the effect of surface texture on light extraction has been investigated over last a few ten years. **Figure 3.6** describes the basic concept of the effect of surface texture [26]. A perfectly smooth surface shown in Figure 3.6a results in the light cannot easily escape. However, as surface becomes rough shown in Figure 3.6b and c, the scattering becomes strong and thus the light has more chance to escape from inside to outside. By roughening a surface, the interfacial refractive index (i.e., ERI) could be reduced, which totally increases θ with reducing the difference between n_{in} and n_{out}. Following this concept, it is important that the surface escaping light should be very rough to increase light extraction efficiency [27]. Song et al. reported that the light extraction of 633 nm AlGaInP LED can be enhanced by antireflective subwavelength structures (SWS) [28]. Since SWS structure reduces the reflection between GaP surface and air, light extraction increases.

Figure 3.7 explains why surface morphology critically affects light extraction. As described in Figure 3.7a, the moth-eye structure has rough morphology at the interface between air and structure. This roughing structure provides relatively low refractive index than the refractive index of original material. For example, rough surface makes alleviated slope of refractive index between material and air, and thus, refractive index does not change drastically, meaning that rough surface creates a different refractive index at the interface, which is so called effective refractive index. Iwaya et al. demonstrated that a biomimicry moth-eye structure at the bottom of GaN blue LED can improve the light extraction efficiency via rough surface [29].

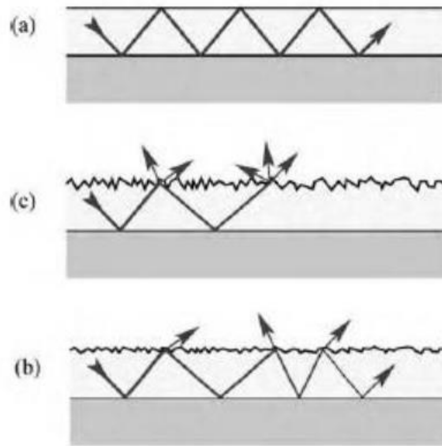

Figure 3.6. Schematic illustration of waveguide with various surface texture, resulting in different light scattering and extraction [26].

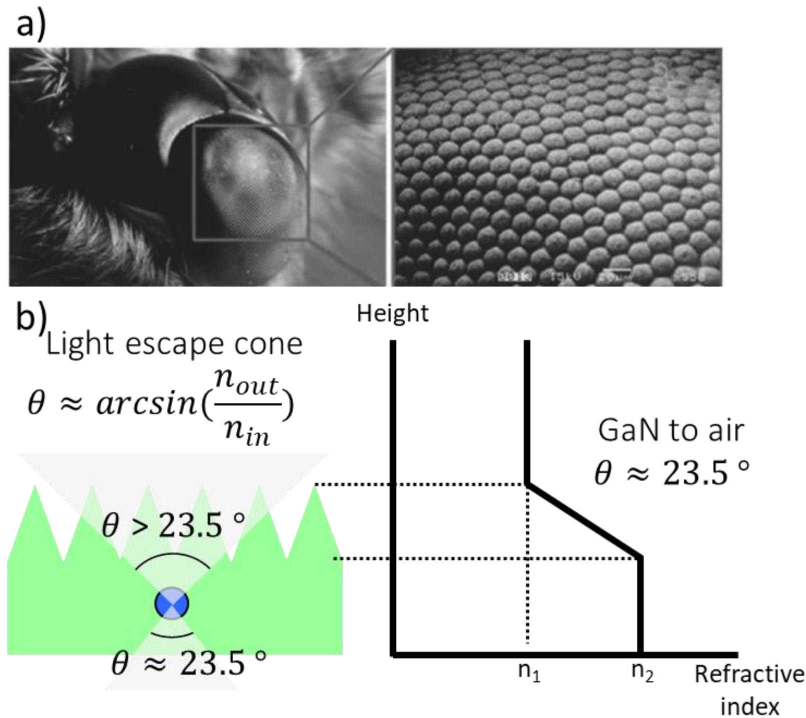

Figure 3.7. a) a biomimicry moth-eye structure of butterfly. A rough surface allows to move a light with large angle. b) Surface morphology dependent refractive index. Refractive index decreases as surface becomes rougher.

Figure 3.8a shows the artificially created moth-eye surface via Au nano mask. With moth-eye structure, light output markedly increased as shown in Figure 3.8b due most likely to the decreasing effective refractive index at the interface. Therefore, this data indicates that surface roughing is a key technology for enhancing light extraction efficiency. So far, commercial LED size (e.g., >300 μm) does not consider light output via sidewall because sidewall area relatively smaller than the bottom or top, therefore, most light goes out through the bottom or top of LED. However, as LED size shrinks (i.e., micro scale LED), the light emission via sidewall becomes dominant.

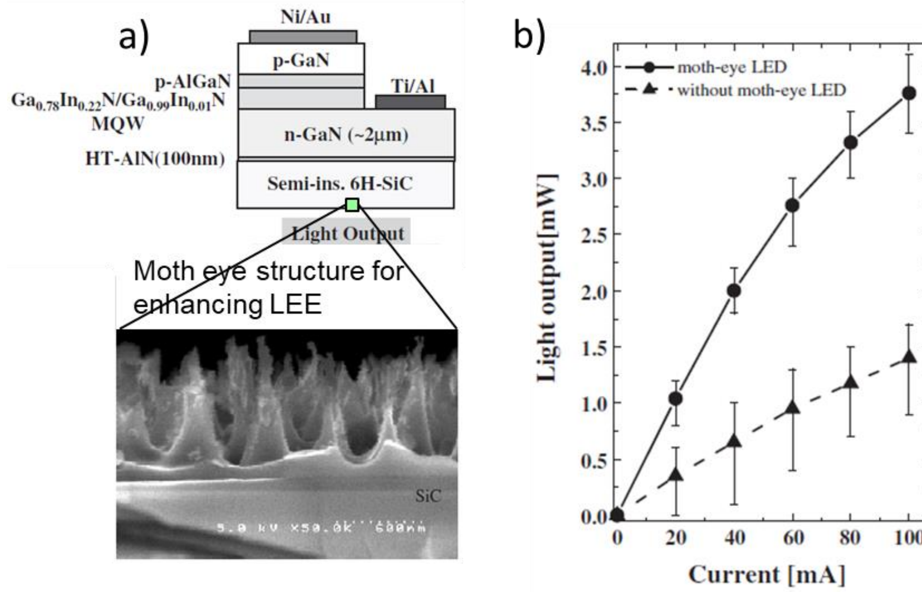

Figure 3.8. a) Schematic of moth-eye surface induced LED structure. b) Light output as function of current with and without moth-eye surface [29].

In other words, the generated light from the MQWs escapes from top, bottom and sidewall, but the portion of light escaping from top, and bottom is smaller. Gou et al. calculated the sidewall emission ratio with various chip size [30]. According to **Figure 3.9**, the sidewall emissions from R,G,B micro-LEDs increases more with smaller chip size, suggesting that the sidewall emission have to be carefully considered to realize high efficiency ultra-small micro-LEDs.

Chip size (μm^2)	Red		Green		Blue	
	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.
15 × 30	10.8%	11.0%	58.9%	58.5%	62.2%	65.7%
35 × 60	5.3%	5.6%	52.4%	54.2%	55.1%	56.7%
50 × 100	3.8%	4.0%	47.2%	49.6%	50.1%	52.9%

Figure 3.9. Calculated sidewall emission ratio with different LED size and color [30].

In summary, as the size decreases, the light emission via sidewall acts as a main factor in light extraction efficiency, and thus it is required to create rough sidewall for highest light extraction efficiency.

To improve the roughness of sidewall, chemical treatments such as hydroxyl-based potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) can be used to reveal m-plane nano facets. These etchants increase the roughness of the sidewall morphology because it reacts with non-polar nitride surface and reveals m-facets. This revealed m-facets increases the sidewall morphology, and thus increases the light extraction efficiency [8-9].

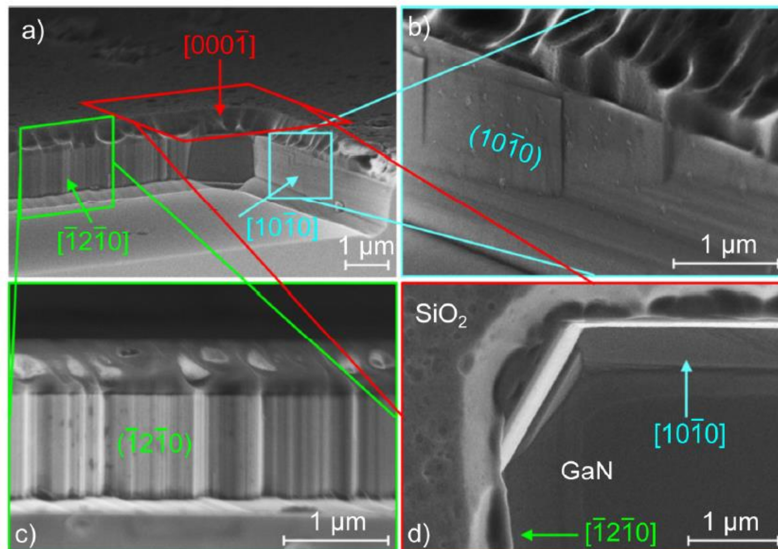

Figure 3.10. KOH treated non-polar GaN surface [31].

As shown in **Figure 3.10**, it can be seen that a-plane GaN surface shows jagged surface behavior; however, m-plane GaN surface looks smooth, indicating that the chemical treatment on the nitride non-polar surface only selectively creates rough surface depending on the direction of the surface owing to the lack of reaction [31]. Because most LED structures have square shape, it has a- and m- plane both direction sidewall. The chemical treatment may not be sufficient to create a rough

sidewall morphology since the reaction is only fast on the a-plane sidewall. In this regard, it is worth noting that the sidewall morphology could be roughened by changing the etching bias power regardless of the plane direction as shown in Figure 2.6. To confirm the effect of sidewall roughness on the light extraction efficiency of micro-LEDs, the light extraction behavior has been investigated by 3D FDTD simulation (Lumerical Inc.).

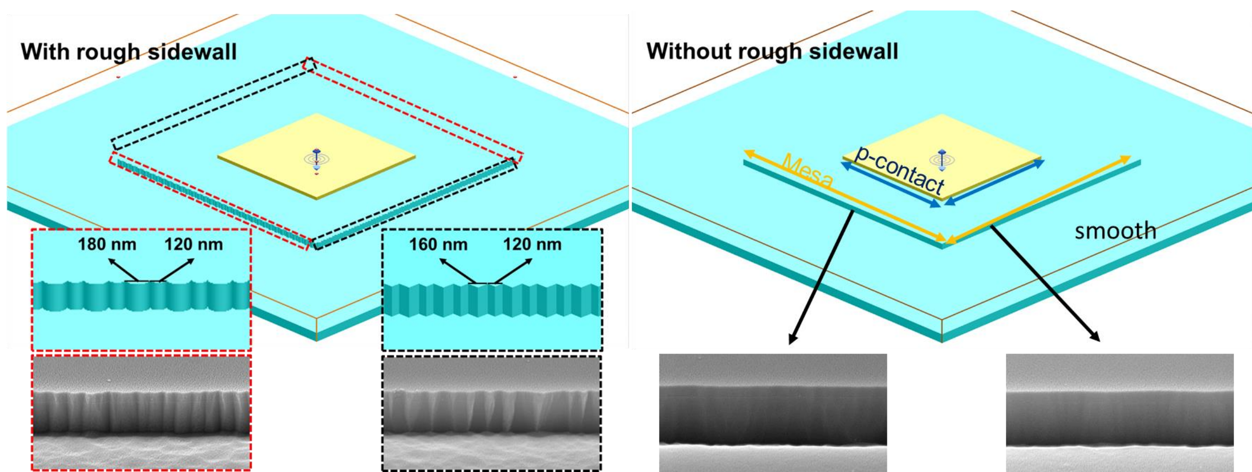

Figure 3.11. Schematic of 3D FDTD simulation setup. The rough sidewall was assumed as 2.5 W bias power etched surface and the smooth sidewall was assumed as 30 W bias power etched surface.

As shown in **Figure 3.11**, the bias power of 2.5 W had the roughest surface, and the bias power of 30 W had the smoothest surface in both sidewall direction. Therefore, based on these two cases, sidewall morphologies were adopted similarly from SEM image in the simulation system. Because the a- and m-plane morphologies were different with the bias power of 2.5 W, the morphology was applied differently each direction. For example, a-plane morphology looked a cylinder shape with 180 and 120 nm diameters and m-plane morphology looked a triangular pillar with 160 and 120 nm distance. Therefore, in simulation system, the sidewall morphology was set up following SEM information similarly as shown in Figure 3.11. Regarding 30 W, both directions were not

significantly different, and thus the same smooth morphology was applied to both directions. In this simulation system, several materials such as Ni, Au, sapphire, and GaN were used. Before simulation start, refractive index and absorption coefficient of the used materials have been set up according to the embedded values in the FDTD system. A GaN layer has around 2.5 and 0 of refractive index and absorption coefficient in the visible range, respectively [32]. In addition, the refractive index and absorption coefficient are not significantly different by the doping concentration and content, refractive index and absorption coefficient of the GaN layer have been set by 2.49 and 0 respectively. Micro LED structures of two sizes have been studied in simulation system to clarify LED size dependent effect of sidewall morphology. The smaller one had 5 × 5 μm^2 Ni/Au p-contact and 10 × 10 μm^2 mesa. The larger one had 10 × 10 μm^2 Ni/Au p-contact and 20 × 20 μm^2 mesa. The mesa width and length are two times larger than p-contact. All simulation systems had a same Ni/Au (20/300 nm) and mesa (600 nm) thickness. Since the PL peak was observed around 440 nm as shown in Figure 3.1b, the dipole source had a wavelength of 400 nm with z-axis single polarized source. Finally, boundary conditions were set to a symmetric for x, and y minimum to save simulation time. **Figure 3.12**a and b shows 20 × 20 μm^2 and 10 × 10 μm^2 mesa size field intensity distribution observed by monitor next to the sidewall. There was no difference in the field intensity of smooth sidewall (30 W case) regardless of sidewall direction, which is caused by the equally set the sidewall morphology on both directions. On the other hand, it was observed that the field intensity of rough sidewall (2.5 W case) differed with plane direction. These differences indicate that the surface roughing decides the light extraction. In addition, regardless of plane direction, the rough sidewall had more concentrated field intensity in both direction than the smooth

sidewall, suggesting artificially roughen sidewall enhance the light extraction. Furthermore, FDTD calculated the enhancement of light extraction efficiency. The calculated enhancements were approximately 1.20, 1.27 for 10 × 10 μm^2 and 20 × 20 μm^2, respectively, which obviously indicates that the artificially roughen sidewall enhances the light extraction efficiency again. Therefore, the improving sidewall emission via roughening will be a key factor in increasing the efficiency of micro-LEDs.

Regarding the display application, the enhancement of LEE through the sidewall emission shown in Figure 3.12 is undesirable because the light traveling parallel leads the optical crosstalk, which aggravates the performance of display. Therefore, the light needs to be collected perpendicularly to the wafer to suppress the optical crosstalk. The solutions will be discussed in Chapter 5.

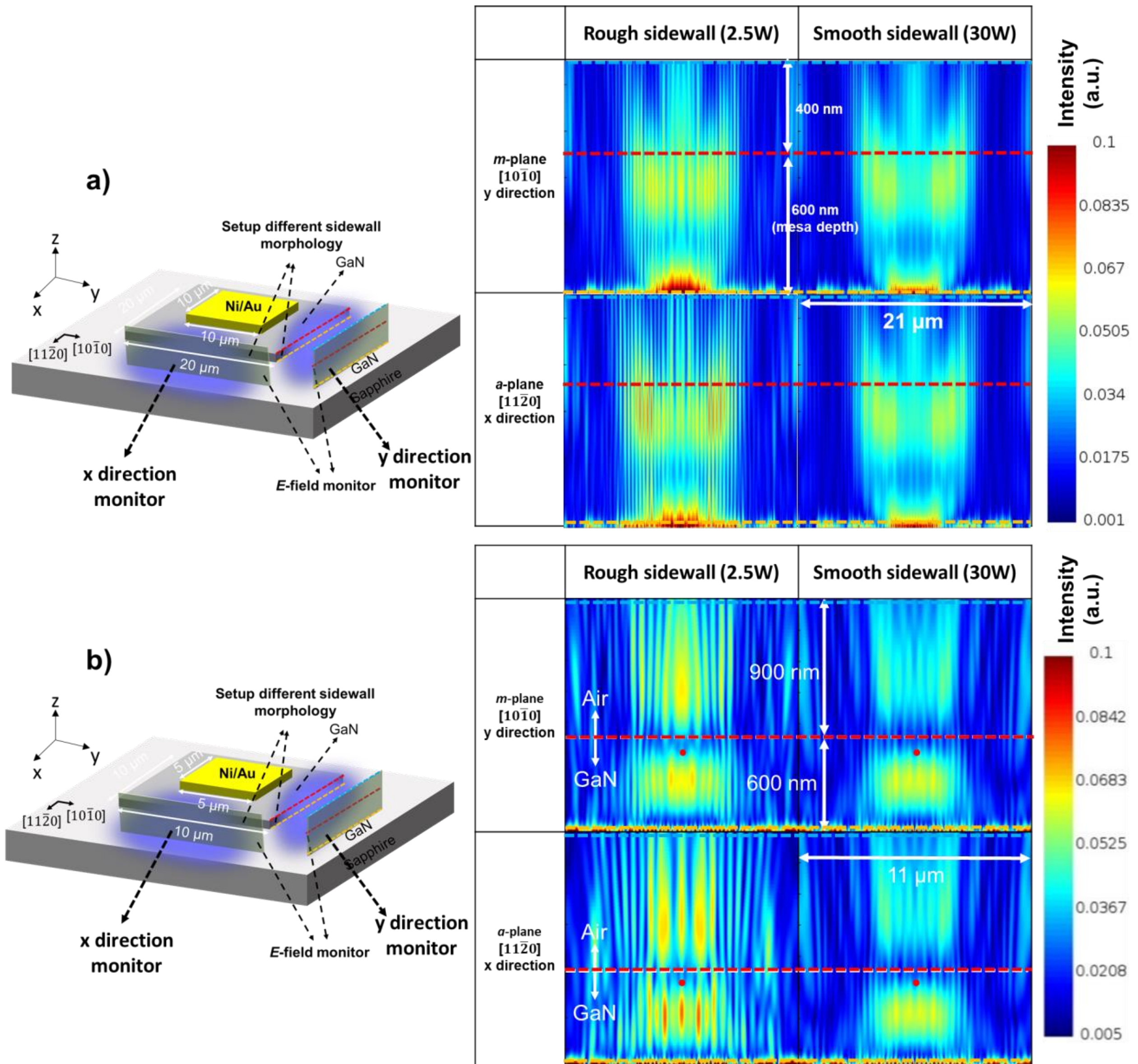

Figure 3.12. Sidewall morphology and plane direction dependent light field intensity captured next to the sidewall. a) 20 × 20 μm^2 GaN mesa structure b) 10 × 10 μm^2 GaN mesa structure.

3.5 Combined effects of suppressed sidewall damage and enhanced light extraction efficiency on EQE

Figure 3.13 shows light output and EQE curves as a function of the injected current density for 10×10 μm^2 scale size blue micro-LEDs at the high current density region and measured by an integrating sphere (Ocean Insight, FOIS-1) that was placed under the sample according to the etching bias. The EQE graphs were plotted by Equation (3),

$$\mathrm{EQE}(\%) = \frac{P_{out}\lambda_{peak}}{I} \times \frac{q}{hc} \times 100 \qquad (3)$$

where I is the injected current, λ_{peak} is the EL peak wavelength at I as a plotted in Figure 3.16, and q, h, and c are the elementary charge, Plank constant, and light speed, respectively. Regardless of etching bias, the efficiency droop at the 10 mA was approximately 20%, where 10 mA is corresponding to the 10,000 A/cm^2. Furthermore, the maximum EQE of all samples were observed at 2,000 A/cm^2, which is much higher than the reported results [33]. These two results could be explained by thin QB that leads to not only more efficient hole injection in QW but also the suppressed polarization effect (Detail of the polarization effect will be explained in section 3.6). However, as shown in **Figure 3.14** for 20×20 μm^2 scale size blue micro-LEDs, it was observed that the efficiency droop was approximately 40% at the 40 mA, where 40 mA is corresponding to the 10,000 A/cm^2. According to Hwang et al., efficiency droop of micro-LEDs could be attributed to the current spreading [34]. They investigated the size dependent efficiency droop that was proportional to the LED size, which means larger LED, higher efficiency droop. This phenomenon might be explained by uniform current spreading for small device through the sidewall. For example, the current of large size LED (> 300 μm) is concentrated at the sidewall because current flows from p-contact to n-contact. Therefore, as LED size increases current is more concentrated

at the sidewall (i.e., increasing current crowding). If LED size small, current can be more uniformly distributed, which makes more uniform light emission and less efficiency droop [35-36]. However, it needs to be understood that LEDs usually suffer from increasing junction temperature with high injection current due to the current crowding. Gong et al. showed that junction temperature does not significantly increase if size is less than 40 µm diameter even though current density reached approximately 2000 A/cm^2 [35]. Therefore, as LED size decreases, the current distributes uniformly near the mesa, which makes less current crowding, less temperature increasing.

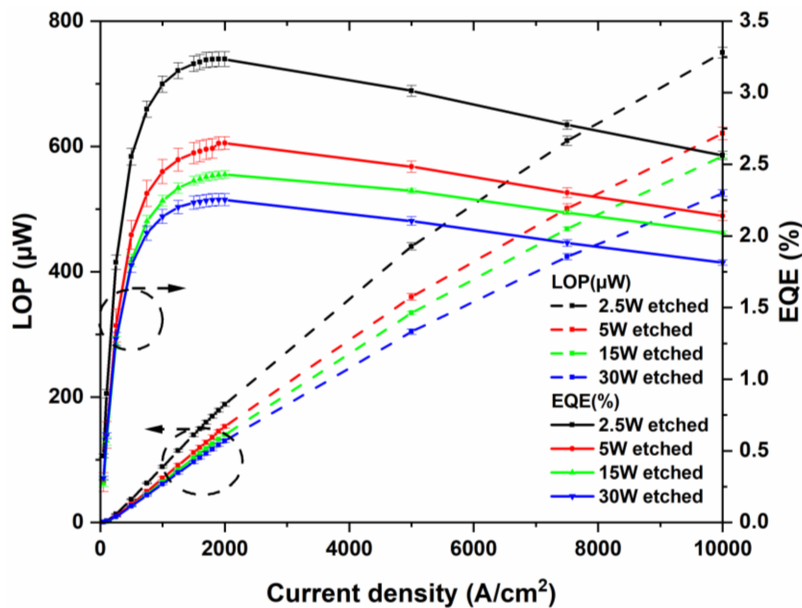

Figure 3.13. Light output and EQE curves as a function of the injected current for 10 × 10 µm^2 scale size blue micro-LEDs.

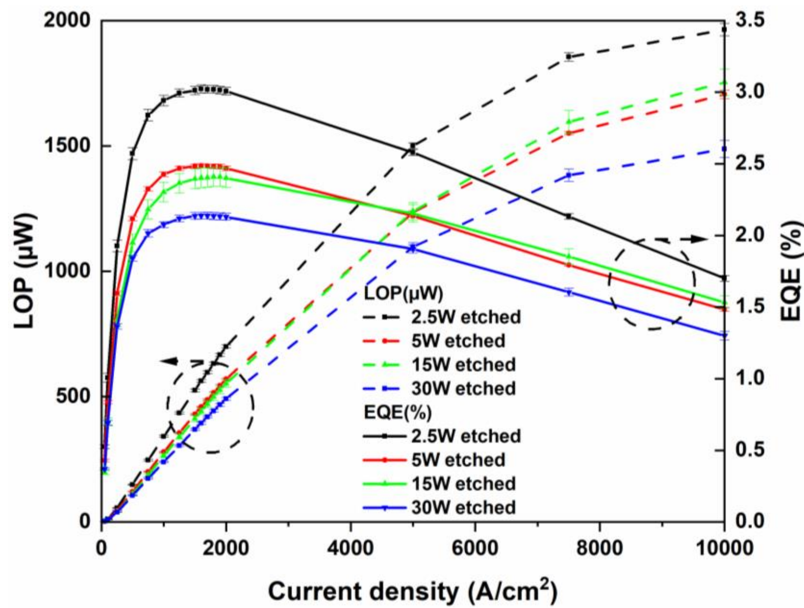

Figure 3.14. Light output and EQE curves as a function of the injected current for 20 × 20 μm^2 scale size blue micro-LEDs.

It was observed that maximum EQEs differed with the etching bias both sizes and were 3.23%, 2.65%, 2.43%, and 2.25 % for 2.5, 5, 15, and 30 W, respectively for 10 ×10 μm^2 size shown in Figure 3.19 and were 3.02%, 2.48%, 2.40%, 2.13% for 2.5, 5, 15, and 30 W, respectively for 20 × 20 μm^2 size shown in Figure 3.20. Interestingly, 15 W sample showed higher EQEs than 30 W sample even though both samples had almost similar sidewall morphologies as shown in Figure 2.6 and showed overlapped light output at the low current region shown in Figure 3.15. This different behavior could be explained by the reduced sidewall damage of micro-LEDs rather than the effect of light extraction efficiency. On the other hand, 2.5 W sample showed the highest light output and maximum EQE among all samples. This result can be explained by two reasons as follows. First, as discussed above, the dominant chemical etching by the bias power of 2.5 W rather than physical etching resulted in the rough sidewall surface, which could improve light extraction

efficiency via sidewall emission. Recently, Kumabe et al. reported that as ICP-RIE etching bias decreased, etching-induced damage such as occurring isolated nitrogen vacancies was effectively suppressed [37]. Furthermore, Zhu et al. also found that low-etching-induced damage at the sidewall played an important role for improving the EQE of micro-LEDs via the neutral beam etching technique [38]. There two results suggest that the highest EQE with 2.5 W can be associated with the combined effects of increasing light extraction efficiency and suppressed etching damage at the sidewall. Therefore, it is concluded that two parameters that affects EQE (i.e., SRH-non radiative recombination, sidewall damage and light extraction efficiency) should be enhanced to realized high performance of micro-LEDs.

3.6 Appendix

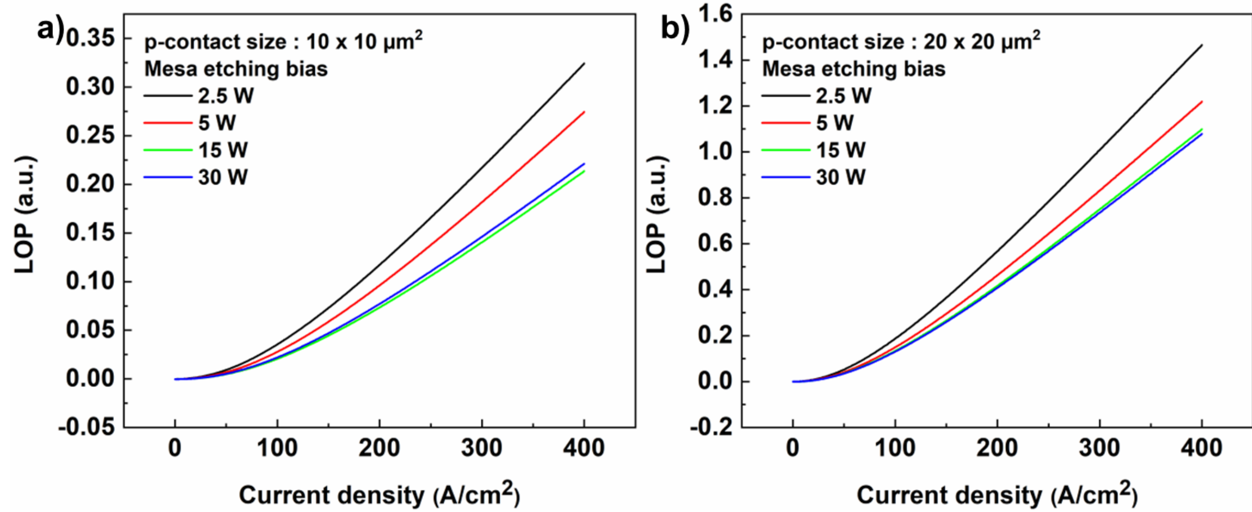

Figure 3.15. Etching bias dependent light output as a function of the current density measured by Si photodiode. a) 10 × 10 μm^2 b) 20 × 20 μm^2 size micro-LEDs.

In this appendix, we further discuss that the effect of polarization suppressed epitaxial wafer. **Figure 3.15** displays the L-I curves corresponding to etching bias measured at the relatively low current region. Light output (LOP) was measured by a silicon photodiode (Hamamatsu, S1337-1010BQ) placed under the sample and collected the light within around a 60° half-angle cone. It was observed that the LOP of 2.5 W etched one was highest in both 10 × 10 μm^2 and 20 × 20 μm^2 sizes. Interestingly it was observed that the L-I curves had a superlinear shape regardless of the etching bias. We speculated that this result may be caused by the suppressed polarization effect. For example, Lee et al. reported that $In_{0.1}Ga_{0.9}N$ quantum barrier (QB) layer can reduce polarization mismatch between the InGaN QWs than conventional GaN QB layer due to the reduced internal electric field (slope of band edges),

resulting in the superlinear LOP and less EL wavelength shift [39]. Additional evidence of suppressing the polarization effect can be evaluated by **Figure 3.16a and b.** It was observed that the EL peak wavelength shift. as approximately 7 nm blue shift even though injected current dramatically changed from 0 to 10,000 A/cm^2.

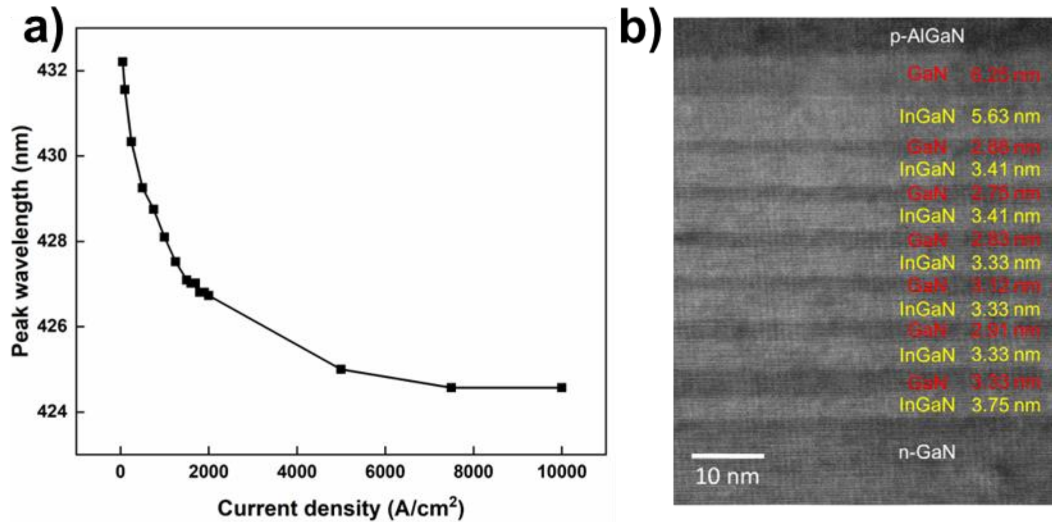

Figure 3.16. a) EL peak wavelength from 0 to 10,000 A/cm^2 showing ultra-small peak shift. b) Cross-sectional HAADF-STEM observed at the MQWs indicating a thin quantum barrier.

We further investigated that the EL peak shift of 10 × 10 μm^2 scale blue micro-LED fabricated by commercial blue LED wafer that has thick quantum barrier as shown in **Figure 3.17a**. Compared to the Figure 3.16, EL peak shift dramatically changed around 18 nm from 2 A/cm^2 to 250 A/cm^2, which was very large due to the polarization effect.

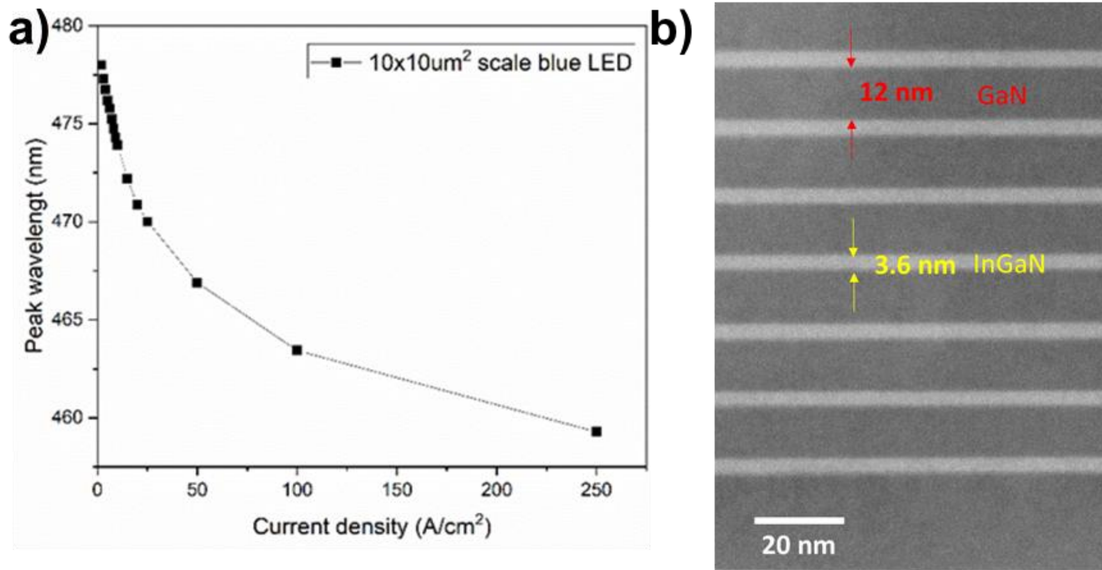

Figure 3.17. a) EL peak shift as a function of current density. b) Cross-sectional HAADF-STEM image indicating thick QB.

The main difference between Figure 3.16b and 3.17b is the QB thickness. According to the Lin et al., the band slope in the quantum well (QW) indicating the polarization effect is defined by Eq. (4) [40].

$$E_{QW} \approx E_0 \frac{1}{1+(\frac{t_{QW}}{t_{QB}})} \tag{4}$$

Where E_0 is constant, t_{QW} is the QW thickness, and t_{QB} is the QB thickness. Therefore, the slope of electrical field in the QW could be attributed to the ratio of t_{QW}/t_{QB}. Although the ratio could increase with increasing t_{QW}, it can make larger spatial separations of elections and holes in the QW, which is called Stokes-like shift [41]. Only one solution is to decrease t_{QB}, which could alleviate the slope of electrical field in the QW.

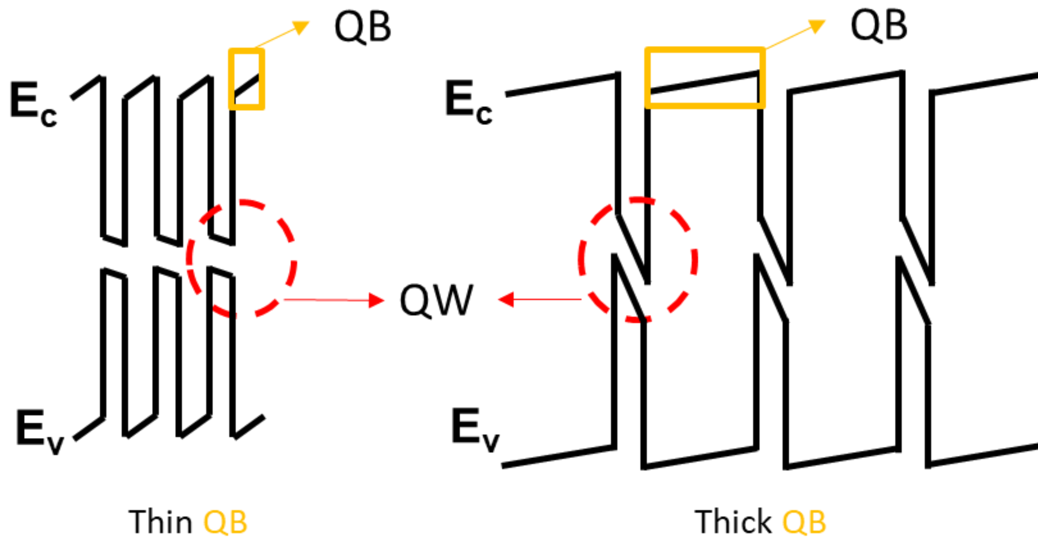

Figure 3.18. Schematic of band slope of quantum well depending on the thickness of quantum barrier.

As described in **Figure 3.18**, This thin quantum barrier can lead to the alleviation band slope in the quantum well and make the relaxed polarization-induced electric filed, resulting in the less EL peak shift and superlinear curve at the low current density regime [39,40,42]. Moreover, as shown in Figure 3.13 and 3.14, maximum EQE occurred at the relatively high current density and showed less efficiency droop than the commercial LED [33], which might be caused by uniform hole distribution in QW due to the alleviation band slope [39,40,42]. Although the specially designed thin QB wafer has relatively low efficiency at the low current region, it may be suitable for the outdoor display requiring high brightness and high LOP such as AR or projection display [11-12].

For collecting the LOP, we used two different equipment. A silicon photodiode (Hamamatsu, S1337-1010BQ) placed under the sample. The absolute LOP and the EL intensity were measured by an integrating sphere (Ocean Insight, FOIS-1) connected to a miniature spectrometer (Ocean Insight, FLAME-S) for EQE. Since the silicon photodiode and the integrating sphere were placed under the sample, it might not collect all light emission because the light generated at MQW has 4π geometry (e.g., sphere shape). Anaya et al. suggested that the measurement system placed under the sample can collect in the forward-emitting hemisphere through use of an integrating sphere in a 2π geometry and a spectrometer as shown in **Figure 3.19** [43]. We believe that our integrating sphere also collected the photons in the forward-emitting hemisphere, indicating around half of the photons we measured. We also agree that this method is not enough to evaluate precisely and quantitively. However, this method may allow for a relative analysis of the effect of etching bias.

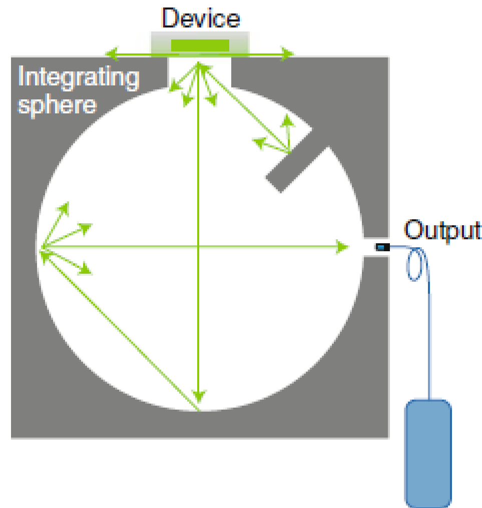

Figure 3.19. Integrating sphere placed under the sample. This method allows us to collect the light in the forward-emitting hemisphere [43].

3.7 Summery

In conclusion, it was investigated that the influence of dry etching conditions on the performance of blue micro-LEDs with reduced quantum confined Stark effect epitaxial layer. The etched n-GaN and sidewall surface differed depending on the etching bias. Especially, the bias power of 2.5 W resulted in the rough surface due to the chemical reaction between the Cl_2 etching gas and the GaN epi layer rather than ion bombardment, where the chemical reaction could effectively suppress the plasma damage on the n-GaN and sidewall surface and thus, improve the I-V characteristics such as the leakage current and ideality factor. Meanwhile, it was demonstrated that rough sidewall morphology could improve light extraction efficiency through FDTD simulations and light output curve. The mechanism of surface roughing with low etching bias has been further demonstrated by SEM and CL images via various substrates that has different dislocation density, where the higher dislocation, the rougher surface. In addition, a thin QB produced low efficiency droop and a small EL peak shift even current reached approximately 10,000 A/cm^2 due to suppressed polarization effect. From EQE curve, it was observed that the peak EQEs were different depending on the etching bias, where it was evaluated without passivation layer; thus, low etching bias suggests not only the increasing light extraction efficiency but also suppressing sidewall damage. Therefore, optimizing dry etching conditions is crucial step for high performance of micro-LEDs, and polarization-suppressed LED wafer could be applied to the realization of high-brightness displays.

3.8 References

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Chapter 4

Interplay of sidewall damage and light extraction efficiency of micro-LEDs

4.1 Introduction

Since 1962, III–V compounds light emitting diodes (LEDs) have been demonstrated their outstanding properties and developed by many researchers. In turn, the world is now becoming brighter via this technology [1-2]. LEDs become core elements of next-generation display, for virtual reality (VR), augmented reality (AR) that are attracting attention as a next-generation display [3-7]. These systems —a short viewing distance between eyes and display—require a high pixel per inch (PPI) density rather commercial display in consideration of the eye resolution, meaning that a lot of pixels should be placed within a limited area [8-9]. For example, since lightweight non-obstructed glasses are desired, 10000 PPI are needed (assuming a 4 k display on 1 cm^2 chip), 10000 PPI would translate to 2.5 μm per pixel. Therefore, a small pixel size is essential for ultra-high PPI display. So far, relatively large-size LEDs have been widely used; however, shrinking LEDs to these small dimensions and then called micro-LEDs (μLEDs) is very challenging, especially retaining the radiative performance. One strong contribution to degradation is to the plasma induced sidewall damage [10-13]. Recently, Smith et al. reported that under 5 μm and smaller μLEDs extremely suffer sidewall damage, resulting in low external quantum efficiency (EQE) and high peak current density (J_{peak}) [14]. Finot et al. quantized the sidewall damage induced by an inductive coupled plasma reactive ion etching (ICP-RIE) through spatially

resolved time-correlated cathode luminescence and reported a width of approximately 1 μm [15]. Therefore, μLEDs less than 2 μm would be entirely corrupted by sidewall damage. On the other hand, it was reported that smaller mesa has indeed high light extraction efficiency despite of relatively large sidewall damage, which is caused by an increased light extraction via the sidewall [16-17]. Because light extraction efficiency is independent to sidewall damage, [18] an improvement in light extraction efficiency could somewhat alleviate the decrease in radiative efficiency form sidewall damage for small size μLEDs.

The display companies are now using the diamond pixel structure as a strategy, which is found in current display technology such as Galaxy Note 20 and iPhone 13 [19-20]. This structure considers not only high PPI but also efficiency. To active the highest PPI, each pixel design should be different such as square, stripe, and circular for placing pixels in the limited area. In addition, each pixel size and density are dependent on the emission color. For example, the green subpixel can be smaller and densely populated than the blue and especially red subpixel due to the different sensitivity of the human eye and efficiency of the emitters [21-22].

Regarding above issues, EQE, PPI, and, luminous efficiency, the studying various LED designs are important and pathway to realize high-efficient and high-PPI μLEDs display. In this study, we attempted to demonstrate the designing μLEDs can manipulate their sidewall damage and light extraction efficiency that changes μLEDs properties. Furthermore, we investigated the effect of surface recombination on the performance of μLED via tetramethylammonium hydroxide solution (TMAH) treatment and J_{peak} based on the experimental results. Our results guide how to realize the highest EQE for μLED display.

4.2 Device structure and fabrication process

To investigate the effect of the peripheral length on the performance of micro-LEDs, four different mesa structures were designed as shown in **Figure 4.1**, but all mesa structures had a same 400 μm^2 mesa area. Circular, square, short stripe, and long stripe have 70.9, 80, 100, and 170 μm of peripheral length, respectively.

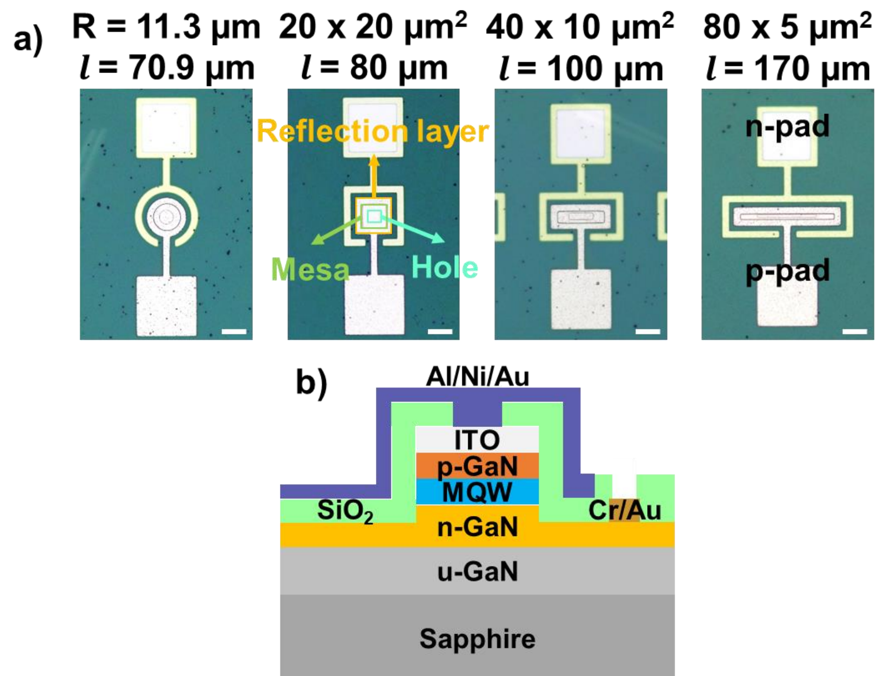


Figure 4.1. a) 400 μm^2 mesa scale designed micro-LEDs with four different mesa geometries. Scale bars are 20 μm. b) Cross sectional of schematic of designed micro-LEDs.

All devices were proceeded by a standard blue LED wafer grown on c-plane sapphire. **Figure 4.2.** shows the SIMS data for doping concentration and In, Ga, and Al ratio for each

layer. To suppress the overflow of electron into p-GaN layer, p-AlGaN layer was grown before p-GaN growth.

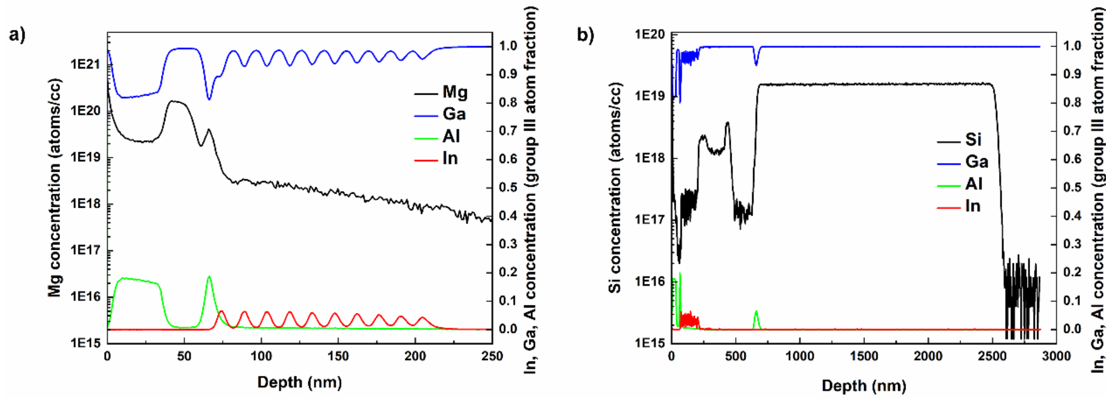


Figure 4.2. SIMS data for confirming a) Mg concentration and b) Si concentration. Additionally, 10 pair MQWs is additionally observed.

The epi wafer was annealed at 700 ℃ for 5 min in N_2 ambient by rapid thermal annealing (RTA) to activate p-GaN layer. A transparent indium tin oxide (ITO) layer around 100 nm was deposited on the p-GaN layer by sputtering system. After that, it was annealed at 600 ℃ for 5 min in N_2 ambient by RTA for ohmic contact between ITO and p-GaN layer. The various mesa shapes were defined by using ICP-RIE. ITO and epi structure were etched down until n-GaN layer was revealed, where an ICP power, bias power, Cl_2, and pressure were 150 W, 15 W, 30 sccm, and 2.0 Pa, respectively. The 100 nm ITO and 700 nm epi were etched by ICP-RIE. After mesa etching, the sidewalls were treated with 25 wt% TMAH at 80 ℃ for 10 min to remove sidewall damage. The n-type ohmic contact (Cr/Au 30/160 nm) was formed by electron-beam evaporation. To form p-electrodes, the mesa was firstly covered by around 400 nm SiO_2 by using plasma enhanced chemical vapor deposition. To connect p-electrodes and ITO, a hole was opened by CF_4 based RIE

process. Where bias power, CF_4, and pressure were 100 W, 15 sccm, and 4.2 Pa, respectively. Finally, an Al/Ni/Au (400/20/160 nm) layer was deposited as p-electrodes on ITO layer by using electron-beam evaporation. An Aluminum layer worked as a reflection layer, leading that sidewall and top light emission move to the bottom. Therefore, all light emission was collected under the sample [23]. **Figure 4.3.** shows the cross-sectional image of micro-LEDs observed by SEM. It can be seen that all mesa area was covered by Al/Ni/Au metals. Because first Al layer has over 90 % reflectance under 500 nm wavelength, all emitted light could move under the sample.

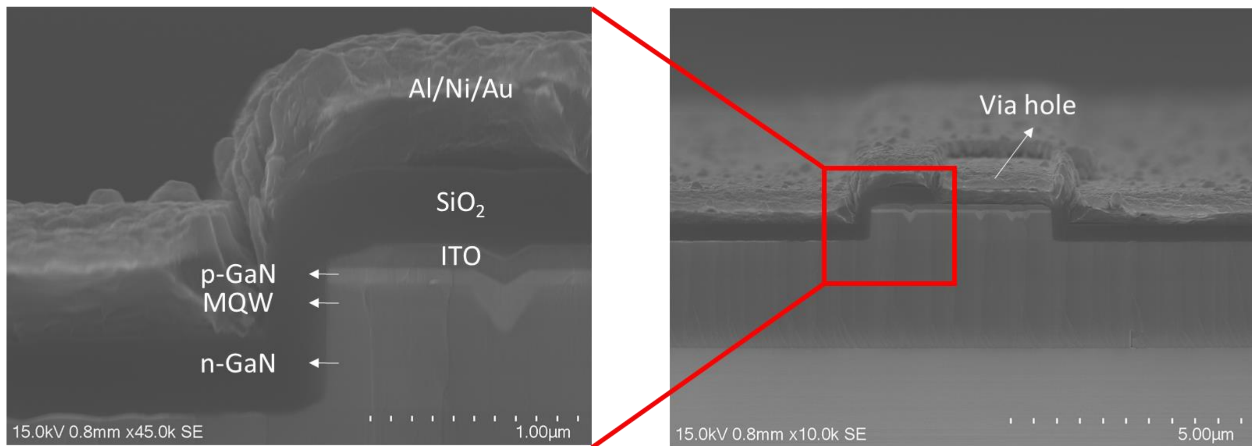


Figure 4.3. Cross sectional SEM image of fabricated micro-LEDs.

4.3 Peripheral length dependent absolute EQE

The optical properties of all samples were investigated by an integrating sphere (Ocean Insight, FOIS-1) that was placed under the sample. An integrating sphere was connected to a spectrometer (Ocean Insight, FLAME-S) shown in **Figure 4.4**. The light output (P_{out}) and electroluminescence (EL) spectra were measured in the darkroom and at room temperature.

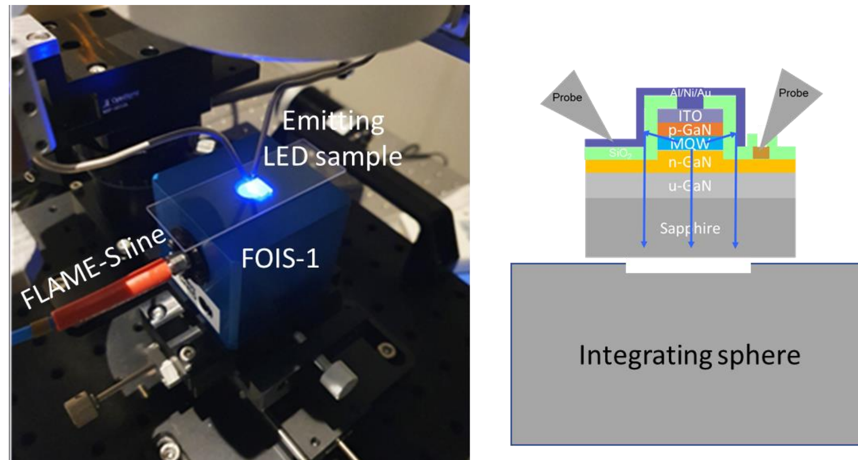


Figure 4.4. An integrating sphere for analyzing optical performance of micro-LEDs.

To evaluate the performance of designed micro-LEDs, the EQE was calculated with the parameters of P_{out}, EL peak (λ_{peak}), and injected current (I). The EQE form is given by [16]

$$EQE(\%) = \frac{P_{out}\lambda_{peak}}{I} \times \frac{e_0}{hc} \times 100 \quad (1)$$

In Equation (1), λ_{peak} was used because all EL spectra had a gaussian formation. e_0, h, and c are elementary charge, Planck constant, and light speed in vacuum, respectively. All EQE data were averaged by eight devices for each sample. To obtain data reliability, all measured data are displayed in **Figure 4.5**.

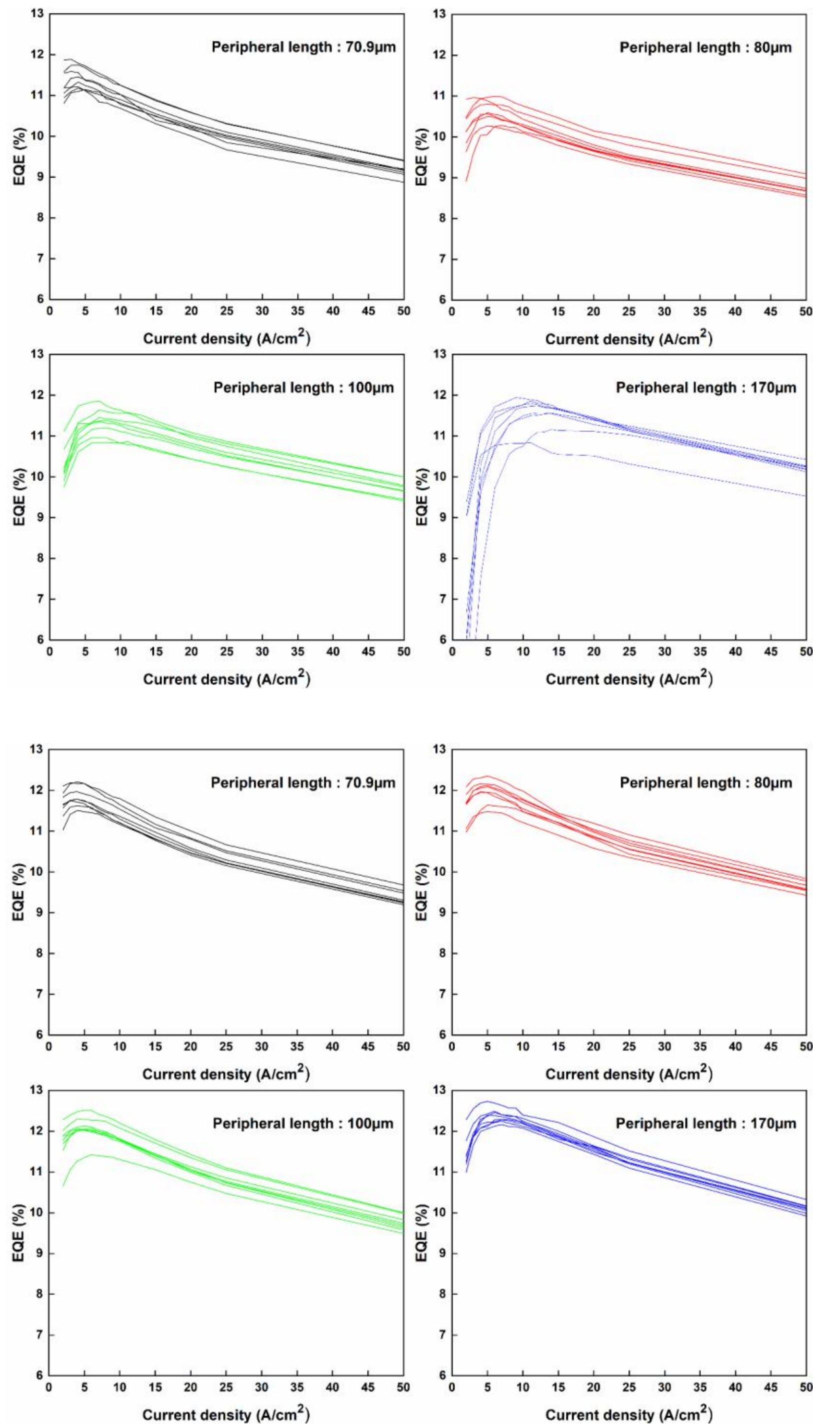


Figure 4.5. Absolute EQE as a function of current density for each peripheral length. Top) without TMAH etching. Bottom) with TMAH etching.

Because all samples were fabricated on the same wafer (i.e., same epi structure), the emitted peak wavelength for each device was no significant difference as shown in **Figure 4.6.**, which may indicate that the peripheral length does not affect the EL peak position. Since this wafer had around 13 nm quantum barrier thickness, the piezoelectric filed was induced in the quantum well, which led the quantum confined Stark effect (QCSE) with increasing injection currents.

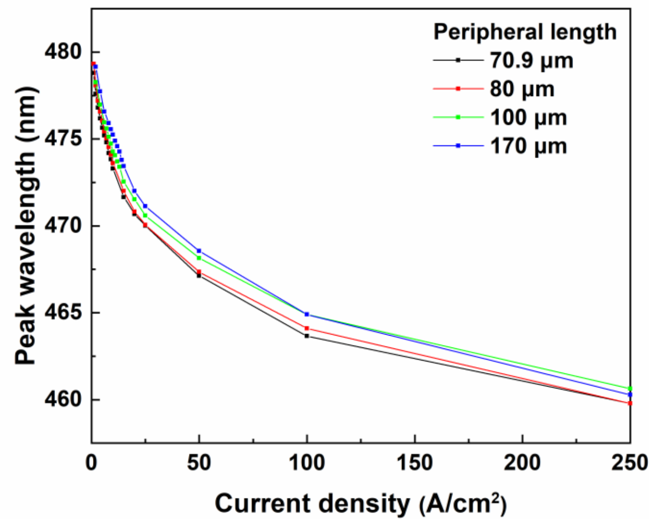


Figure 4.6. EL peak wavelength as a function of injected current density.

The peak EL wavelength shifted from 479 nm (at 1 A/cm^2) to 460 nm (at 250 A/cm^2) regardless of the mesa peripheral length. This peak shift demonstrates that the peripheral length does not affect the peak shift, which further indicates that QCSE only depends on the epitaxial structure and carrier density. Therefore, all samples showed similar peak shift regardless of shape of micro-LEDs.

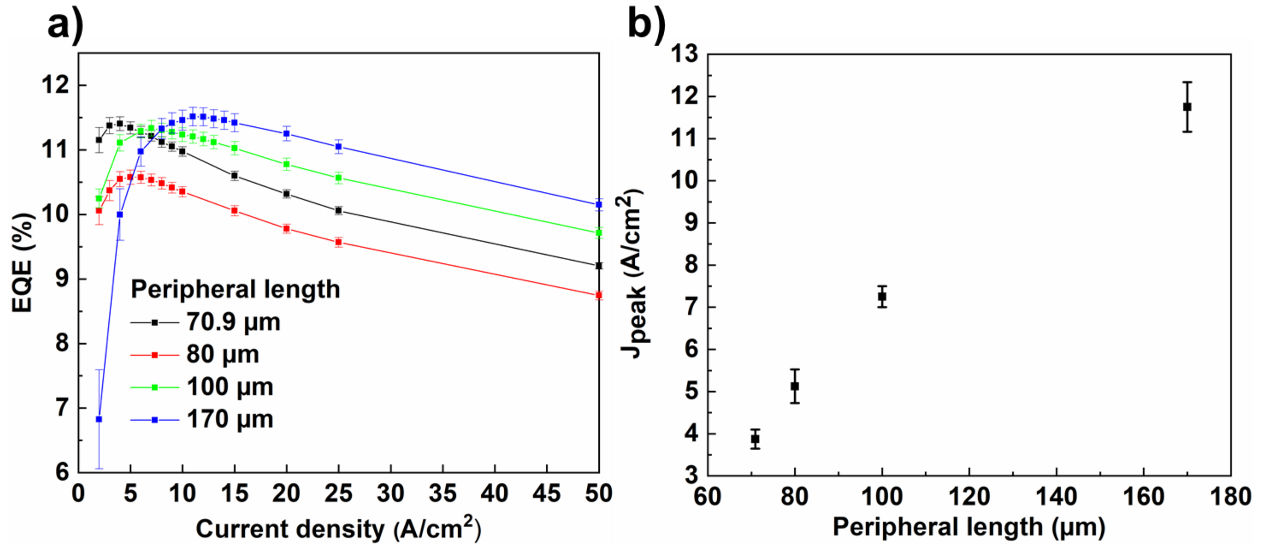


Figure 4.7. a) Mesa peripheral length dependent absolute EQE without TMAH treatment. b) Extracted J_{peak} from absolute EQE curve.

Average EQE curves before TMAH treatment had a different maximum EQE and J_{peak} as shown in **Figure 4.7**a. Because the mesa area was fixed as 400 μm^2, only the different peripheral length of mesa affects EQE characteristic. To clarify the effect of peripheral length, ABC model of EQE can be applied to Figure 4.7a. The basic ABC model is defined with three recombination parts:[18]

$$\boldsymbol{EQE = IQE \times \eta_e = \frac{Bn^2}{An+Bn^2+Cn^3} \times \eta_e} \tag{2}$$

A is Shockly-Read-Hall (SRH) non-radiative recombination, B is radiative recombination, C is Auger non-radiative recombination, n in the carrier density, and η_e is light extraction efficiency. Equation (2) assumes the ideal injection efficiency ($\eta_J = 1$). Equation (2) can provide the information for maximum EQE, and J_{peak} by differentiating it and setting $dEQE/dn = 0$ then, one obtains

$$\boldsymbol{n_{peak}} = \sqrt{\frac{\boldsymbol{A}}{\boldsymbol{C}}} \tag{3}$$

The current density at maximum EQE can be obtained via the current density form from the denominator of Equation (2). By putting Equation (3) into the denominator of Equation (2) one obtains

$$J_{peak} = e_0 w\left(An_{peak} + Bn_{peak}^2 + Cn_{peak}^3\right) = e_0 wA\left(\frac{B}{C} + 2\sqrt{\frac{A}{C}}\right) \approx e_0 wA\frac{B}{C} \tag{4}$$

Where w is the total thickness of quantum wells. Because all devices were fabricated on the same wafer, therefore, the parameters of QWs as well as B and C should be same for all devices. By assuming the B and C parameters as 10^{-12}cm^{3}s^{-1} and 10^{-32} cm^{-6}s^{-1}, B/C ~10^{20} cm^{-3} is approximately ten times larger than $\sqrt{A/C}$ ~ 10^{19} cm^{-3} [24]. Thus, J_{peak} can be approximated as $e_0 wAB/C$. Because all devices must have same parameters (w, B, and C), it is explained that J_{peak} is directly proportional to the SRH non-radiative recombination. Figure 4.7b shows the J_{peak} as a function of the peripheral length of mesa. The observed J_{peak} increased as peripheral length increased, with a J_{peak} of 3.88 A/cm^2, 5.13 A/cm^2, 7.25 A/cm^2, and 11.8 A/cm^2 for 70.9 µm, 80 µm, 100 µm, and 170 µm of peripheral length. Therefore, it can be inferred that the longer peripheral length, the higher SRH non-radiative recombination because J_{peak} is proportional to the parameter A as described in Equation (4). Additionally, it was confirmed that the longest peripheral length showed quite low EQE at the small current regime (<10 A/cm^2), which further demonstrates that longer peripheral length, higher sidewall damage from dry etching process because SRH nonradiative

recombination is dominant at the low current regime. Finot et al. investigated the sidewall damage length induced by ICP-RIE through spatially resolved time-correlated cathodoluminescence [15]. They observed the lifetime up to 1 µm away from the sidewall is shorter than bulk mesa. Moreover, David et al. investigated that most of the generated carriers are concentrated within a few micrometers [25]. Therefore, it can be assumed that all mesa has a damaged area near all of mesa edge up to 1 µm. **Figure 4.8.** should help to understand the effect of peripheral length on SRH non-radiative recombination.

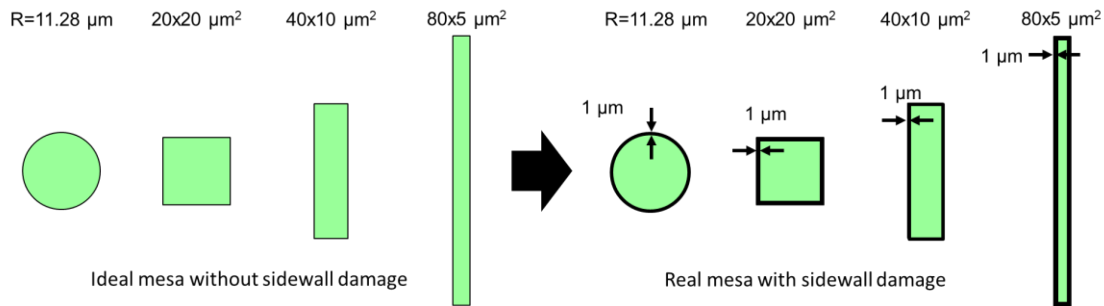


Figure 4.8. Schematic of designed mesa structure with same mesa area. Left) ideal mesa without ICP-RIE induced sidewall damage. Right) real mesa with ICP-RIE induced sidewall damage assumed around 1 µm damage width.

As can be seen, the longer peripheral length (e.g., 80 x 5 μm^2 stripe) the lager sidewall damage area. Following sidewall damage width, J_{peak} and sidewall damage area can be compared in **Table 4.1.**

Table 4.1. The relationship between J_{peak} and sidewall damage area of various peripheral length of mesa.

	Circular	Square	Stripe (40x10 μm^2)	Stripe (80x5 μm^2)
Peripheral length(μm)	70.87	80	100	170
Sidewall damage (μm^2)	67.75	76	96	166
J_{peak}(A/cm^2)	3.88	5.13	7.25	11.8

Although all designed micro-LEDs had a same mesa area of 400 μm^2, the ICP-RIE induced sidewall damage area could change with the peripheral length of mesa. Again, Table 4.1 shows J_{peak} is proportional to the sidewall damage area that is proportional to the peripheral length of mesa. According to Equation (2), EQE is inverse proportional to the SRH-non radiative recombination, parameter A, because parameter A is related to the denominator of EQE equation. However, the peak EQE did not decrease, rather peak EQE increased with the peripheral length of mesa as shown in Figure 4.7a. The peak EQEs were 11.4%, 10.6%, 11.3%, and 11.5% for for 70.9 μm, 80 μm, 100 μm, and 170 μm of peripheral length. Since EQE is proportional to IQE and light extraction efficiency, EQE should be analyzed by separating IQE (SRH-non radiative recombination) and light extraction efficiency to clarify the relationship between IQE and light extraction efficiency. To determine IQE and light extraction efficiency, we fitted the normalized EQE curves by peak EQE following Equation (5) as below: [26-27]

$$\frac{EQE(x)}{EQE_{peak}} = \frac{P+2}{P+\frac{1}{x}+x} \qquad (5)$$

x is the dependent variable $x = \sqrt{L/L_{peak}}$ with *L* is light output and L_{peak} is the light output at peak EQE. The peak IQE can be defined by putting Equation (3) into Equation (2)

$$\boldsymbol{IQE_{peak}} = \frac{\frac{B}{\sqrt{AC}}}{\frac{B}{\sqrt{AC}}+2} = \frac{P}{P+2} \tag{6}$$

The fitting parameter *P* is related to the parameter of A, B, and C recombination rate from Equation (2) as $P = B/\sqrt{AC}$. Because light extraction efficiency is independent parameter from A, B, and C, it is canceled out by normalizing as Equation (5). The example of fitting model is available in **Figure 4.9**.

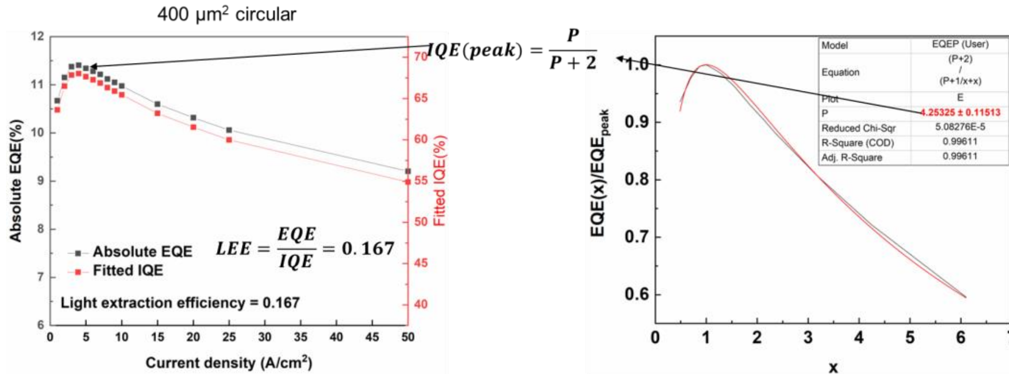


Figure 4.9. Example of EQE fitting via parameter P.

By fitting the Equation (5) with formation of EQE(x)/EQE$_{peak}$ verse *x*, the parameter *P* can be obtained as shown in Figure 4.9. By putting the obtained value of parameter *P*, the IQE can be plotted. Finally, light extraction efficiency is given by $\eta_e = EQE_{peak}/IQE_{peak}$. **Figure 4.10** shows the obtained peak IQE and light extraction efficiency from fitting via Equations (5) and (6) for different peripheral length of mesa.

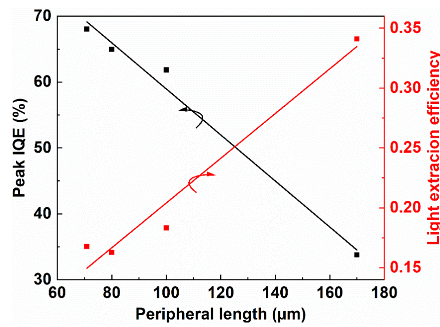
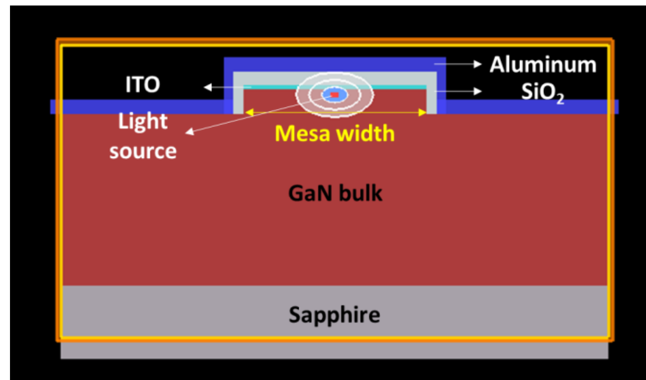


Figure 4.10. Peripheral length dependent peak IQE and light extraction efficiency obtained by fitting via Equations (5) and (6).

Consistent with an increasing J_{peak}, the fitted peak IQE decreases with increasing peripheral length because IQE is inverse proportional to SRH-non radiative recombination. However, light extraction efficiency increases with increasing peripheral length, which indicates the emitted light can move out more through the sidewall. In addition, it can be inferred that light extraction efficiency has a strong effect on the EQE because the longest peripheral length had highest EQE at the relatively high current region and highest peak EQE even though longest peripheral length was confirmed it had highest SRH-non radiative recombination. Thus, changing the micro-LEDs geometry to a narrow stripe increases light extraction efficiency. To further investigate the light intensity at the sidewall, we used Finite-difference time-domain simulation (FDTD, Lumerical software). To save a simulation time, simulation was proceeded by two-dimensional structure. More detail simulation condition is described in **Figure 4.11**. The difference in each simulation



Mesa width : 5, 10, 20, and 22.6 μm
Mesa thickness : 700 nm
GaN bulk thickness : 4.7 μm
ITO thickness : 100 nm
Al thickness : 400 nm
SiO_2 thickness : 360 nm
Light source wavelength : 470 nm

Figure 4.11. Detailed 2D FDTD simulation condition for confirming light intensity at the sidewall.

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was the mesa width that was 5 μm, 10 μm, 20 μm, and 22.6 μm corresponding to 170 μm, 100 μm, 80 μm, and 70.9 μm of mesa peripheral length respectively. **Figure 4.12** shows the light field intensity near the mesa sidewall. It was observed that the light field intensity increased at the sidewall as mesa width decreased, meaning that the emitted light propagation is more concentrated at the sidewall as LED mesa becomes the smaller and narrower. Therefore, as LED structure becomes narrow (i.e., small size), light extraction efficiency relatively increases due to increasing the sidewall emission. Since the mesa was covered by a top aluminum reflection layer, the light field more concentrated on the bottom. This simulation data suggests that decreasing IQE induced by ICP-RIE sidewall damage can be compensated by the increasing light extraction efficiency via the concentrating sidewall emission.

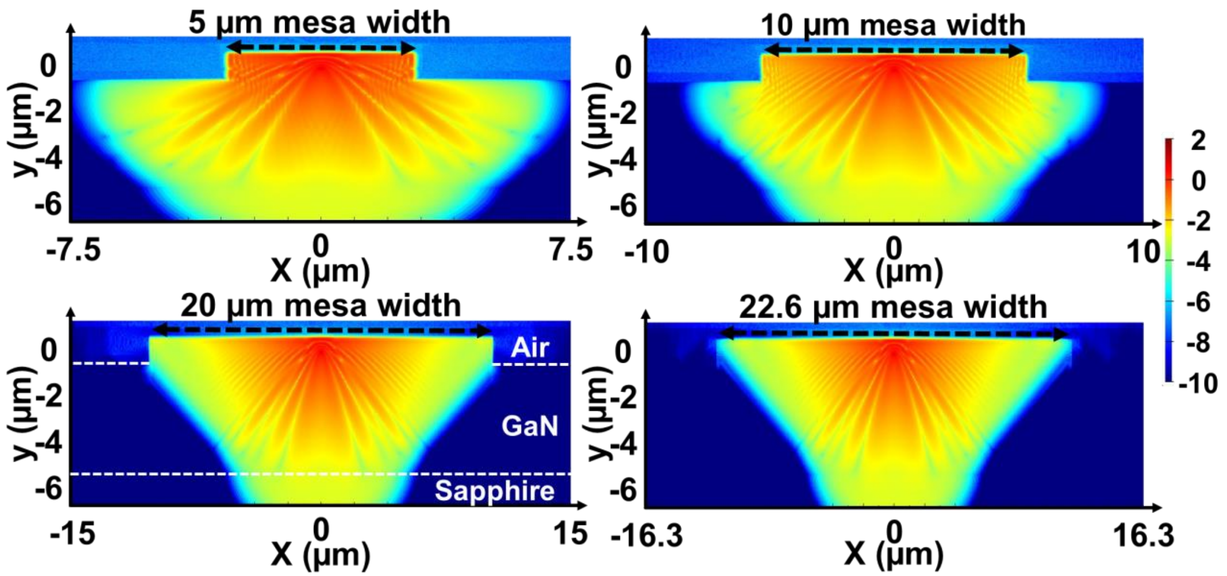

Figure 4.12. Simulated light field intensity at four different mesa width. The field intensity at the sidewall enhances with decreasing mesa width, indicating that the smaller mesa, the higher light intensity.

Meanwhile, Guo et al. reported that an interdigitated mesa structure (i.e., a large mesa sidewall area) leads to better light extraction via sidewall [28], which agrees to our result on light extraction efficiency. Ley et al. recently reported that for a series of cone shaped micro-LEDs the peak EQE strongly increased despite sidewall damage, due to the increasing light extraction via the sidewalls for smaller mesa [16]. These reported data confirm again our analysis with EQE, J_{peak}, and FDTD simulations that an increasing the light extraction efficiency can compensate the decreasing IQE. Now, it is clearly understood that the IQE and light extraction efficiency changes with the peripheral length of mesa as shown in Figure 4.10. For fixed mesa area as 400 μm^2, the longest stripe structure showed the highest EQE at a high current density in the efficiency droop regime. In this efficiency droop regime, the SRH-non radiative recombination, An, can be negligible and

Auger losses, Cn^3, dominate the IQE in Equation (2). Therefore, the high light extraction efficiency becomes important to increase the EQE for shirking micro-LEDs size.

4.4 Influence of surface recombination on the EQE

Because III–N based LED needs to take an ICP-RIE process for mesa structure, the plasma induced sidewall damage cannot be avoided, which makes the surface recombination at the sidewall. So far, relatively large size III–N based LED (> 100 µm) does not need to consider the surface recombination due to low surface recombination velocity than other III–Vs LEDs as shown in **Figure 4.13**.

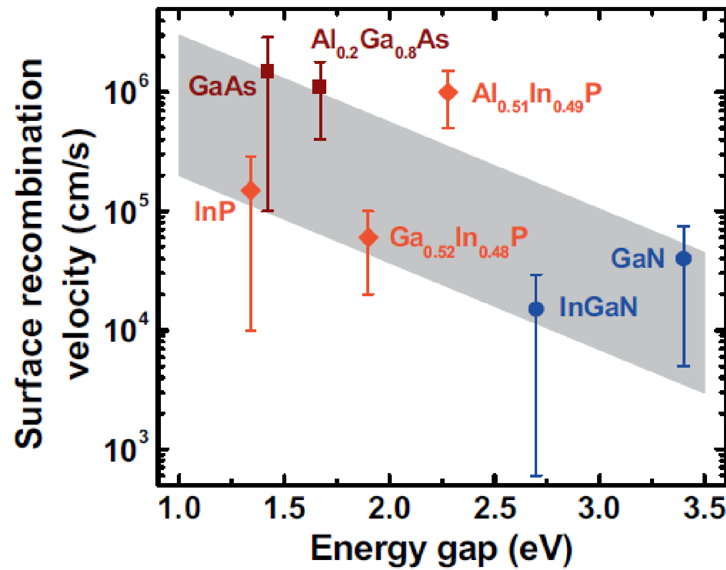

Figure 4.13. Surface recombination velocity of various III–Vs materials. Typically, III-Nitrides have low surface recombination velocity, which less affects the performance of large size III-nitride LED [29].

However, for small size LED surface recombination velocity becomes important since more carriers can move to the sidewall and thus, it will recombine as a non-radiation. **Figure 4.14** well describes the recombination process in LED device.

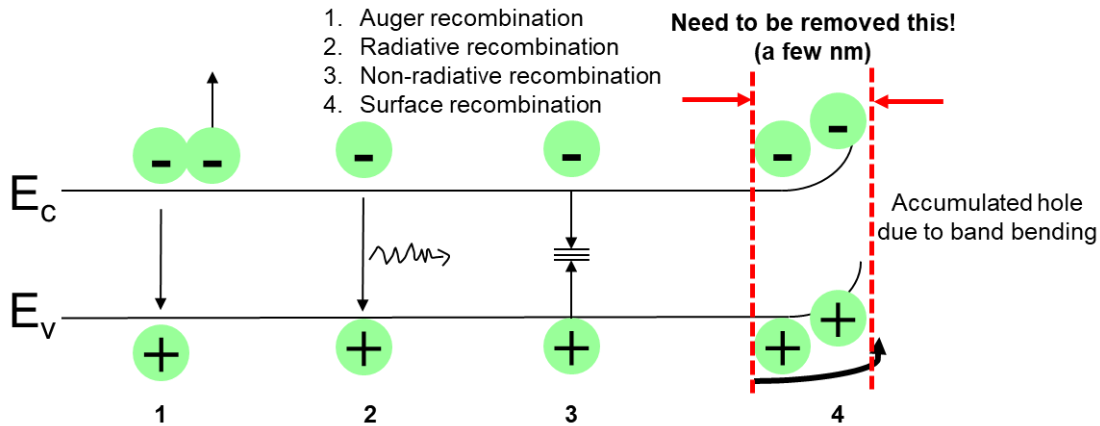

Figure 4.14. Schematic of four recombination process in III-nitride LED.

In general, there are four different recombination process in III-nitride LED. Auger recombination, radiative recombination, non-radiative recombination, and surface recombination. Auger recombination is electrons or holes that are excited into higher energy levels within the same band, which is strong in low energy band gap materials [30] Radiative recombination occurs when electrons in the conduction band and holes in the valence band recombine and the energy is emitted as a photon. Non-radiative recombination is mainly related to the defects in the semiconductor such as point defect and dislocation. Because of this, the electrons cannot recombine with the holes rather it is trapped into the defects. Therefore, non-radiative recombination as well as auger recombination reduce the luminescence efficiency in LED. Additionally, surface recombination induced at the etched surface due to the surface disorder about a few ten nm. also leads the carrier loss, which degrades the radiative recombination. For example, because of generated dangling bonds at the sidewall, the surface depletion region will be introduced, making the surface band bending. This surface band bending makes accumulation of the hole at the surface depletion region in the sidewall, which leads non-radiative surface recombination [31]. The surface recombination

becomes strong as LED size decreases. **Figure 4.15** explains the LED size dependent surface band bending and trapped holes proportion.

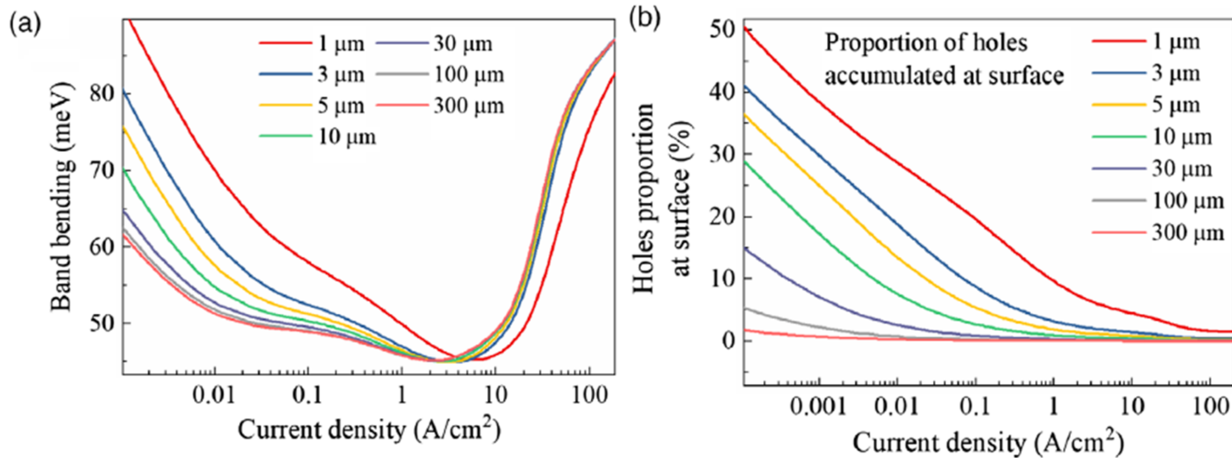

Figure 4.15. Size dependent a) band bending, b) trapped holes proportion at the sidewall [31].

As described in Figure 1.8, the smaller LED, the larger sidewall damaged area. The sidewall damaged area is related to the band bending that occurs due to the surface disorder [32]. Therefore, the sidewall damaged area (i.e., the band bending) becomes relatively large as the LED size decreases because the ratio of moving carrier into the damaged area increases (i.e., relatively small bulk area); The smaller LED much more suffers to the carrier loss, low radiative recombination. Therefore, it is necessary to remove a generated band bending for highly efficient micro-LEDs.

Because band bending occurs due to surface disorder, it need be removed or suppressed. There have been reports over the past few years to remove the damage points (i.e., band bending) by using chemical treatment. Jung et al. reported that the sidewall of AlGaInP red LED can be treated by hydrofluoric acid [33]. This method removes bad atomic arrangement and increase the EQE. Wong et al. etched the sidewall by using phosphoric acid, ultraviolet-ozone, and buffered

hydrofluoric acid [34]. After this process, EQE and wall plug efficiency were improved. Finot et al. also investigated the lifetime of cathodoluminescence after KOH treatment at the sidewall [15]. They showed the lifetime enhanced at the sidewall after KOH treatment, which is caused by the reduced surface recombination. So far, many research groups showed and demonstrated the sidewall etching by chemical treatment is useful to improve the performance of micro-LEDs. However, still no detail report why and how the chemical treatment is effective in terms of the surface recombination. Here, we will explain how much surface recombination is suppressed by chemical treatment as well as the effect of sidewall morphology that changes with chemical treatment on the light extraction efficiency.

As well explained previous in chapter 3, hydroxyl-based etchant such as KOH and TMAH can etch the non-polar or semi-polar GaN surface [35]. These etchants can remove the sidewall damage, meaning that surface recombination is also suppressed due to the removing band banding depletion region. To clarify the effect of hydroxyl etchant, the mesa sidewall was etched by TMAH. **Figure 4.16** shows SEM images of the sidewall in a- and m-plane directions before and after TMAH treatment. Before TMAH treatment, the morphology of the sidewall was not significant different for both directions, which means that ICP-RIE dry etching was uniform in both directions. After TMAH treatment the sidewall morphologies were different in both directions. Because TMAH reveals the m-plane facets, a-plane sidewalls became more vertical with a regular wiggling of m-planes. In addition, m-plane sidewall became very smooth, which indicated TMAH can etch the m-plane direction sidewall. As marked yellow lines in Figure 4.16, both directions revealed the m-plane facets after TMAH treatment. These etching behavior by TMAH demonstrate that TMAH can etch both direction and thus, the surface recombination that is placed on a few ten nanometers width at the sidewall could be removed.

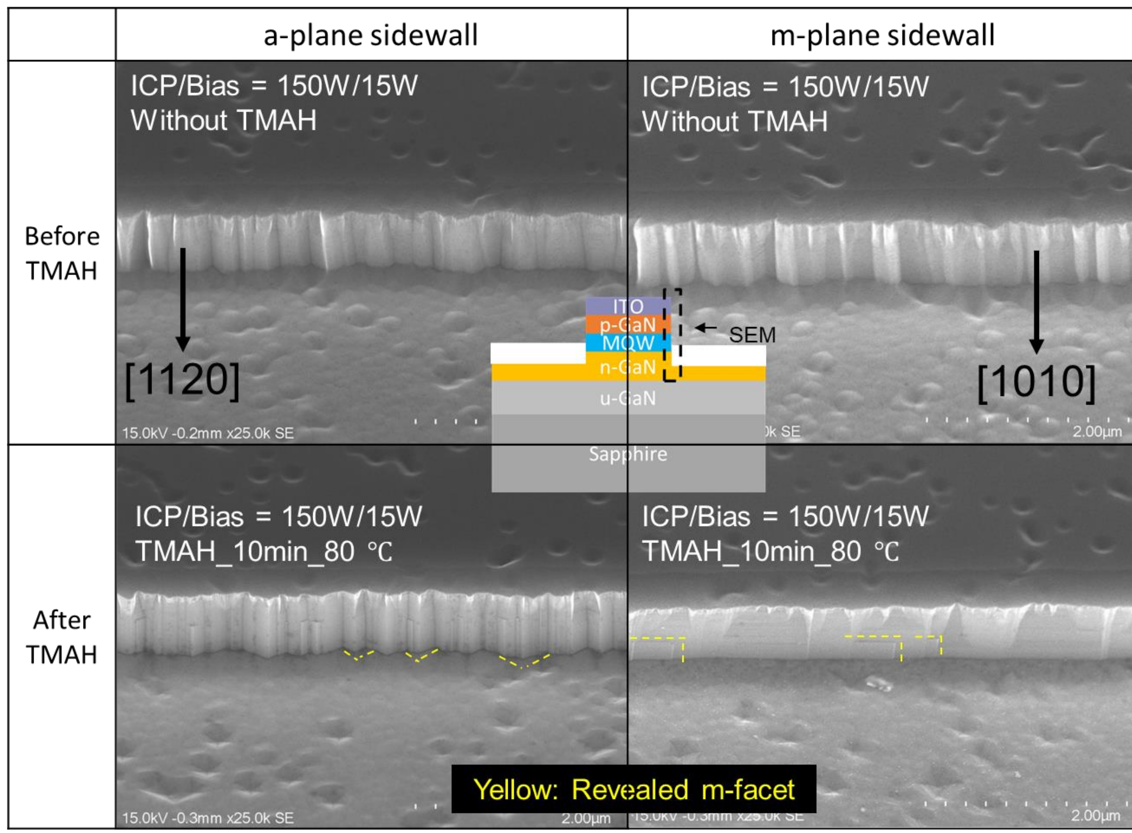

Figure 4.16. SEM images of sidewall morphology of a- and m-plane before and after TMAH treatment.

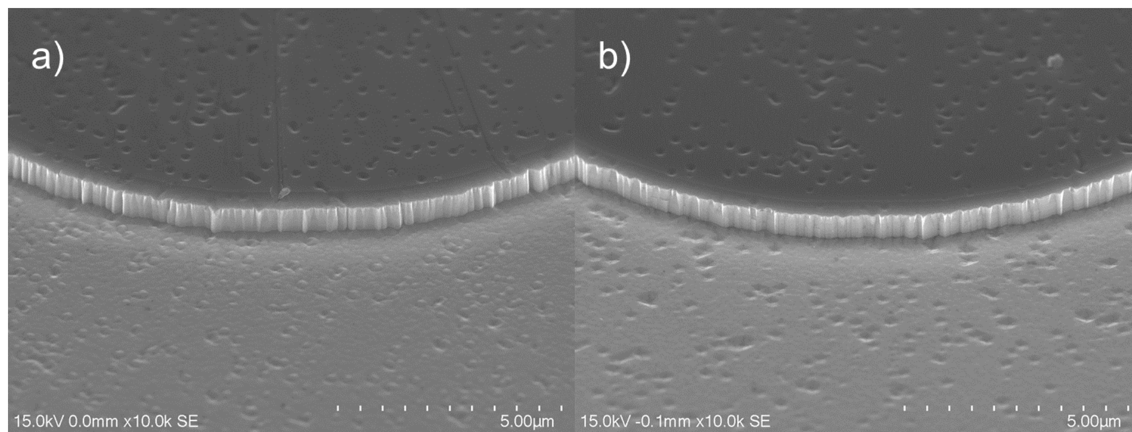

Figure 4.17. SEM images of sidewall morphology of circular shape a) before and b) after TMAH treatment.

Additionally, the sidewall morphologies of circular shape were observed as shown in **Figure 4.17**. As same as in Figure 4.16, the sidewall reacted with TMAH and morphology changed, meaning that regardless of mesa shape, the sidewall could be slightly etched by TMAH. Therefore, etching damage induced surface recombination could be also removed.

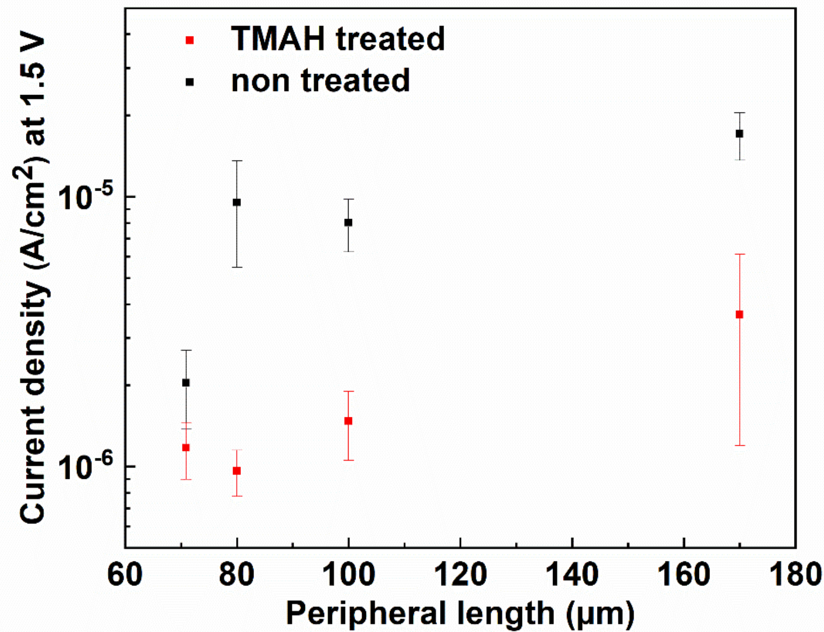

Figure 4.18. The leakage current density measured at 1.5 V before and after TMAH treatment.

To enter additional insight on the effect of TMAH treatment, the leakage current was firstly measured. Because leakage current flows through the sidewall surface, the worse sidewall might increase the leakage current. **Figure 4.18** shows the measured leakage current density at 1.5 V a function of peripheral length before and after TMAH treatment. It was confirmed that TMAH treatment yielded low leakage current density regardless of peripheral length, indicating that the sidewall successfully was etched by TMAH and thus, leakage path was removed together. In addition, it was observed that the leakage current density increased as peripheral length increased, which further demonstrated that leakage current depends on the sidewall damage.

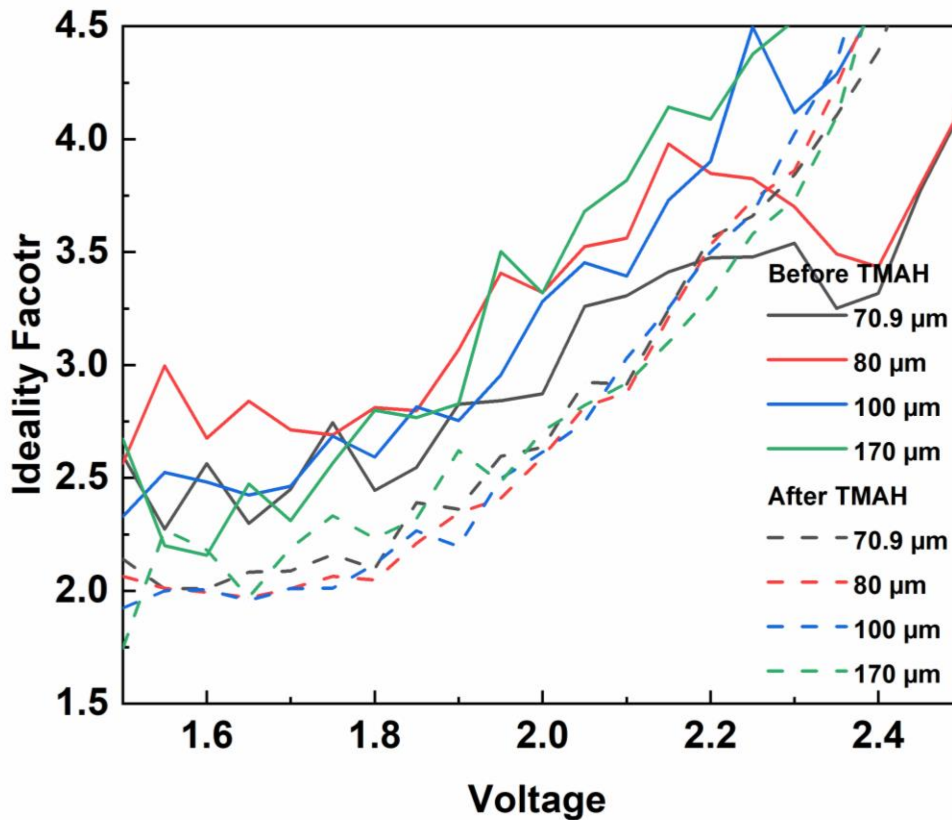

Figure 4.19. The comparison of ideality factor before and after TMAH treatment.

In addition, the observed ideality factor further demonstrates that TMAH can remove the sidewall damage. **Figure 4.19** shows the decreasing ideality factor after TMAH etching. Regardless of the peripheral length, all devices after TMAH decreased the ideality factor compared to before TMAH, which indicates that TMAH improves the electrical performance of micro-LEDs by removing the sidewall surface defect points. Again, the decreasing leakage current and ideality factor clearly demonstrates that the sidewall etching by TMAH enhances the performance of micro-LEDs.

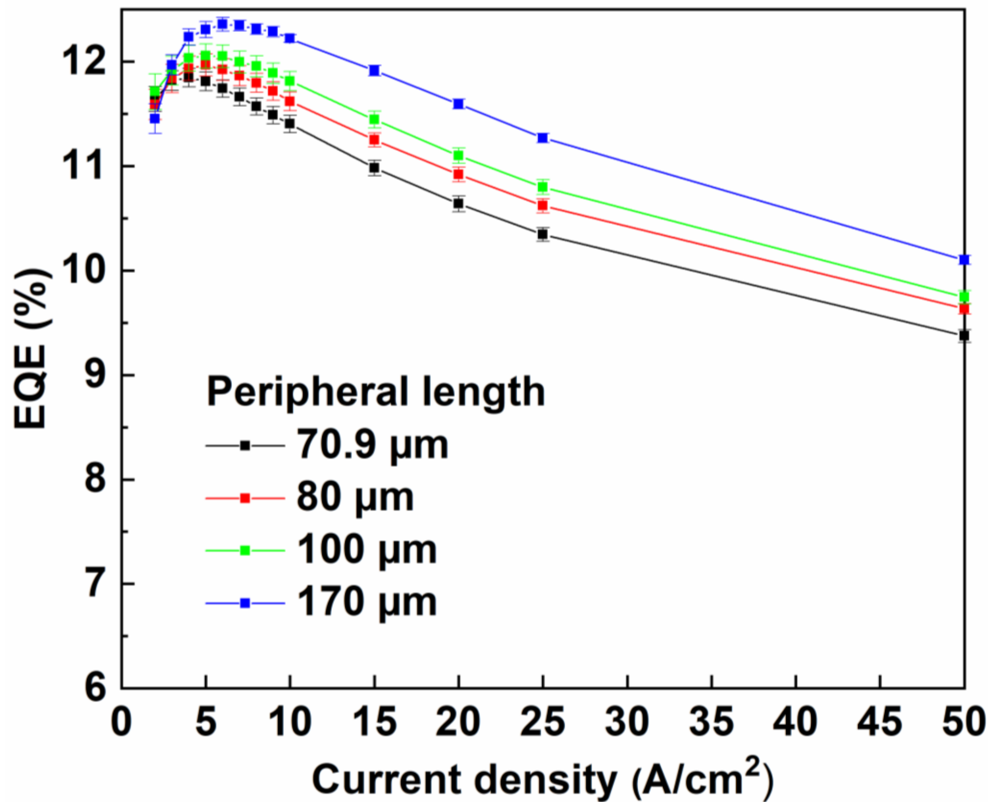

Figure 4.20. Peripheral length dependent absolute EQE with TMAH treatment.

Figure 4.20 shows the absolute EQE curves of TMAH treated micro-LEDs for various peripheral lengths. Comparing to Figure 4.7a, peak EQE of all shapes increased after TMAH treatment. As described in **Table 4.2**, peak EQE enhancement was observed for all peripheral length, which is caused by not only reduced surface recombination but also changed light extraction efficiency. In addition, it was similarly observed that the longer peripheral length the higher EQE at the high current region, which is caused by increasing the light extraction efficiency via sidewall emission. Interestingly, the J_{peak} of all shapes decreased after TMAH treatment, indicating that SRH non-radiative recombination also

decreased because J_{peak} is proportional to the SRH-non radiative recombination. To quantify the effect of TMAH treatment, the surface recombination should be discussed.

Table 4.2. Peripheral length dependent absolute EQE with TMAH treatment.

	Peak EQE			
	Circular	Square	Stripe (40 x 10 μm²)	Stripe (80 x 5 μm²)
Peripheral length (μm)	70.9	80	100	170
Before TMAH	11.4%	10.6%	11.3%	11.5%
After TMAH	11.8%	12.0%	12.1%	12.4%
Enhancement (After/Before)	3.5%	13.2%	7.07%	7.82%

Konoplev et al. suggested that surface recombination can be roughly accounted for in the model of $A'=v\frac{l}{s}$ [36], where v is surface recombination velocity, $\boldsymbol{l}$ is peripheral length of mesa, and $\boldsymbol{S}$ is area of mesa. We followed an approach similar to Konoplev et al.[36] and we expressed the non-radiative recombination rate A adding surface recombination and we obtain.

$$\boldsymbol{A = A_0 + A_s \frac{\lambda l}{S}} \tag{7}$$

Where A_0 is non-radiative recombination rate in the volume, A_s is surface recombination rate, $\boldsymbol{\lambda}$ is carrier diffusion length. By putting Equation (7) into Equation (4) J_{peak} is defined as

$$\boldsymbol{J_{peak} \approx e_0 w \frac{B}{C}(A_0 + A_S \frac{\lambda l}{S})} \tag{8}$$

A recent paper calculated that more than 20% of total holes could be trapped at the sidewall surface when the device size is under 10 μm especially at the low current [31]. This can happen with a surface band bending of around a few ten nm at the sidewall. In addition, the J_{peak} of the different peripheral lengths are same magnitude (i.e., under 10 A/cm^2 scale), and thus the carrier diffusion length, λ, is not change too much.

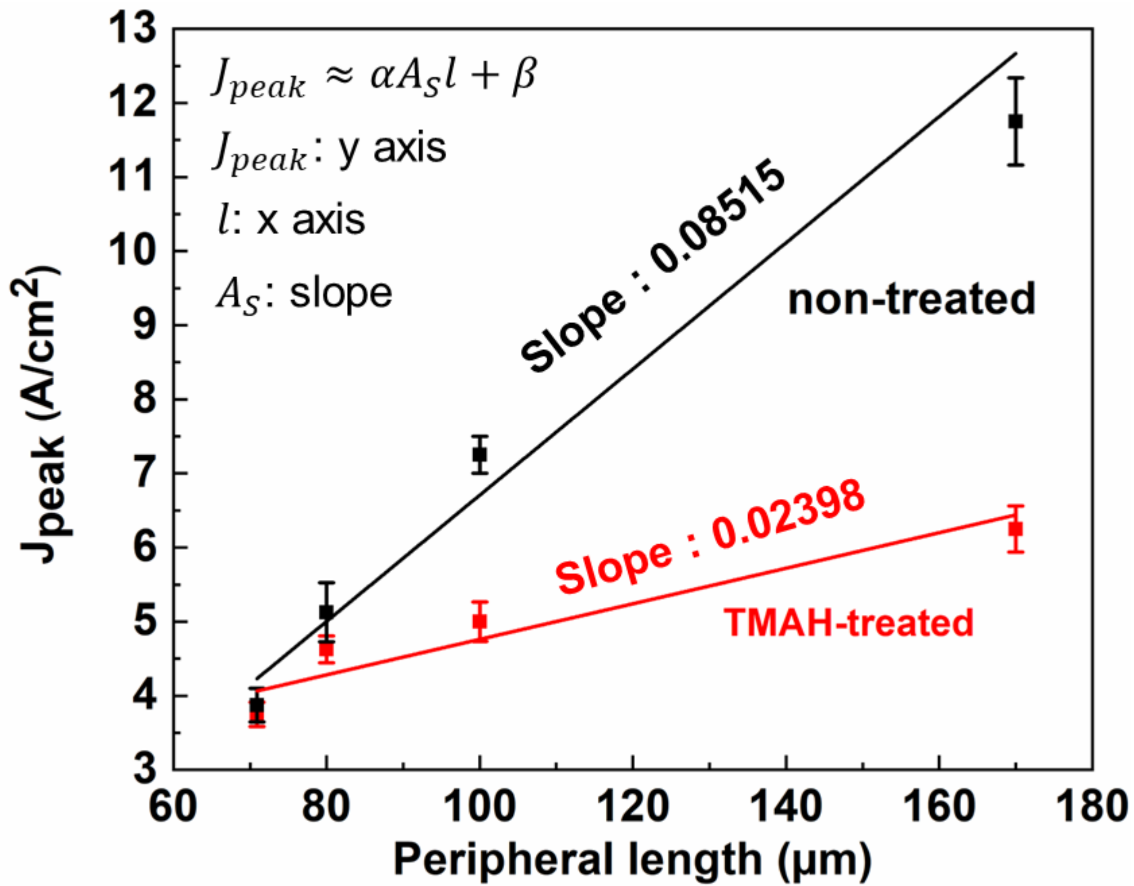

Figure 4.21. Extracted J_{peak} from EQE curves as a function of the peripheral length before and after TMAH treatment.

According to the Equation (8), J_{peak} can be plotted as a function of the peripheral length as shown in **Figure 4.21**. Since the peripheral length, l, is x axis, the surface recombination rate (A_s) is

corresponded to the slope. These slopes were extracted by linear fitting. Before TMAH treatment, the slope was 0.08515; however, the slope decreased after TMAH treatment as 0.02398, indicating that surface recombination reduced, where TMAH treated J_{peak} were 3.75 A/cm^2, 4.63 A/cm^2, 5.0 A/cm^2, 6.25 A/cm^2 for peripheral length of 70.9 µm, 80 µm, 100 µm, and 170 µm, respectively. Quantitatively, it can be calculated that how much TMAH reduces the surface recombination. According to the equation (8), the slope is corresponded to the surface recombination rate. Therefore, the ratio of slope gives quantitative information of effect of TMAH. Slope decreased almost by a factor of four (0.08515/0.02398 = 0.28), indicating that TMAH can suppress the surface recombination by etching the sidewall.

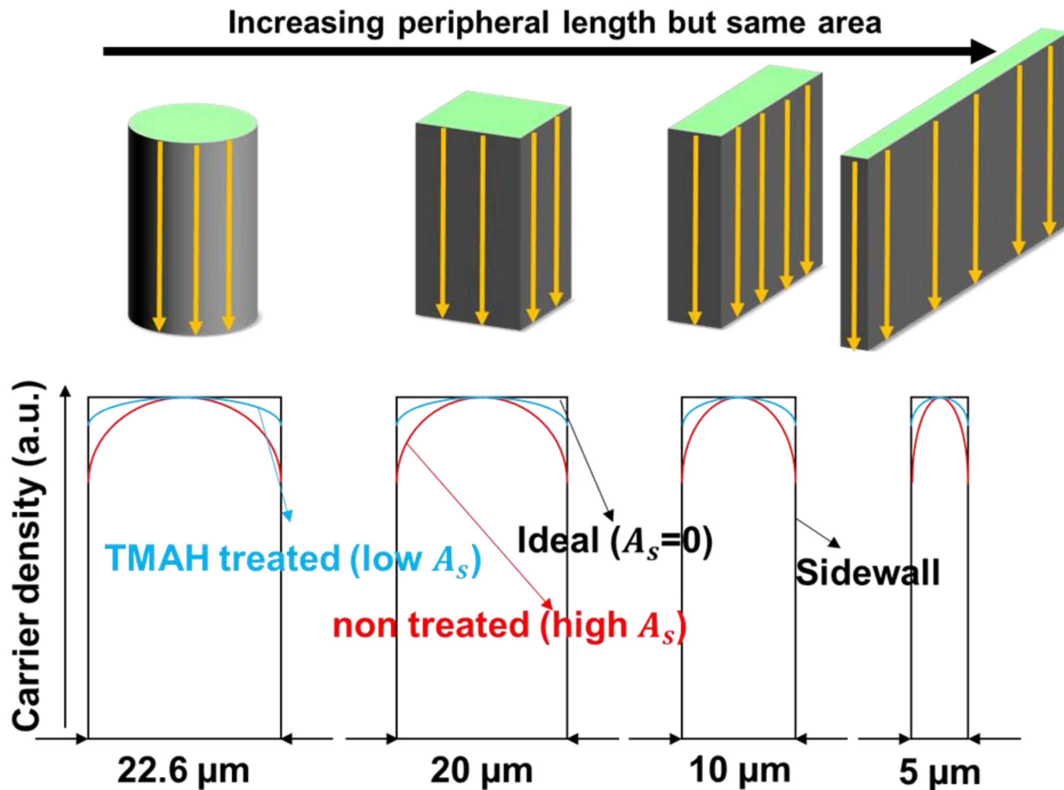

Figure 4.22. Schematic of carrier density with various mesa width and before and after TMAH.

However, the slope of J_{peak} after TMAH did not zero. This may indicate that TMAH somewhat alleviate the sidewall damage; however, it does not make that micro-LED fully avoid the sidewall damage. This behavior can be explained by the surface pinning effect. The surface of semiconductor does not have a band gap unlike the bulk area because the surface cannot have same atomic structure of the bulk (i.e., non-periodicity). This results in the free electrons are placed on the surface. To keep an equilibrium condition, the fermi level moves to appropriate position, which makes the band bending the band bending (i.e., depletion region). Lymperakis et. al found that all non-polar GaN surface are intrinsically pinned at E_c-0.6 eV even though no artificially induced surface damage [38], which might indicate that the surface pinning effect is inevitable. Therefore, it is difficult to fully avoid the sidewall damage, carrier's trap into the sidewall surface state leading non radiative recombination even though the sidewall is treated. **Figure 4.22** describes the relative carrier density with various mesa width. Although mesa size is fixed, the carrier loss is different depending on the mesa width and peripheral length due to the surface recombination rate. If all devices have same surface recombination rate, carrier loss relatively accelerates with decreasing the mesa width because the surface recombination term is inversely proportional to the mesa area. As we demonstrated, TMAH can decrease the surface recombination rate, which could suppress the carrier loss as described in Figure 4.22. On the other hand, even though TMAH etched the sidewall, the slope of J_{peak} is not still 0 as shown in Figure 4.21, inferring that ICP-RIE made not only the surface recombination at the sidewall surface but also the inside defects of mesa around 1 μm width. And the sidewall etching by etchant cannot perfectly remove the sidewall damage due most likely to the surface pinning effect.

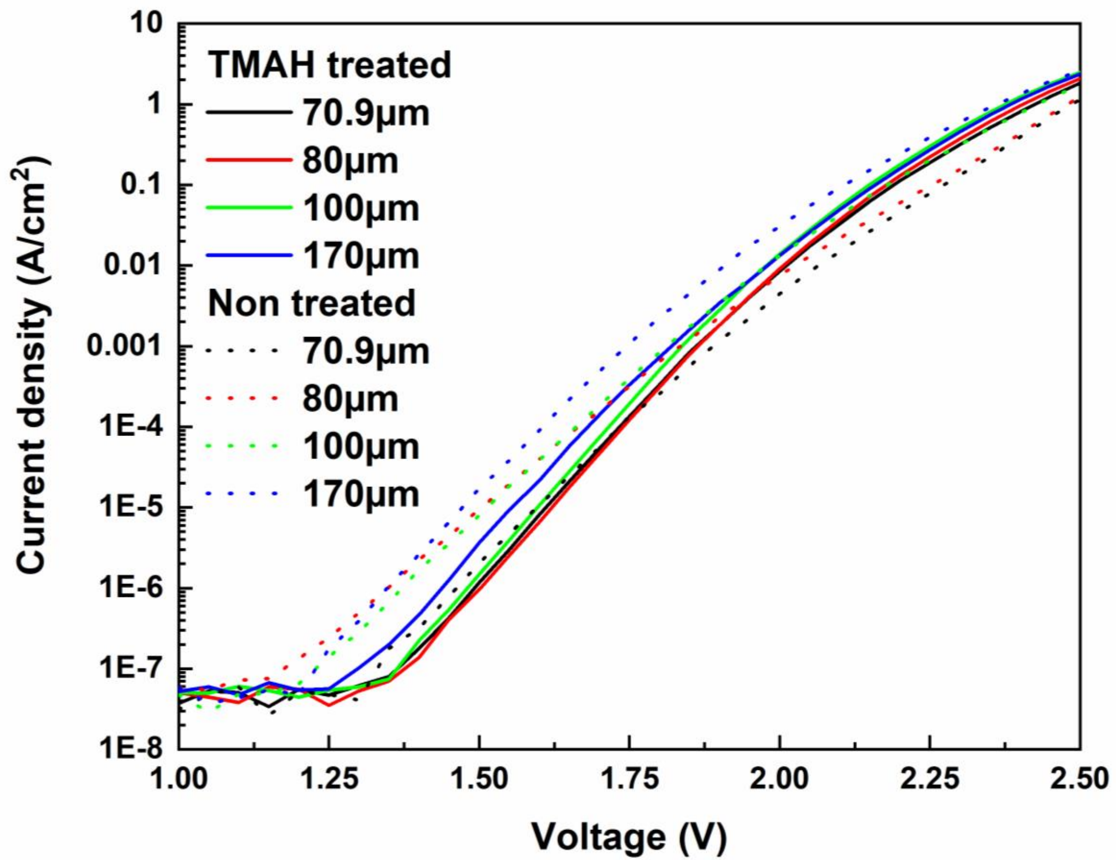

Figure 4.23. Current density-voltage characteristic of various peripheral lengths with and without TMAH treatment.

Additionally, it was confirmed that TMAH treated devices, regardless of the peripheral length, showed that the leakage current overall decreased from 1.25 to 2V, which agrees well TMAH removes the defect points that provides leakage path at the sidewall (**Figure 4.23**).

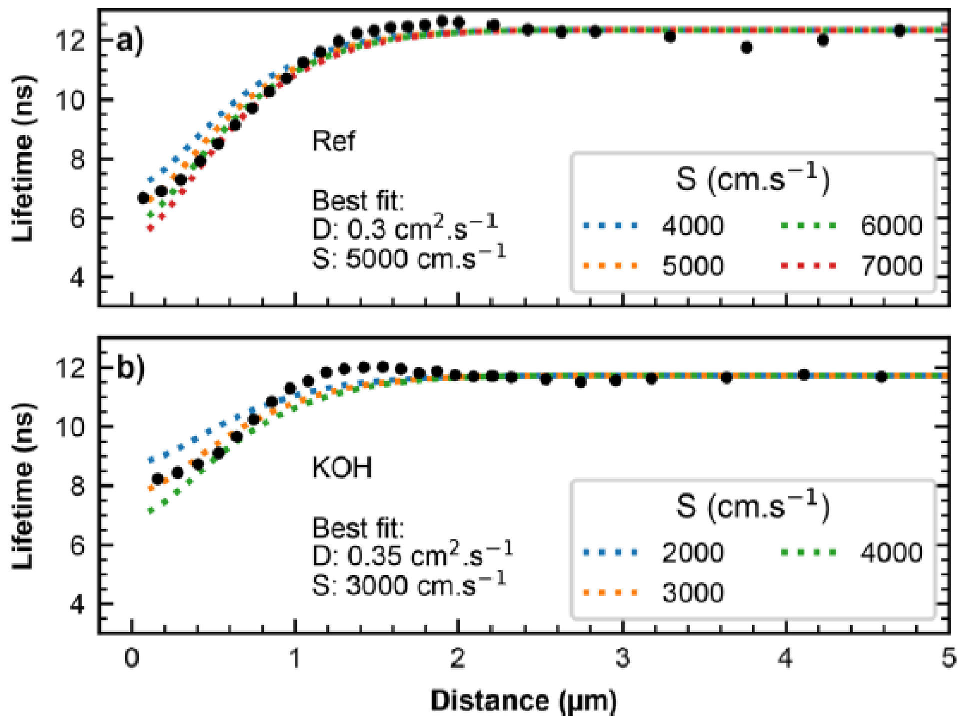

Figure 4.24. CL lifetime profile of a) without KOH b) with KOH treatment [15].

According to Finot et al., CL lifetime decreases as become close to the sidewall as shown in **Figure 4.24**. After KOH treatment, CL lifetime increases; however, it is still lower than the inside area (> 2µm distance). This data similarly say that the chemical treatment somewhat alleviates SRH non-radiative recombination by decreasing surface recombination; however, it cannot perfectly recover the plasma induced sidewall damage due to the surface pinning effect [38].

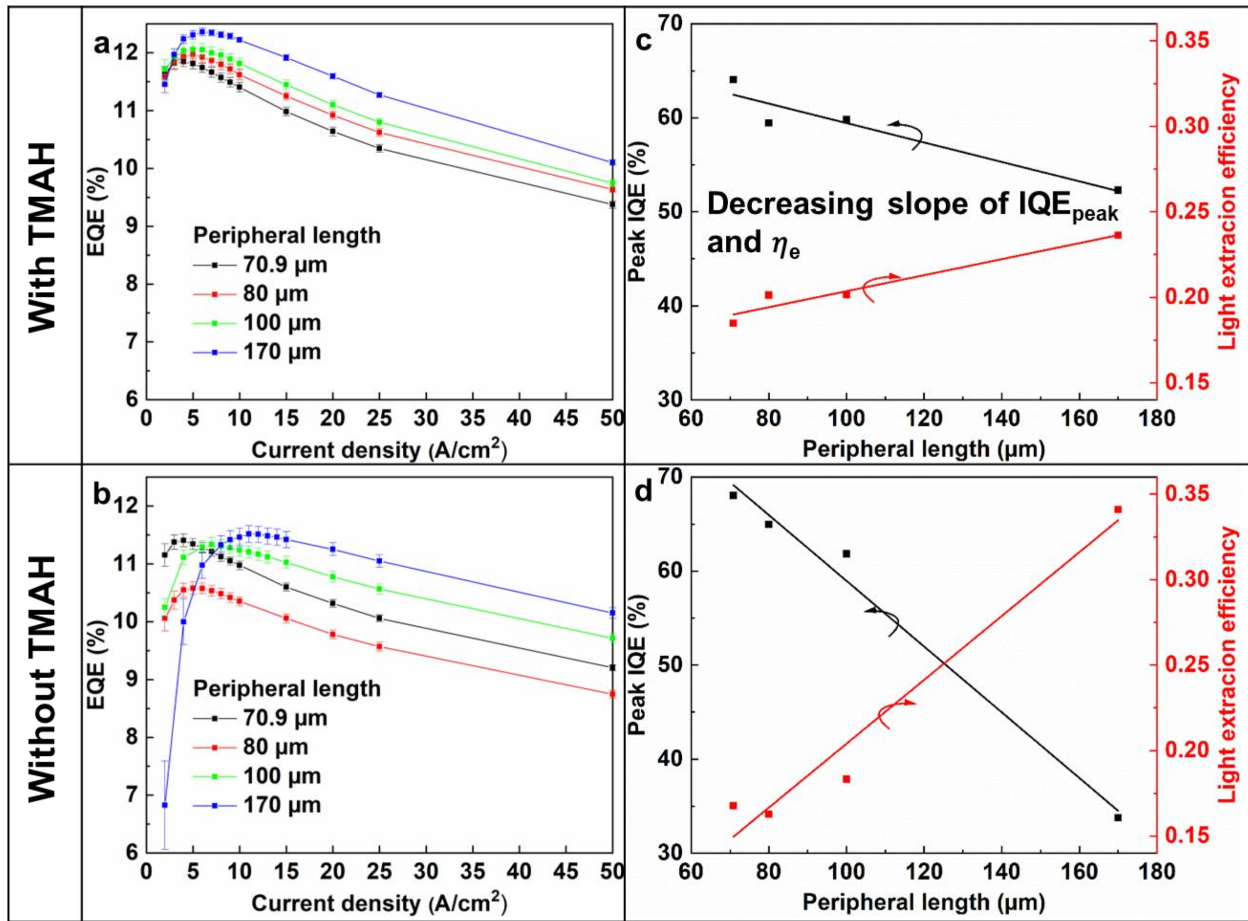

Figure 4.25. Peripheral length dependent absolute EQE of micro-LEDs with and without TMAH treatment. a) after TMAH treatment and b) before TMAH treatment. Peak IQE and light extraction efficiency as a function of the peripheral length of mesa obtained from absolute EQE curves. c) after TMAH treatment and d) before TMAH treatment.

Although TMAH treatment can decrease the surface recombination as a factor of four, the peak EQE did not dramatically increase as a decreasing surface recombination rate as shown in Table 4.2. After TMAH treatment, the sidewall surface became smooth as shown in Figure 4.16, meaning that before TMAH treatment had a rougher sidewall surface, which might increase light extraction efficiency due to decreasing the effective refractive index of sidewall. To clarify the effect of not

only surface recombination but also light extraction efficiency, all EQE curves were fitted by using Equation (5) and (6) and compared as shown in **Figure 4.25**. All fitting parameter P is available in the **Table 4.3**.

Table 4.3. Fitting parameter P extracted from each absolute EQE curves through Equation (5) and (6).

	Parameter P	
Peripheral length (μm)	Before TMAH	After TMAH
70.9	4.253	3.566
80	3.711	2.932
100	3.240	2.974
170	1.019	2.192

Regardless of TMAH, peak IQE decreased and light extraction efficiency increased with increasing the peripheral length. These results further clearly demonstrated that the longer peripheral length, the lower IQE and higher light extraction efficiency. Interestingly, it was observed that the slope of peak IQE and light extraction efficiency changed after TMAH treatment as shown in Figure 4.24a. Especially, the slope of peak IQE after TMAH treatment alleviated but, still it was not 0, agreeing that the sidewall damage cannot be perfectly removed by TMAH treatment. This result is similar to the slope of J_{peak} as shown in Figure 4.21 because IQE and J_{peak} are directly related to the SRH non-radiative recombination. In addition, the alleviated slope of light extraction efficiency was also observed after TMAH treatment, which indicates that the effect of peripheral length on the light extraction efficiency is less effective after TMAH treatment. As discussed, the effect of sidewall morphology in the chapter 3, the alleviated slope of light

extraction efficiency could be caused by changing the sidewall morphology as shown in Figure 4.25. Because of ITO layer placed on the top of p-GaN, ITO was etched together when mesa etching was proceeded. Compared to the without ITO layer, with ITO layer clearly formed the rough sidewall morphology, which could lead high light extraction efficiency via the sidewall. However, TMAH treated sidewall morphology became a smooth compared to before TMAH as shown in Figure 4.16 even though m-facet nano structures were revealed in both directions. This suggests again that the sidewall morphology critically affects the light extraction efficiency for small size LEDs. Therefore, the mesa etching together with ITO layer is a promising way to increases light extraction efficiency.

4.5 Appendix

In this appendix, additional data related to the chapter 4 is explained, especially sidewall conditions.

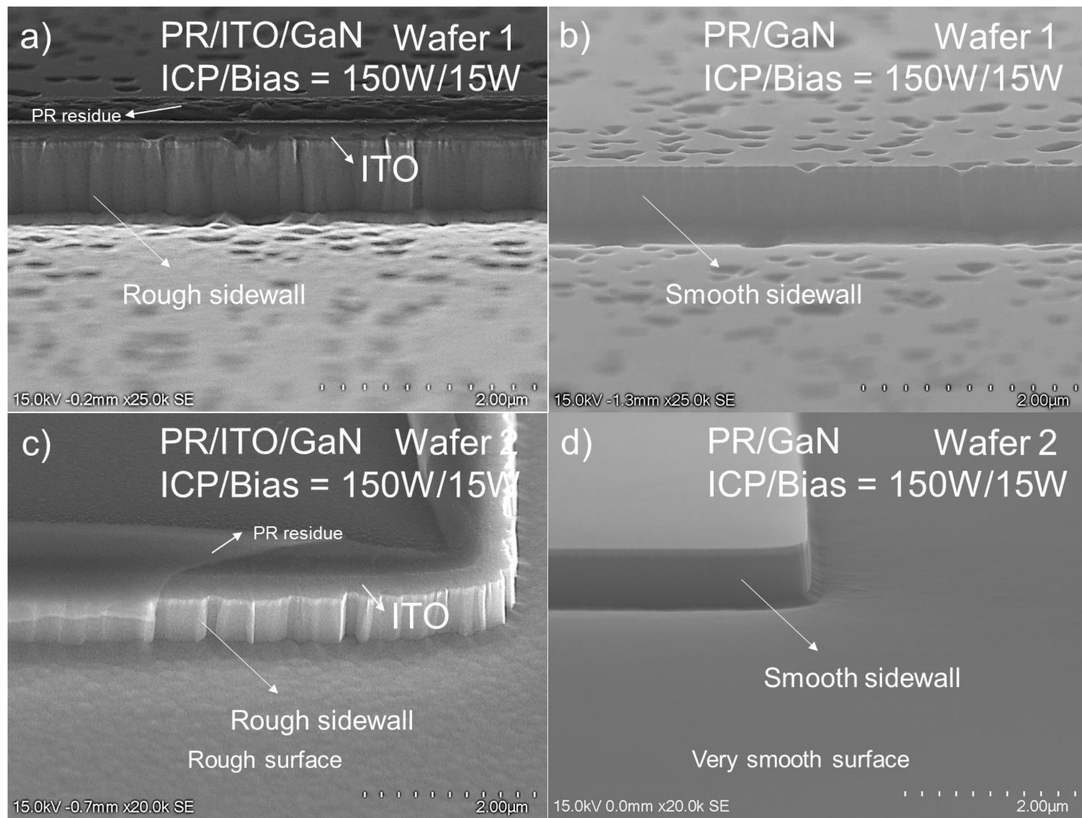

Figure. 4.26. SEM images of sidewall morphology after ICP-RIE etching. Observed sidewall morphology of wafer 1 a) ITO/GaN LED wafer b) GaN LED wafer. Observed sidewall morphology wafer 2 c) ITO/GaN LED wafer d) GaN LED wafer.

Figure 4.26 shows the observed sidewall morphology after ICP-RIE dry etching with the same etching conditions. For ITO/GaN samples shown in Figure 4.25a, c, it had 100 nm ITO layer and it's etching rate was around 0.3 nm/sec. Therefore, total etching time was about 330 second longer than GaN samples shown in Figure 4.25b, d. To clarify effect of ITO layer on the morphology, two different wafers were used for double checking. Interestingly, it was observed that the surface

morphology even sidewall differed depending on the presence of absence of ITO layer. Similar result was recently reported by Liu et al. [39]. They etched ITO and epi layer in ICP-RIE with combined etching condition and showed that etched n-GaN surface was rough because the splashed ITO crumb created by ICP-RIE led the inhomogeneity etching resulting in nanorods (rough surface) on the n-GaN layer. Absence of ITO layer showed smooth surface as shown in Figure 4.26b, d, which is common result; however, presence of ITO layer showed rough surface regardless of the wafer type, which clearly indicates that ITO layer leads the rough morphology. This rough morphology could make a high light extraction efficiency.

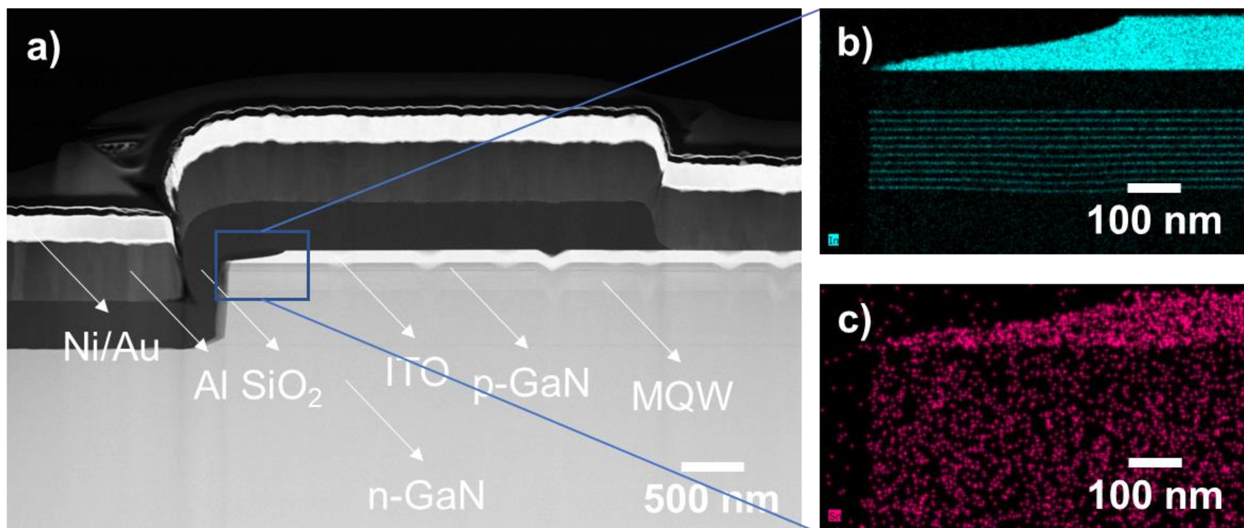

Figure 4.27. a) Cross sectional HAADF-STEM image showing device structure. EDS mapping for showing remained ITO layer after ICP-RIE etching b) In and c) Sn scan.

Cross sectional high angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image showing detail structure is available in **Figure 4.27**a. As shown in Figure 4.27a, ITO was slightly etched near the sidewall, the remaining ITO layer was clearly confirmed

by In and Sn Energy-dispersive X-ray spectroscopy (EDS) mapping as shown in Figure 4.27b, c, indicating that ITO layer worked as a transparent p electrode near the sidewall.

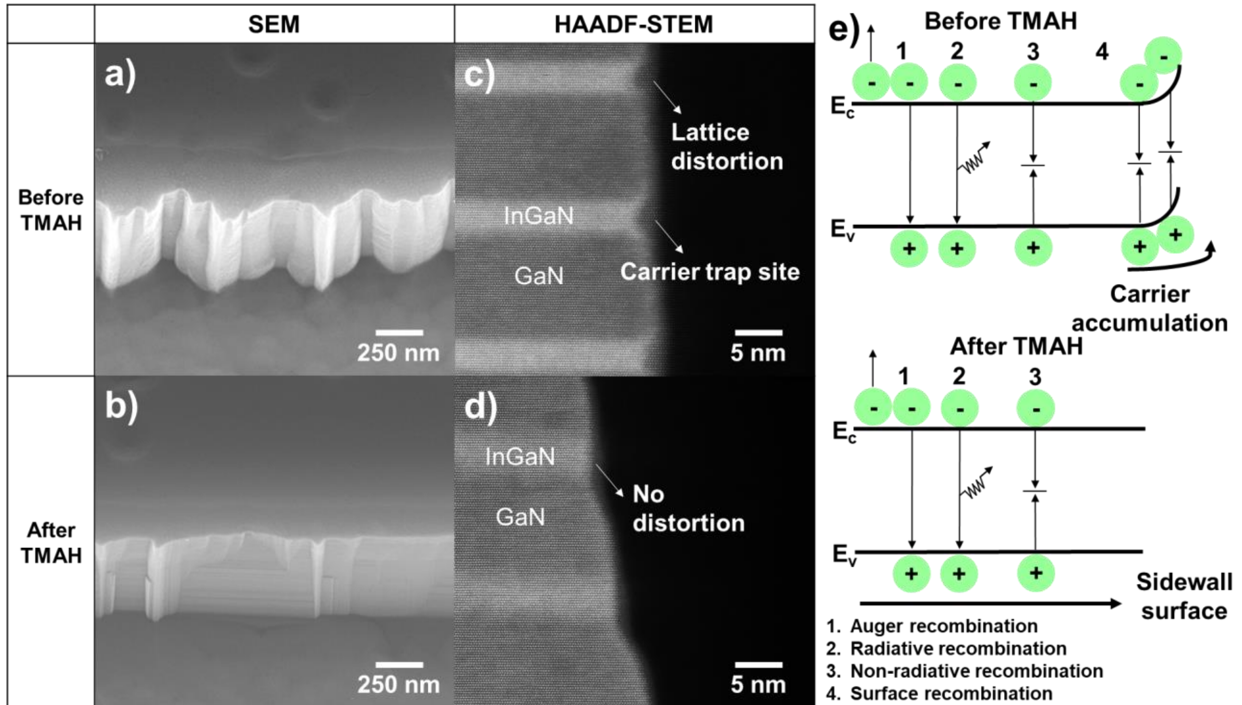

Figure 4.28 SEM image of bird's eye view showing sidewall morphology a) before and b) after TMAH etching. HAADF-STEM image observing lattice distortion at the sidewall c) before d) after TMAH etching. e) Schematic of various recombination process in µLED and describing effect of TMAH etching on the surface recombination.

Figure 4.28a, b shows that typical SEM images of m-plane direction sidewall before and after TMAH etching (observed it after ICP-RIE etching). Unlike the general case, the sidewall morphology before TMAH was quite rough because the ICP-RIE process was performed after deposition of ITO layer on the epi wafer. We compared the sidewall morphology without ITO

layer via same ICP-RIE etching conditions as shown in Figure 4.26. The sidewall morphology was not smooth before TMAH; however, it became quite smooth after TMAH, which clearly demonstrates TMAH etched the sidewall. Since TMAH etched sidewall morphology, the observed HAADF-STEM images shown in Figure 4.28c, d were also quite different before and after TMAH. According to Olivier et al., *A* dramatically increases due to the sidewall defects that makes more suffering with shrinking µLED size [11]. Moreover, Jiang et al. suggested that the carrier could be trapped at the sidewall and turned to be non-radiative recombination due to the modulation of the surface density of states [31]. Therefore, the observed the lattice distortion at the sidewall resulting from plasma induced ICP-RIE shown in Figure 4.28c might provide a chance increasing surface recombination rate and thus the carrier moves into the trap site and recombines as a non-radiation. On the other hand, it was clearly observed that lattice distortion disappeared after TMAH at the sidewall, which could reduce the surface recombination rate and decrease the carrier trap. The mechanism of carrier traps with surface recombination is described in Figure 4.28e. Bartos et al. systemically investigated that the surface band bending by X-ray photoelectron spectroscopy for polar, semipolar, and non-polar GaN. Moreover, they demonstrated that the surface disorder leads to major changes of the band bending and the charge redistribution on the surface. Therefore, an upward band bending could occur due most probability to the surface disorder [32] (same as lattice distortion), which seriously leads the non-radiative surface recombination by accumulating the carriers at the sidewall surface [31]. By etching sidewall through TMAH, the area of the lattice distortion disappears, which suppresses the surface recombination. Therefore, it is concluded that the surface disorder at the sidewall leading the band bending and SRH non-radiative recombination should be removed to realize high performance micro-LEDs.

4.6 Summary

It was confirmed that there is an interplay between sidewall damage and light extraction efficiency. Since the IQE of micro-LEDs is critically affected by the sidewall damage, the longer peripheral length showed lower IQE, which indicates that the sidewall damage is proportional to the peripheral length of mesa. On the other hand, the light extraction efficiency increased with increasing the peripheral length of mesa, which means the light could move out via the sidewall dimension. Although longest peripheral length was damaged and had lowest IQE, it had highest EQE at the relatively high current region, meaning that the light extraction efficiency more contributes to EQE than IQE. Therefore, enhancing light extraction efficiency is a promising way to realize high EQE of micro-LEDs. Furthermore, TMAH etching greatly reduced the surface recombination by 75%, which was confirmed by the slope of $J_{peak.}$ Because the surface recombination suppressed, peak EQE increased regardless of the peripheral length after TMAH etching. However, the slope of J_{peak} was not zero, which could say the sidewall damage could not be perfectly avoided by the sidewall etching process or the damage width induced by ICP-RIE is longer than the expected width.

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Chapter 5

Conclusions and future work

5.1 Summary

III−nitride based micro-LEDs can replace current display technologies such as LCD and OLEDs due to the superior physical and material performance. Moreover, top-down proceeded micro-LEDs allow us ultra-small pixel of micro-LEDs, which is the pathway to realize ultra-high PPI display. However, ICP-RIE system involves the plasma induced sidewall damage on micro-LEDs, which makes loss the efficiency of micro-LEDs as size goes down.

In this study, the influence of sidewall condition on the performance of micro-LEDs was investigated. Because ICP-RIE system is most important on the fabrication process of micro-LEDs, the ICP-RIE etching conditions was firstly investigated in this work. The etching bias power of ICP-RIE mainly decides an ion-bombardment that includes high energy and thus makes the non-radiative recombination centers at the sidewall. To suppress the ion-bombardment when the mesa of micro-LEDs is defined, we controlled the etching bias power. It was confirmed that the etched n-GaN surface and sidewall morphologies were different depending on the etching bias power. At the high bias power, the morphologies were smooth both n-GaN and sidewall; however, the morphologies became a rough as etching bias power decreased. Especially, lowest etching bias power (e.g., 2.5 W) showed roughest surface. This surface behavior with lowest bias power is caused by the chemical reaction between Cl_2 etching gas and GaN dislocation, which was clearly investigated via various substrates and panchromatic CL method. Because of chemical reactions

rather than physical based ion-bombardment, the EQE of micro-LEDs increased compared to high etching bias power. Two evidences support the enhancement of EQE of micro-LEDs:

-Lowest etching bias power sample showed lowest leakage current and lowest ideality factor, which indirectly demonstrates that the sidewall damage was suppressed.

-The roughed sidewall morphology increased the light escape cone due to decreased effective refractive index at the interface between GaN sidewall and air, which was further investigated by FDTD simulation, and it confirmed that light intensity near the sidewall increased with rough sidewall morphology rather than smooth one.

Therefore, it is speculated that the combined effect between suppressed sidewall damage and enhanced light extraction efficiency via roughed sidewall improved the EQE of micro-LEDs.

Current display system takes various pixel design such as circular, square, and stripe for best performance of display. To clarify effect of pixel design on the performance of micro-LEDs, EQE and J_{peak} were quantitatively analyzed by 400 μm^2 scale. It was confirmed that the peripheral length of micro-LEDs changed EQE especially IQE and light extraction efficiency. First, J_{peak} increased with increasing the peripheral length, indicating that longer peripheral length, higher sidewall damage since J_{peak} is proportional to SRH non-radiative recombination. Interestingly, EQE did not decrease even though the peripheral length increased. Rather, longest peripheral length had highest EQE. This behavior was further analyzed by separating IQE and light extraction efficiency from EQE since EQE includes IQE and light extraction efficiency. IQE decreased with increasing the peripheral length, which is caused by increasing SRH-non radiative recombination since IQE is reverse proportional to it. However, light extraction efficiency increased with increasing the peripheral length because the light also propagated from the sidewall, indicating that longer peripheral length higher sidewall emission and thus higher light extraction efficiency. This

increasing light extraction efficiency rather led enhancing EQE although IQE decreased. This result suggested that decreasing IQE could be compensated by increasing light extraction efficiency.

Since SRH non-radiative recombination includes surface recombination, we further quantitatively investigated via J_{peak}. It was found that the surface recombination velocity is proportional to the peripheral length, which increased SRH non-radiative recombination and thus decreasing IQE and increasing J_{peak}. One solution minimizing surface recombination rate is TMAH treatment at the sidewall. After TMAH treatment J_{peak} decreased regardless of the peripheral length, indicating that the surface recombination rate reduced. The observed STEM images at the sidewall further showed that TMAH removed the carrier trap site, which could decrease the surface recombination rate. Therefore, EQEs of TMAH treated devices regardless of peripheral length were higher than without TMAH treatment. As a consequence, this thesis suggests that the sidewall conditions critically contribute to the performance of micro-LEDs. Therefore, optimization of sidewall conditions could pave the way for realizing high performance of micro-LEDs for next-generation display.

5.2 Future work

This thesis mainly emphasizes that the sidewall condition critically affects the performance of micro-LEDs. Especially, the sidewall emission can increase total light extraction efficiency, which also leads increasing the EQE since EQE is proportional to light extraction efficiency. Enhancing the light extraction efficiency via sidewall is promising way to increase EQE; however, it may invariably bring the optical crosstalk between adjacent pixels due to the light emission of horizontal direction. This optical crosstalk makes a blur and smudging image, which aggravates the display quality. Therefore, it is necessary to make the light moves vertical direction.

To suppress the optical crosstalk, several methods were invented in micro-LEDs. Li et al. suggested that the light absorber layer placed back side can suppress the optical crosstalk [1]. Lin et al. reported that the photoresist can be used to alleviate optical crosstalk, which led better color purity in quantum dot applied micro-LEDs [2]. Abovementioned methods are useful for suppressing the optical crosstalk; however, it may not be suitable for allowing light emitted through the sidewall to be concentrated in a vertical direction. In the chapter 4, we confirmed that the sidewall emission becomes dominant as size decreases. A reflective layer may be applied to next to the sidewall of micro-LEDs to guide light in on direction. **Figure 5.1** shows the light field intensity with/without reflective layer at 470 nm wavelength. Figure 5.1a describes FDTD simulation structure for 5 μm mesa width micro-LED. Figure 5.1b shows the light propagation proceeds in all directions. Because there is no reflection layer next to the sidewall of micro-LED, the light emission shows the sphere pattern. Moreover, the light emitted from the sidewall also moves horizontally, which makes the cross talk between the pixels. Therefore, the horizontal emission from the sidewall needs to change vertically to suppress the cross talk. To overcome this, we can introduce the reflective layer. Figure 5.1c shows that Al reflective layer placed next to the

sidewall makes light emitted via the sidewall to be concentrated in a vertical direction. Moreover, thick Al reflective layer as shown in Figure 5.1d clearly shows that light emitted via the sidewall can move out to vertical direction without the spread. Therefore, it is necessary to apply the reflective layer next to the sidewall, which not only solves cross talk but also changes the light propagation from horizontal to vertical.

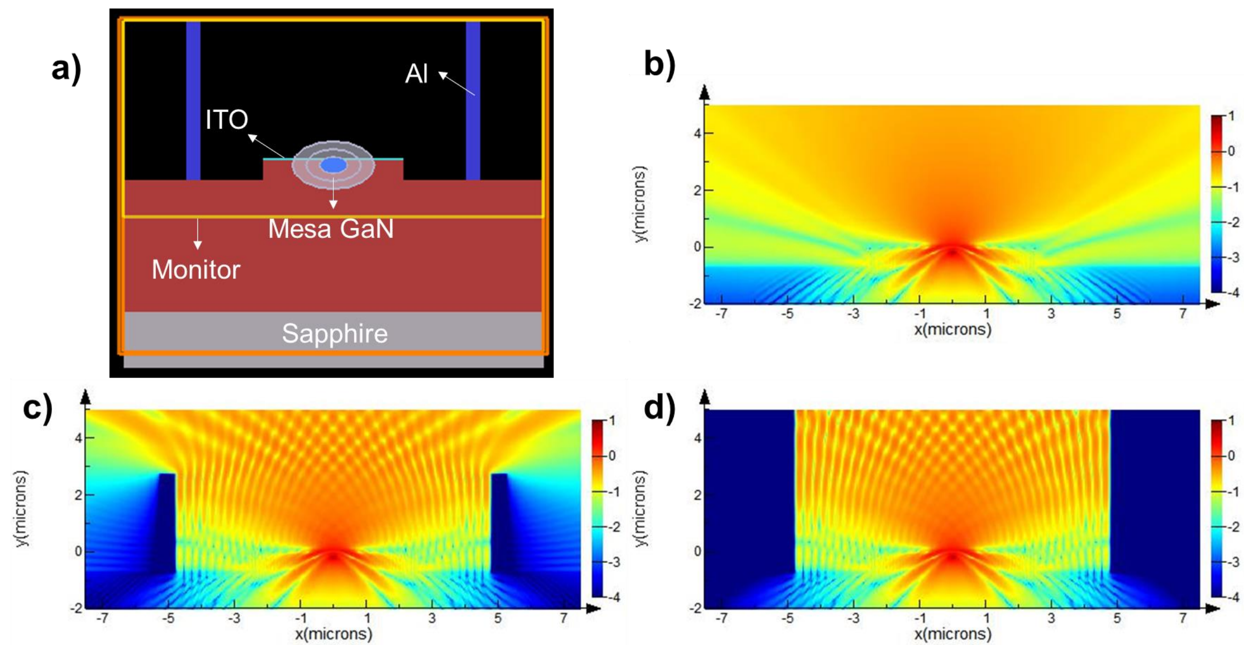

Figure 5.1. a) 2-D FDTD simulation structure for 5 μm mesa width micro-LED. Light field intensity b) without Al reflective layer c) with 3.5 μm and d) 5.7 μm thick Al reflective layer.

This introduced reflective layer is also used as a metal contact layer. OSRAM invented the trench formed LED structure (so-called UX:3 LED) shown in **Figure 5.2** [3]. In this structure, n-contact layer is designed as a reflector by creating trench structure. The metal layer placed in the trench works not only n-contact but also reflective layer. Therefore, the micro-LEDs whose performance

is improved by the lateral sidewall emission need to be constructed with the reflective layer that helps that the light moves vertically.

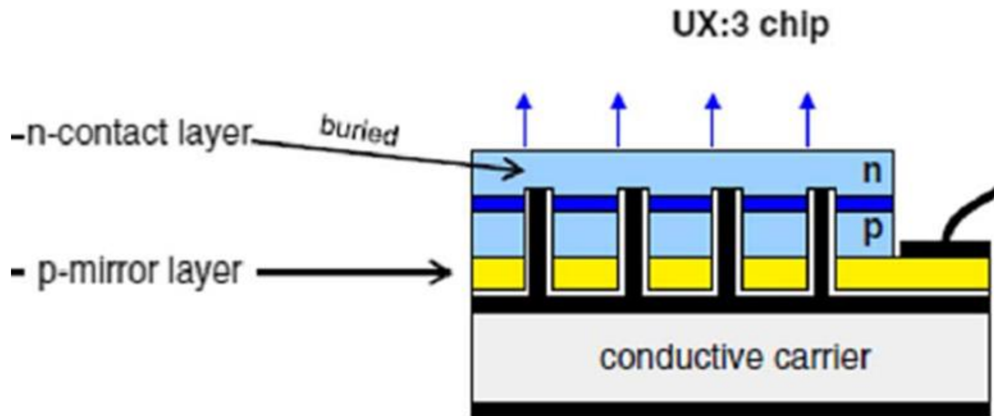

Figure 5.2. Schematic of UX:3 LED. The n-contact layer works as a mirror for light emission from the sidewall.

Another solution is to apply an omni-direction reflector (ODR). Hu et al. simulated that by covering the sidewall with ODR, the emitted light via sidewall can move in the vertical direction, thereby enhancing the front emission for light extraction efficiency improvement [4]. All of introduced methods in this section consequently share a similar purpose moving the light vertically. Although there are methods to solve the problem of sidewall emission, it is necessary to verify how much light extraction efficiency improves when the solutions are applied to micro-LEDs device.

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1. "Influence of sidewall condition on the performance of micro-LEDs"; **Jeong-Hwan Park**, Markus Pristovsek, Wentao Cai, Heajeong Cheong, Tae-Yeon Seong, Hiroshi Amano, (Article in preparation)

2. "High indium Content Nitride Submicron-Platelet Arrays: An Ultimate Platform for Long Wavelength Optical Applications"; Wentao, Cai, Yuta Furusawa, Jia Wang, **Jeong-Hwan Park**, Yaqiang Liao, Heajeong Cheong, Shugo Nitta, Yoshio Honda, Markus Pristovsek, Hiroshi Amano, (Article in preparation)

3. "Interplay of sidewall damage and light extraction efficiency of micro-LEDs"; **Jeong-Hwan Park**, Markus Pristovsek, Wentao Cai, Heajeong Cheong, Takeru Kumabe, Dong-Seon Lee, Tae-Yeon Seong, Hiroshi Amano, *Optics Letters*, *May 2022* https://doi.org/10.1364/OL.456993

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5. "The stability of graphene and boron nitride for III-nitride epitaxy and post-growth exfoliation"; **Jeong-Hwan Park**, Xu Yang, Jun-Yeob Lee, Mun-Do Park, Si-Young Bae, Markus Pristovsek, Hiroshi Amano, and Dong-Seon Lee, *Chemical Science*, *Jun. 2021* [selected as cover picture] https://doi.org/10.1039/D1SC01642C

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LIST OF PRESENTATIONS (International)

1. "Relationship between sidewall damage and light extraction efficiency on the micro-LED"; **Jeong-Hwan Park**, Markus Pristovsek, Wentao Cai, Heajeong Cheong, Takeru Kumabe, Dong-Seon Lee, Tae-Yeon Seong, Hiroshi Amano, *International Workshop on Nitride Semiconductors (IWN)*, *Oct. 2022* (Accepted)

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LIST OF PRESENTATIONS (Domestic)

1. "Stability of Graphene on GaN for the Realization of III-Nitride Remote Epitaxy", **Jeong-Hwan Park,** Xu Yang, Jun-Yeob Lee, Mun-Do Park, Dong-Seon Lee, Si-Yeong Bae and Hiroshi Amano, *The Korean Physical Society (KPS) Spring Meeting, Apr. 2021*

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