# Nanorod-Based Vertical GaN-on-GaN Schottky Barrier Diodes Fabricated by Top-Down Approach

**(トップダウン的手法により作製したナノロッド縦型GaN-on-GaNショットキーバリアダイオード)**

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Doctoral Dissertation

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# Abstract

In this day and age, the concerns on reduction of power dissipation in power conversion systems become significantly urgent towards the sustainable development of society. Silicon (Si)-based power devices, as the essential components in power conversion system, have been widely developed and become indispensable parts in our modern life. Since Si-based power devices have experienced extensive research and sophisticated development for a long-term time, a further improvement of device performance is severely hindered by physical limitations of Si-based materials.

Gallium nitride (GaN) has already become a prevailing candidate for high-performance power electronics owing to its excellent material properties including a wide bandgap, a high critical electric field, a high electron saturation velocity and high temperature endurance. Over the last two decades, lateral GaN/AlGaN heterojunction-based high electron mobility transistors (HEMTs) have witnessed rapid progress with recent large-volume commercialization in a variety of applications such as power supply and fast charger. Meanwhile, as free-standing GaN substrates with a low threading dislocation density ($< 10^6/cm^2$) become more widely available, vertical GaN-on-GaN power devices are attracting widespread attention because of their great potentials in achieving some desirable device performances such as high-power handling capability, improved device reliability, and more efficient thermal dissipation and management over their lateral counterparts.

As an elementary building block in GaN electronics, GaN-Schottky barrier diodes (SBDs) have been extensively studied owing to their low turn-on voltage ($V_{ON}$) and rapid

switching speed. However, the device performance is typically hindered by a high reverse leakage current and premature breakdown. To overcome these shortcomings, a substantial amount of research for high-voltage GaN-SBDs has been devoted to the development of edge termination techniques such as field plate, junction barrier Schottky diode, trench MOS barrier Schottky diode, and others. Nanorod/nanowire (NR/NW) and Fin structures have enabled the implementation of novel GaN device concepts such as enhancement-mode MOSFETs, FinFETs, and super-junction structure. Furthermore, it is also interesting to note GaN NR-based SBDs whether they could serve as an alternative to high-voltage SBD, because nanostructures can readily make the most of the Reduced Surface Field (RESURF) effect.

In this dissertation, the author studies on NR-based vertical GaN-on-GaN SBDs fabricated by top-down approach. In Chapter 1, the author describes the background, as well as the outstanding issues, and the motivation of this study.

In Chapter 2, the author discusses the feasible methods to fabricate GaN nanostructures and an etching-based top-down approach is regarded as a suitable way for the subsequent fabrication. Moreover, relevant process/characterization facilities, which would be frequently utilized throughout this study, are briefly introduced.

In Chapter 3, by Silvaco TCAD simulations, the author indicates GaN NR/NW-based structures could benefit from the dielectric RESURF effect and be regarded as an alternative for high-voltage SBDs. Furthermore, the practice fabrication of NR (mesa)-SBDs was proceeded by top-down approach. The dielectric RESURF effect on NRSBDs is demonstrated, which corresponds with the simulation results.

However, non-ideal carrier transportation at the Schottky interface was confirmed in the fabricated SBDs, as a result of the adverse effect from $CF_4/O_2$-based etch-back process. To solve this problem, the optimization, which is based on low-damage etch with a fairly low bias voltage and post annealing process, was carried out for NRSBDs. The recovered device performance proved the effectiveness of this optimization.

In Chapter 4, the author introduces the optimized dry- as well as wet-etching process, and the vertical NRs with high aspect ratio and distinct non-polar sidewall can be obtained by following the optimizations. Furthermore, a more reliable and feasible process flow for NRSBDs fabrication is proposed. The NRSBDs fabricated by new process flow feature improved and competitive device performance. In addition, the evaluation for Schottky barrier heights (SBH) of NRSBDs, and the importance of wet-etching process were systematically studied by both static and dynamic characteristics.

In Chapter 5, the author summarizes this study and shows some future perspectives on GaN nanostructure-based devices.

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# Chapter 1 Background

**1.1** Introduction to power Electronics

**1.2** Wide bandgap semiconductor

**1.3** Gallium Nitride

**1.4** Motivation and Objective

References

## 1.1 Introduction to power Electronics

For the past several decades, due to the fast expansion of modern civilization, human existence and industry are becoming more reliant on efficient energy consumption. Many clean energy resources, such as wind power, solar power, nuclear power, and others, have been widely investigated and developed by a considerable amount of effort from experts in many fields. As a result, the requirements for high-efficiency electrical power conversion are becoming more significant, and the rehabilitation of power systems is becoming increasingly necessary and challenging. Power electronics, as the fundamental part in power conversion system, have been extensively developed in our life including industry applications and consumer applications, as shown in **Fig. 1.1**.

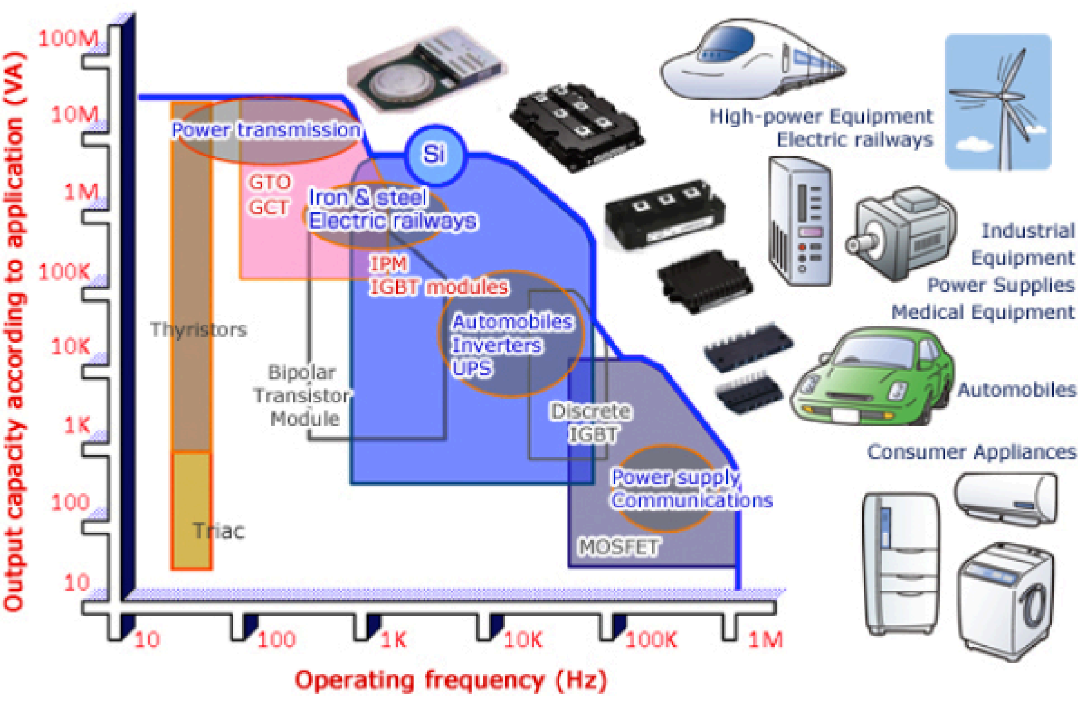


**Figure 1.1:** Various power electronics applications [1].

Power semiconductor devices, such as diodes, transistors, and others, are the basic components of power electronics and attract tremendous attention in modern semiconductor industry. Meanwhile, the market for power devices is sharply expanding in recent years. According to the data from Yole [2] (**Fig. 1.2**), with a compound annual growth rate (CAGR) of 6.9 %, the worldwide market for power electronics is contemplated to rise from its current 2020 valuation of $17.5 billion to over $26.2 billion by 2026.

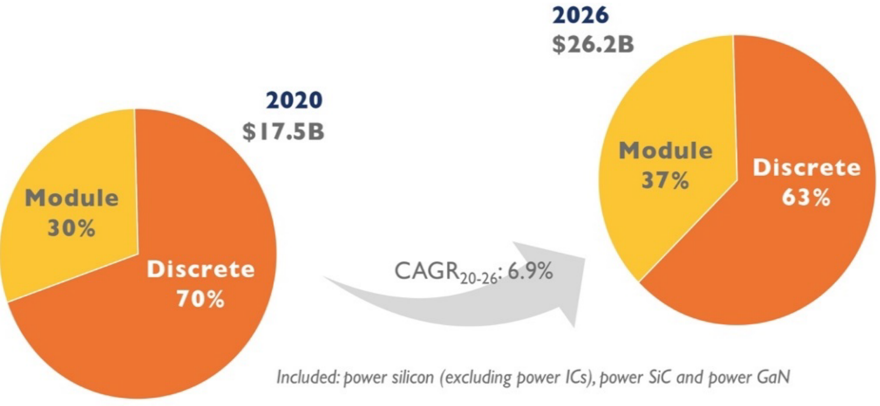


**Figure 1.2:** Global market of power devices in near future.

Nowadays, a vast majority of power devices are fabricated using silicon (Si), as a result of several advantages including simple accessibility, low cost and high quality of large-size bulk Si wafer, sophisticated fabrication technologies and so on. Furthermore, in the past decades, the considerable efforts were devoted to developing Si-related technologies

in fields of material science, semiconductor device physics, integrated circuit and so on. However, with the exponentially increasing command of high-efficiency power conversion for sustainable development, Si-based power electronics has been matured and hindered by the limitation of material properties of Si.

## 1.2 Wide bandgap semiconductors

Compared with Si, the representative wide bandgap (WBG) semiconductors, like Silicon Carbide (SiC), Gallium Nitride (GaN), Gallium Oxide ($Ga_2O_3$), diamond, etc., are regarded as promising candidates for future electronics, due to the excellent material properties including wide bandgap, high critical electric field strength, high electron saturation velocity, superior chemical stability etc. Table 1 lists several key material properties at 300 K for Si, 4H – SiC, and GaN.

**Table 1:** Material properties of Si, 4H-SiC and GaN (at 300K).

| | **Si** | **SiC** | **GaN** |
|---|---|---|---|
| Bandgap (eV) | 1.11 | 3.2 | 3.4 |
| Critical electric field (MV/cm) | 0.3 | 2.6-2.8 | ~3 |
| Electron mobility ($cm^2/V \cdot s$) | 1350 | 300-900 | 2000 |
| Thermal conductivity ($W/cm \cdot K$) | 1.5 | 3.5 | 2.0 |
| Electron saturation velocity ($\times 10^7$ cm/s) | 1.0 | 2.2 | 2.7 |

Furthermore, by using a model of one-sided abrupt junction, the reason why a WBG semiconductor-based power device enables an enhanced breakdown voltage ($BV$) and a reduced specific on-resistance ($R_{on,sp}$) simultaneously compared with its Si-based counterpart can be well explained. In this model, the full depletion is taken into account in

the n-side of the abrupt junction with a net impurity concentration of $N_D$. As a given reverse voltage is applied, **Figure 1.3** delineates the distribution of electric field along the junction distance ($W_D$) in both Si and WBG semiconductor one-sided abrupt junctions. Furthermore, owing to sustaining the same reverse voltage, the triangle area of two one-sided abrupt junctions enclosed by slope of electric field is equal. Furthermore, to take the typical WBG material like SiC or GaN as an example, the material features an approximate critical electric field ($E_{cr}$) around 3.0 MV/cm, approximately tenfold larger than that of Si. Thus, a WBG semiconductor-based junction could enable a tenfold compressed drift region, along with a hundredfold higher impurity density, resulting in a largely reduced on-resistance.

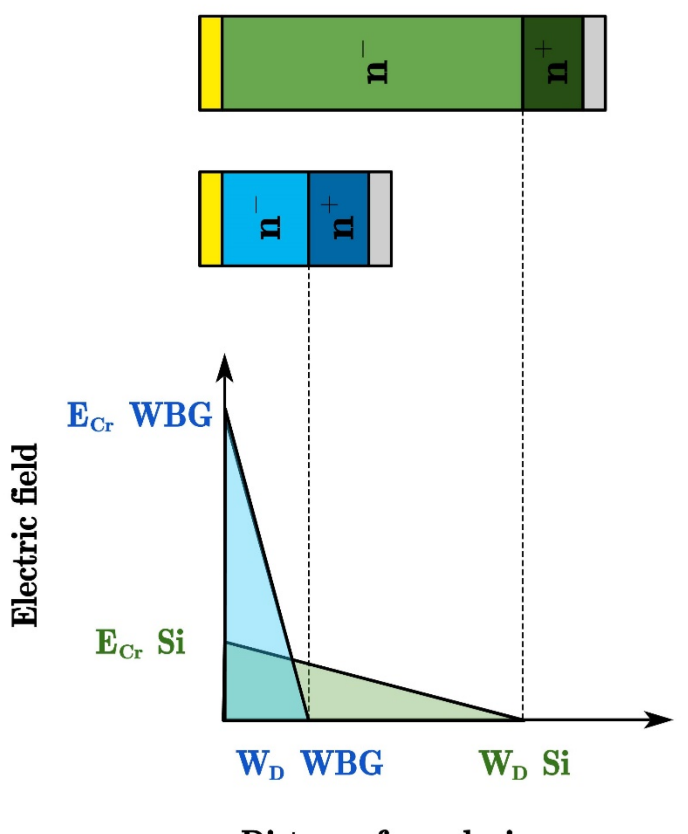


**Figure 1.3:**

In a one-sided abrupt junction, the difference of distribution of electric field between a WBG semiconductor and Si at a given reverse voltage.

Moreover, the discussion above could be well explained by following equations:

$$R_{on.sp} = \left(\frac{W_D}{q \cdot \mu_n \cdot N_D}\right) \quad (1.1)$$

$$W_D = \frac{2BV}{E_{Cr}} \quad (1.2)$$

$$N_D = \frac{\varepsilon_S \cdot E_{Cr}^2}{2q \cdot BV} \quad (1.3)$$

where $q$ is the electronic charge, $\mu_n$ is the electron mobility, and $\varepsilon_s$ is the permittivity of semiconductor. Commonly, the figure of merits (FoMs), contain some important parameters, are usually used to evaluate device performance or procedure. Baliga's FoM (BFoM) [3], which was defined by Dr. B. Jayant Baliga (a pioneer in field of power electronics), is frequently used as an indicator to compare the performance of power device. By combining the equations above, the relationship between $R_{on,sp}$ and $BV$ can be derived as follow:

$$R_{on,sp} = \frac{4BV^2}{\varepsilon_S \cdot \mu_n \cdot E_{Cr}^3} \quad (1.4)$$

In this equation (1.4), $\varepsilon_s \mu_n E_{cr}^3$ is so-called BFoM, tightly related to material properties. Furthermore, according to parameters listed in Table. 1, the limitations of Si-, 4H – SiC-, and GaN-based unipolar devices could be clearly understood.

Researches on SiC have been well investigated over many years. The sophisticated technologies, including epitaxial wafer with high quality [4, 5] and large size, feasible and stable process [6], promote a rapid development and a successful commercialization for SiC. As to the history of industry SiC-based power devices, Infineon and Cree

commercialized SiC Schottky barrier diodes (SBDs) in 2001 and 2002, respectively. In 2011, SiC power MOSFETs were debuted [7] by Cree, and other companies successively introduced their products of SiC power MOSFETs since that time. Until now, SiC has become to a very competitive material and showing a huge potential for future power electronics market, as shown in **Fig. 1.4** [8].

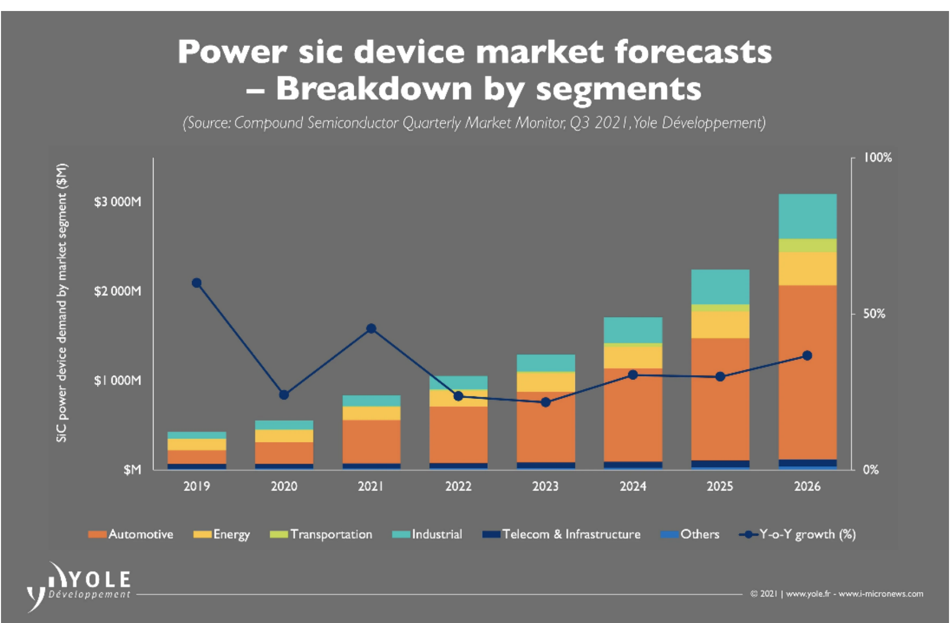


**Figure 1.4:** Perspective of market for SiC power devices [8].

# 1.3 Gallium Nitride

## 1.3.1 Brief history for optoelectronics

Before 1986, researches on GaN seemed to be obstructed and advanced quite slow. In 1986, Amano et al. demonstrated that the GaN film with high quality was successfully grown on a sapphire substrate by using low-temperature buffer layer of AlN [9]. Subsequently, Amano et al. also realized the p-type conduction in p-GaN by low-energy electron beam irradiation and device fabrication of blue/UV LED [10]. Several years later, in 1994, InGaN/AlGaN double-heterostructure blue LEDs with high brightness was demonstrated by Nakamura et al. [11]. After that, GaN and GaN-based optoelectronic devices started to attract tremendous attention in a large scale and become an indispensable material at present. As a result, it was found that the energy utilization of lighting nowadays has been largely decreased with universal utilization of LEDs. Toward a sustainable development of society, it is believed that GaN-based optoelectronics will continuously play an important role. For instance, mico-LEDs are regarded as a pioneer for the next generation of display, due to high power-efficiency [12].

### 1.3.2 GaN-on-Si epitaxial growth

In 1993, Watanabe et al. presented the investigation about successful epitaxial growth of single crystal GaN on a Si (111) substrate [13]. The stress originated from lattice mismatch between Si and GaN could be relaxed using an AlGaN/AlN-based intermediate buffer layer [14-16]. The development of epitaxial growth on GaN-on-Si technology largely promotes the development of lateral GaN devices, and the cost is dramatically reduced because of a dominated price advantage for large-size Si wafer, compared with other substrates. However, it does not seem to readily reduce the relatively high dislocation density (typically > $10^8/cm^2$) from the GaN-on-Si epitaxy. And a relatively high dislocation density generally carries some adverse effects for device performance, like current collapse, premature breakdown, etc. [17-20].

### 1.3.3 Lateral GaN-on-Si power device

Owing to the existence of high threading dislocation density for GaN-on-Si epitaxial growth, the researches about vertical GaN-on-Si power devices are not be discussed in detail. Even though some improvements have been achieved [21-27], an effective way to avoid the dislocations for vertical GaN-on-Si devices is still highly expected.

Alternatively, as the most notable lateral GaN power device, high electron mobility transistors (HEMTs), which is based on AlGaN/GaN heterojunction, have been well

developed in the past years [28-38]. Basically, when a thin AlGaN film layer is grown on the Ga-polar unintentional doped GaN (UID-GaN), as a result of piezoelectric and spontaneous polarization effect [39], a two-dimensional electron gas (2DEG) can be generated at the heterointerface (on the top of UID-GaN), as shown in **Fig. 1.5 (a)**. **Figure 1.5 (b)** depicts the corresponding energy band diagram of the GaN/AlGaN heterojunction. The generated 2DEG can deliver a high carrier concentration, along with a high electron velocity simultaneously, leading the HEMTs to achieve an improved device performance like lower $R_{on}$, compared with Si-based power devices. Apparently, the HEMT in the figure works as a depletion-mode (D-mode) transistor. Its normally ON characteristics are not desired because safe operation in the power conversion system is significant.

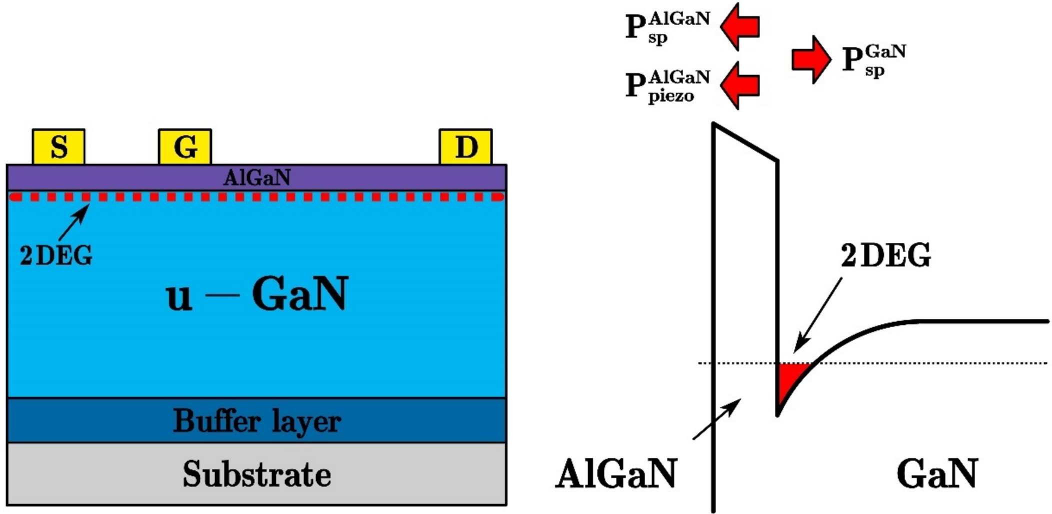


**Figure 1.5:** (a) The schematic structure and (b) band diagram of a typical AlGaN/GaN based-HEMT.

Over the past couple of decades, there has been a great deal of effort focusing on realization of enhancement mode HEMT (E-mode, normally OFF operation). There are two major approaches in which AlGaN/GaN heterojunction-based devices can be made to operate normally OFF. The first approach is considered from the aspect of circuit. By using a cascode structure [40], a D-mode GaN HEMT with high voltage can be matched with an E-mode Si MOSFET with low voltage to achieve normally OFF operation for GaN/AlGaN HEMT, as shown in **Fig. 1.6**. The distinct merit of this configuration is the facile gate control of high-voltage HEMT which is similar to the gate control of low-voltage Si-MOSFET.

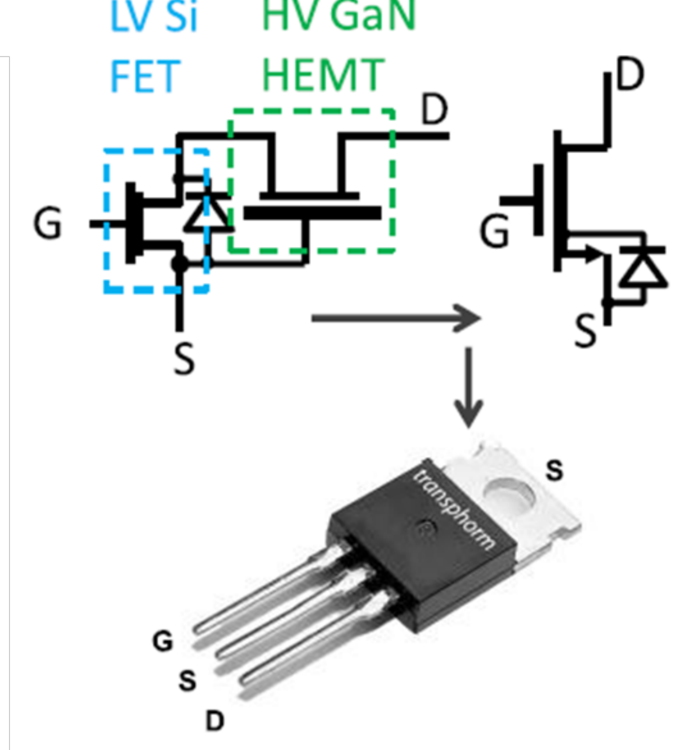


**Figure 1.6:** Cascode configuration of "HV D-mode HEMT + LV Si-MOSFET" [28].

To improve the slew rate, which is tightly related with elimination of ringing noise and safe operation, the individual gate control for the GaN HEMT is urgently desired. Thus, the second approach is mainly considered from the aspect of device fabrication. By lots of effort, two fabrication techniques have been successfully developed. One of methods is to grow an additional p-type GaN film layer on the AlGaN thin layer, so there is an inserted p-GaN between the gate metal and AlGaN after gate process. The negative charge in the p-GaN may effectively deplete the 2DEG in case the doping level and the thickness of p-GaN have been be well designed [41]. As a typical example, the gate injection transistor (GIT, **Fig. 1.7(a)**), proposed by Uemoto et al. [42], realized a normally OFF operation by employing hole injection from p-AlGaN gate. However, it is found the current collapse is still severe in GIT after applying a high reverse voltage on the drain. To solve this kind of degradation of dynamic performance in GIT, Kaneko et al. further developed a hybrid-drain-embedded GIT (HD-GIT) to suppress current degradation by adding another p-GaN to connect with drain electrode, as shown in **Fig. 1.7 (b)** [43]. The injected holes from this additional p-GaN near the drain region could effectively compensate trapped electrons under off-state, resulting a recovered dynamic device performance [44]. Also, towards the stable manufacture, some of new attempts were also utilized to develop p-GaN based E-mode HEMTs like regrowth techniques [45].

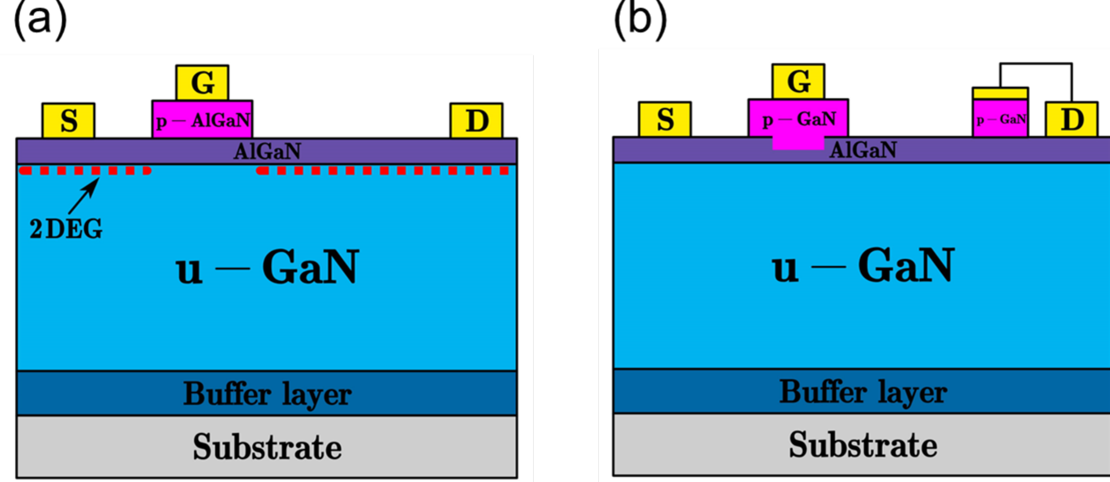


**Figure 1.7:** Schematic structure of (a) conventional GIT and (b) HD-GIT.

Another realization of normal-off power GaN transistor from the aspect of fabrication is called metal insulator semiconductor (MIS)-gate HEMT, as shown in **Fig. 1.8** [46]. The thin AlGaN barrier layer is removed by etching process, as a result, there is no more positive charge under the gate. And an ultra-thin AlGaN layer (typically smaller than 1.5 nm) can be remained to keep the high electron mobility in the channel. Furthermore, dielectrics with high-quality need to be deposited in the recessed region to reduce the leakage current from the gate. Even though low gate leakage and large swing have been reported in MIS-HEMT [47-49], a higher interface state density may be induced at the interface between etch region and deposited dielectric [50], resulting in degraded device performance like resulting in instability of threshold voltage and inferior reliability [51]. Thus, the high-quality dielectric/appropriate etching process is highly required, it is

reported that the SiN deposited by low pressure chemical vapor deposition (LPCVD) is a good choice as dielectric for MIS-HEMT [52,53].

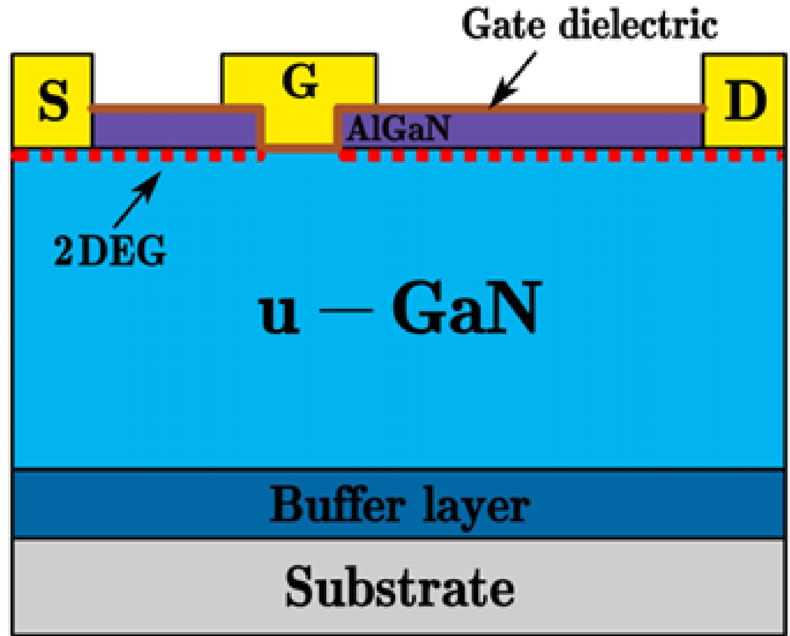


**Figure 1.8:** Schematic structure of a typical MIS-HEMT.

### 1.3.4 GaN-on-GaN epitaxial growth

In the past decades, the researches on how to successfully grow a thick GaN bulk have been extensively carried out. Nowadays, several techniques were successfully developed for GaN bulk crystal growth, including HVPE, Ammonothermal [54], and Na flux method [55]. At the initial stage, the HVPE system is regarded as the most promising candidate,

due to a high growth rate. The challenges were mainly focused on crack and method to reduce dislocation density. A method called void-assisted separation (VAS) was proposed to effectively reduce stress between GaN/Sapphire by Oshima et al [56]. And the GaN substrate was successfully fabricated. Furthermore, based on this method, Fujikura et al. also achieved growing the GaN crystal with large size, microdefect-free and thick layer [57]. The process flow is shown in **Fig 1.9.** With the emerged GaN substrate, the realization of vertical GaN-on-GaN devices has become more promoted. However, owing to the high price of substrate, the commercialized fabrication of GaN electronic devices is still based on epitaxial growth on foreign substrate.

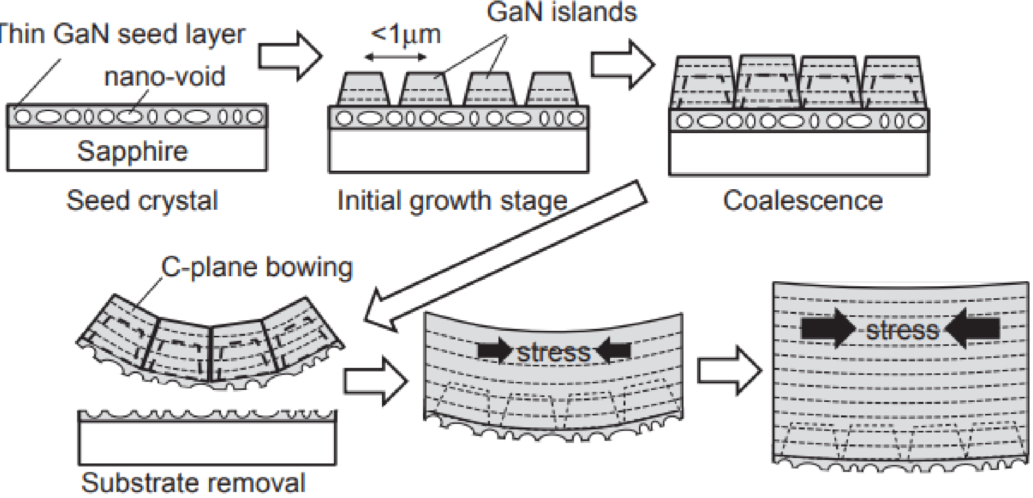


**Figure 1.9:** Process flow of void-assisted separation method [56] in HVPE.

### 1.3.5 Vertical GaN-on-GaN power device

Most of Si- and SiC- based power devices feature a vertical geometry. With the merged conductive n-type GaN substrate with a high quality, more effort has been devoted to realizing novel vertical GaN device concepts. For a lateral GaN power device like HEMT, to achieve a higher $BV$, the distance between gate and drain need to be scaled up, result in the increase of device size. By contrast, for a vertical power device, the high voltage requirement could be realized by increasing the thickness of blocking layer without sacrificing device area. Furthermore, the 2DEG in lateral power HEMT flows near the interface, the electrons are likely to be captured by surface states, which will cause degraded dynamic performance like current collapse [58-60]. Also, the peak of electric field in lateral power devices is commonly close to surface, so a deliberate management of electric field is highly required [61, 62]. On the contrary, the homoepitaxy could offer a vertical structure with high-quality, and the peak electric field of vertical devices could be shifted or located inside bulk, so the device performance will not be readily affected by traps, showing a high device reliability. Moreover, the 2DEG in HEMT structure is confined in a thin layer on top side of GaN, the temperature of device may be elevated causing thermal problem. For vertical devices, the current conducted vertically, more uniform rather than the lateral counterpart, so the thermal management of vertical devices will be better.

From the next paragraph, the development of GaN-on-GaN power diodes and edge termination technologies will be briefly summarized.

### 1.3.5.1 P-I-N diodes

GaN p-i-n diodes on the GaN substrates were firstly reported in 2005 [63]. But, until 2010, Nomoto et al. just reported a high breakdown voltage (*BV*) over 1000 V was achieved [64]. The p-i-n diodes with avalanche *BVs* of 2.6 and 3.7 kV [65,66] were reported by Avogy Inc., an implantation-based edge termination technology was utilized to manage the distribution of electric field, as shown in **Fig. 1.10 (a)**.

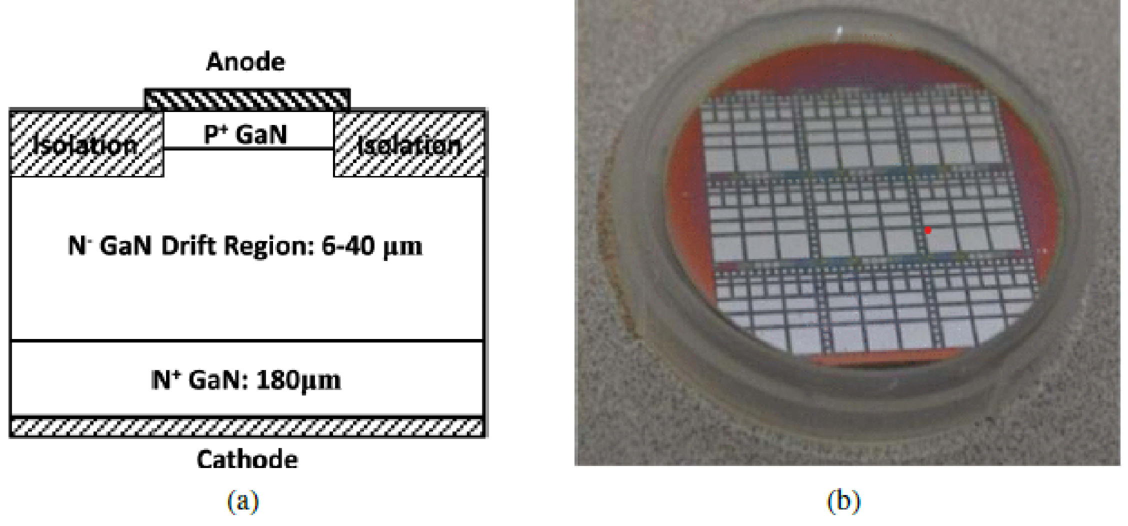


**Figure 1.10:** (a) Schematic structure of the p-i-n diode with implantation-based edge termination technology [66]. (b) Photography of fabricated diodes on the wafer.

In 2015, Ohta et al. reported the p-i-n diodes with a *BV* of 4.7 kV by using a structure with triple drift layer, along with various doping concentration. The drift layer adjacent

with p-GaN was just doped to $10^{15}$ /cm$^3$, as shown in **Fig. 1.11 (a).** The reduced electric field is attributed to the modulated flat electric field profile [67]. Furthermore, a guard-ring termination was continuously proposed to aforementioned p-i-n diodes, as shown in **Fig. 1.11 (b)**. A 200-V-enhanced *BV* of 5 kV was achieved by utilizing this edge termination technology [68].

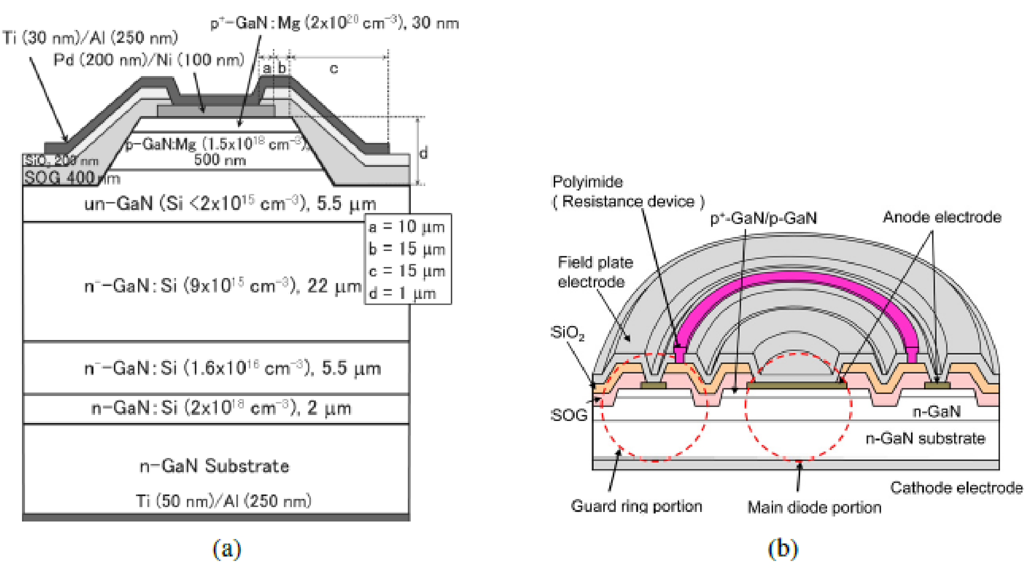


**Figure 1.11:** (a) Schematic structure of the p-i-n diode with a triple drift layer. (b) Guard ring edge termination for (a).

Hu et al. reported that GaN with a high crystal quality could largely affect the device performance, a low Shockley-Read-Hall (SRH) lifetime of 12 ns can be achieved by the p-

i-n diode in **Fig 1.12**. According that, an extremely low $R_{on,sp}$ of 0.12 mΩ·cm$^2$ was extracted, along with a $BV$ over 1400 V, leading to highest BFoM of 16.5 GW/cm$^2$ [69].

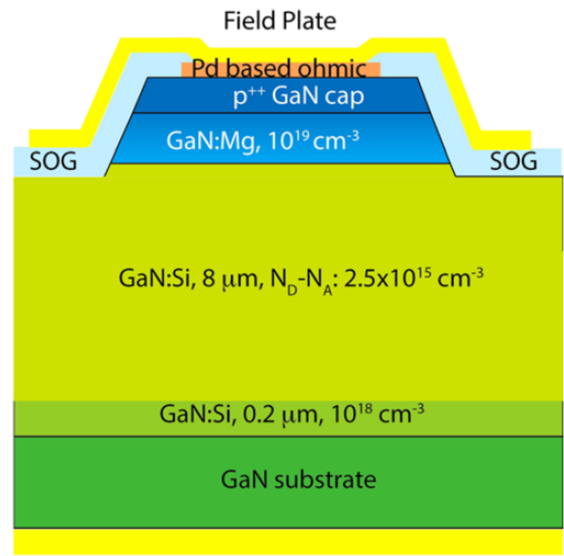


**Figure 1.12:** Schematic structure of the p-i-n diode with a record BFoM all the time [69].

Additionally, p-n diodes with different edge termination technologies have been extensively reported, and as-reported p-n diodes could exhibit competitive device performances, even beyond the limitation of GaN unipolar device predicted by BFoM, as summarized in **Fig. 1.13** [70-72]. At the same time, by virtue of the avalanche capability which has been achieved in aforementioned p-n diodes, some fundamental properties of GaN like impact ionization coefficients were systematically investigated [73-75].

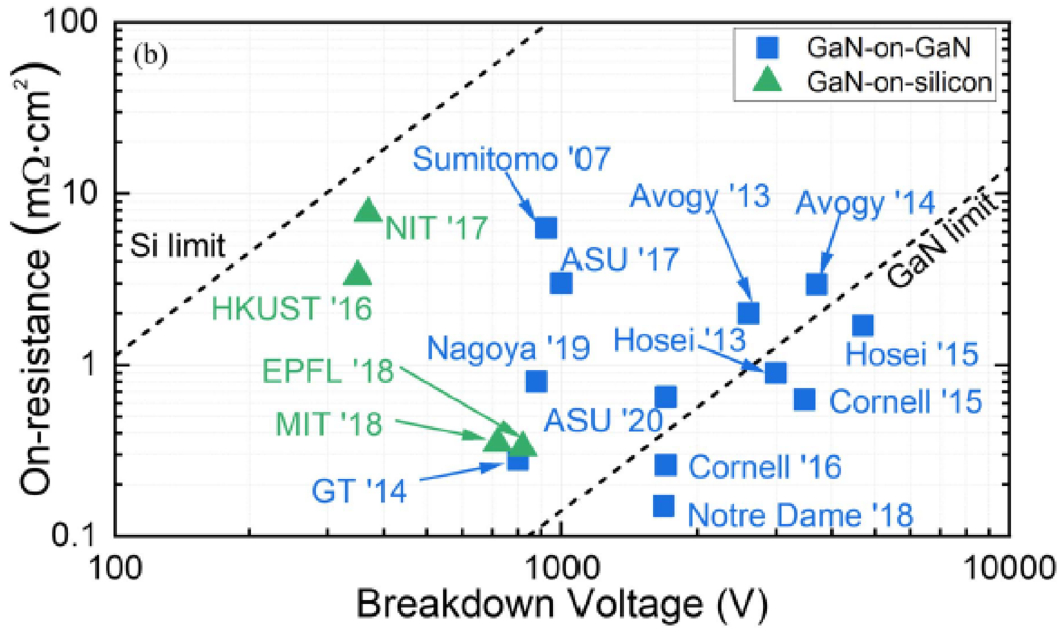


**Figure 1.13:** Benchmark of *BV* vs. $R_{on,\ sp}$ of reported vertical GaN PNDs [71].

### 1.3.5.2 SBDs

Sumitomo Electric Industries firstly reported the Power SBDs with a SiN field plated-based edge termination, as shown in **Fig. 1.14**. The fabricated could deliver a high *BV* over than 1000 V [76]. The growth conditions were discussed in detail, a $R_{on,sp}$ of 0.71 mΩ·cm$^2$ and a *BV* over 1100 V can be achieved simultaneously with the best-optimized growth condition. When a large anode size of 1.3 × 1.3 mm$^2$ was deposited, the new SBD delivered a high forward current of 6 A at 1.46V. And the *BV* was reduced to be ~ 600 V, which could be attributed to more threading dislocations under the large size anode.

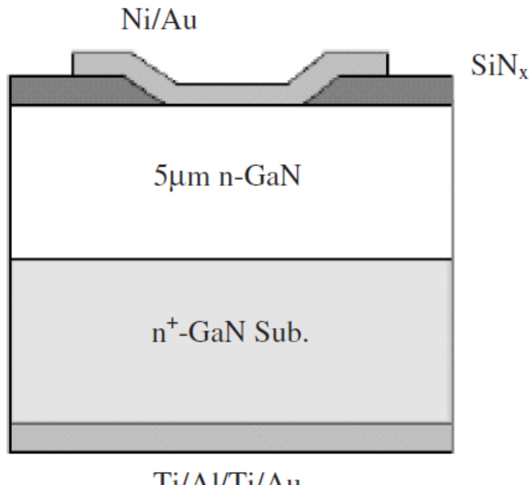


**Figure 1.14:** Schematic structure of the SBD with a SiN field plate-based edge termination [76].

Tanaka et al. proposed a 50 A/790 V SBD with a contact size of 1.3 × 1.3 $mm^2$ by using a wrap-around field plate, as shown **in Fig. 1.15** [77]. The results in forward conduction kept consistence with the thermionic emission (TE) theory, but the leakage current is still higher than the values calculated by a thermionic-field emission (TFE) theory.

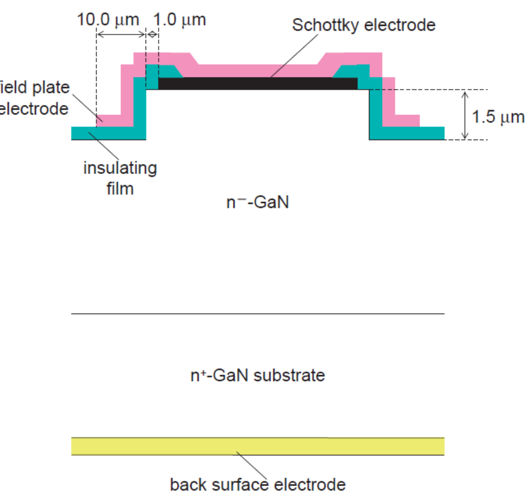


**Figure 1.15:** Schematic structure of the SBD with a wrap-around SiN field plate-based edge termination [77].

Cao et al. [78] reported an improved device performance by inserting an ultrathin tunneling AlGaN barrier, as shown in **Fig. 1.16.** The $V_{ON}$ will be effectively reduced from 0.77 to 0.67 V, still along with a high $BV$ of 700 V, showing a good trade-off between $V_{on}$ and $BV$.

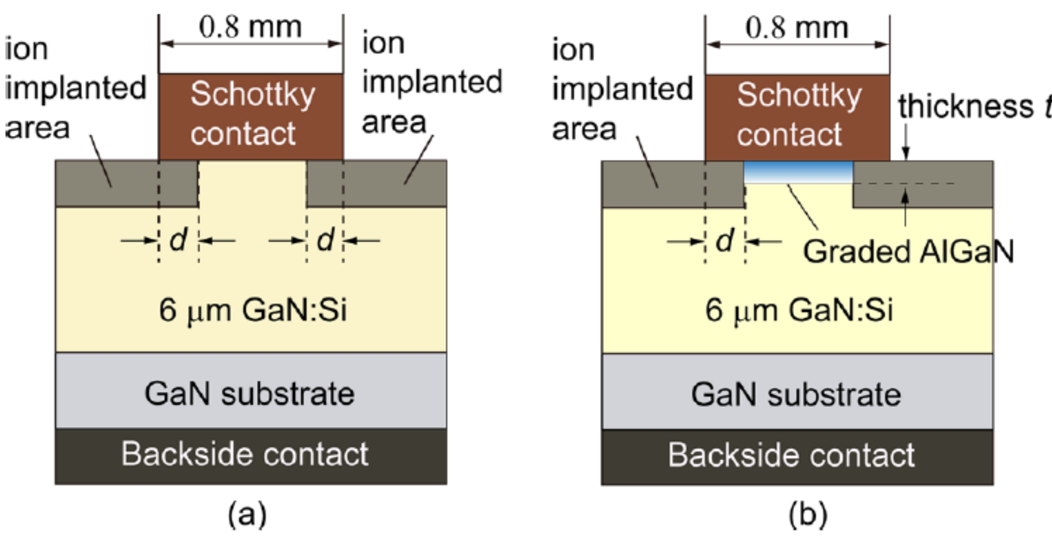


**Figure 1.16:** (a) Schematic structure of the SBD with an ion-implantation-based field plate. (b) AlGaN tunneling layer inserted SBD. [78].

Zhang et al. firstly reported GaN junction barrier Schottky (JBS) diodes by implanting Mg in n-GaN and Si in p-GaN [79], as shown in **Fig. 1.17**. For the JBS implanted by Si, a larger $R_{on,sp}$ of 7 ~ 9 mΩ·cm$^2$ was derived, along with a $BV$ of 600 V. And for the JBS implanted by Mg, the fabricated diodes exhibited a smaller $R_{on,sp}$ of 1.5-2.5 mΩ·cm$^2$, along with a $BV$ of 550 V. Unlike the SiC-based JBS, which can deliver excellent ON-/OFF-performance, more effort for GaN-based JBS including the optimization of pillar size and implantation technique is needed. Also, Li et al. reported trench-based JBS, the device

performance could be improved compared with reference SBD [80], but still need to be optimized. One of the biggest challenges is the low activation ratio for Mg-implanted GaN. The superior p-type region is crucial for JBS, which will form the lateral pn junction, moving the peak electric field from Schottky contact into bulk material under the reverse bias.

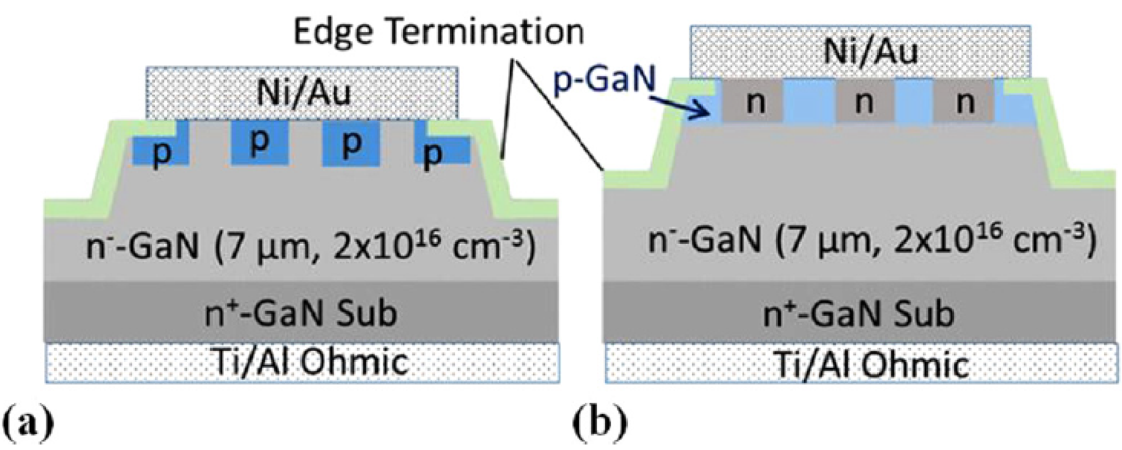


**Figure 1.17:** Schematic structure of JBSs: (a) JBS implanted by Mg. (b) JBS implanted by Si [79].

Trench MOS barrier Schottky (TMBS) devices was also proposed by Zhang et al, as shown in **Fig. 18** [81]. Furthermore, the influence of trench morphology on device performance of TMBS was simulated, and it was demonstrated the flat-bottom rounded vertical trench structure could be a better choice and practically fabricated [82]. In addition, it was proved the implanted field ring at the bottom corner of trench could largely suppress the leakage current. The fabricated TMBSs with optimizations could be successfully turned on and featured the improved the $BV$ ranging from 400 to 700 V.

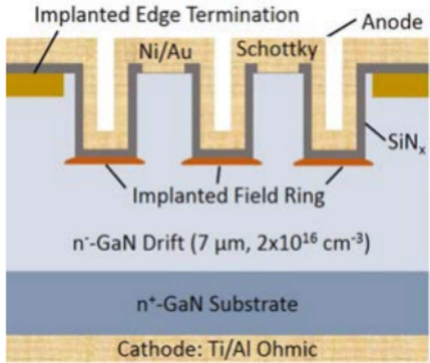


**Figure 1.18:** Schematic structure of TMBS with implanted field rings [81].

In addition to what we discussed above, the GaN-on-GaN SBDs with ion implantation (F/O/N/Ar)-based field plate have also been well investigated in the recent years [83-86]. **Figure 1.19** shows the schematic structure of the SBD with the field plate implanted by F ion [84]. With the negative fixed charges induced by F-based ion implantation near the device periphery, the crowding of electric field at the junction edge can be effectively alleviated, resulting in reduced reverse leakage current. The reported SBD could deliver a low $V_{ON}$ of 0.85 V and a high $BV$ of ~ 800 V.

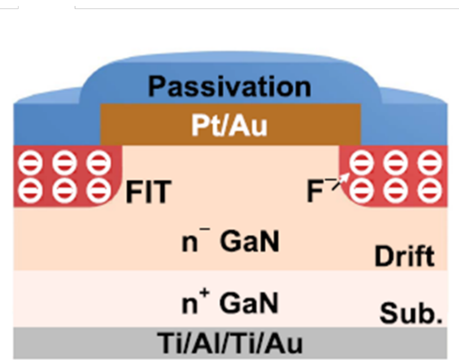


**Figure 1.19:** Schematic structure of the SBD with the F ion implantation-based field plate [84].

Furthermore, Y. Sun et al. summarized recent progress on vertical GaN SBDs with different edge termination technologies, as shown in **Fig. 1.20** [87].

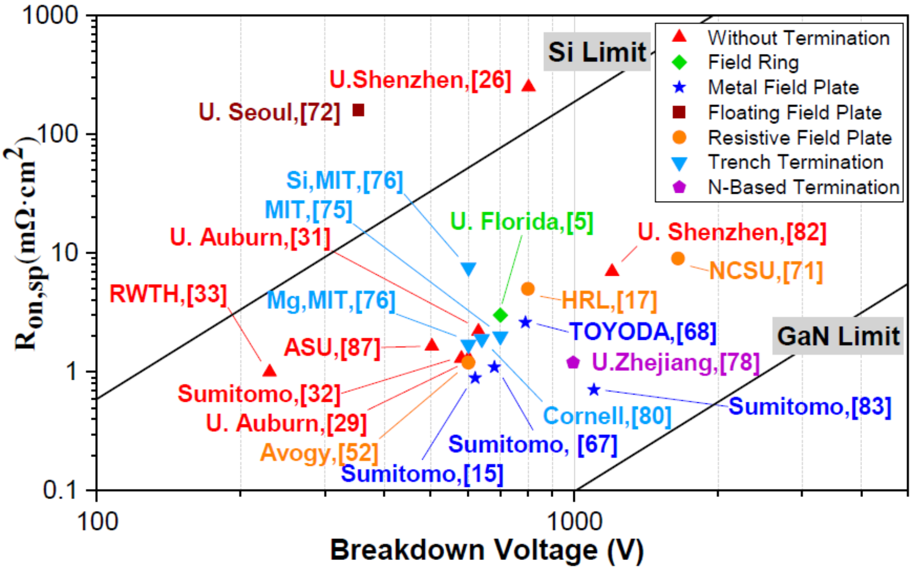


**Figure 1.20:** Benchmark of *BV* vs. $R_{on,\ sp}$ of reported vertical GaN SBDs [87].

## 1.4 Motivation and objective

Except for edge termination techniques, for achieving higher breakdown voltages, Reduced Surface Field (RESURF) concept is an extensively adopted design principle in power devices [88]. The conventional wisdom drawn from a RESURF principle-based super-junction (SJ) structure would be to realize the charge balance via stacked n-pillars and p-pillars which serve as the crucial building block for reshaping the distribution of potential/electric field in drift region under reverse bias, as shown in **Fig. 1.21** [89].

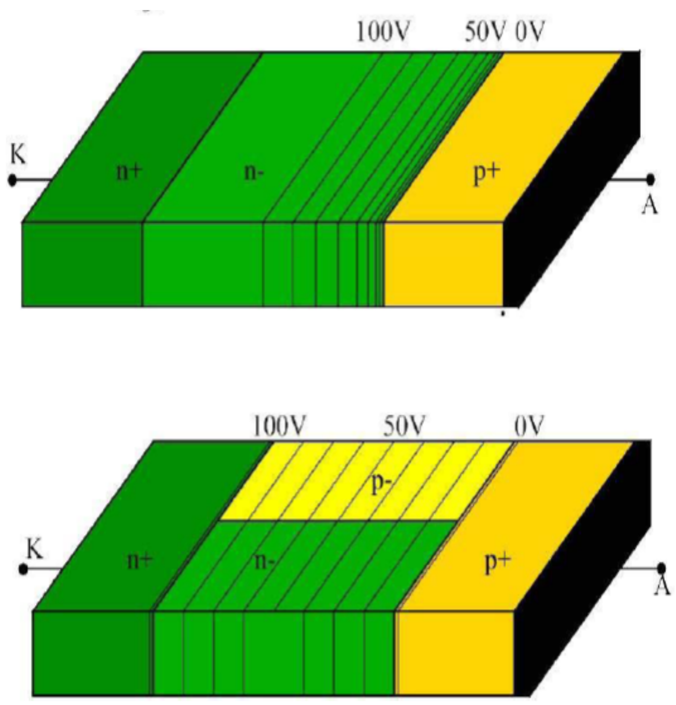


**Figure 1.21:** Potential distribution in a conventional p-n diode and a RESURF-based p-n diodes. [89].

To achieve the excellent performances of SJ structure-based power devices, the aforementioned precise charge balance is highly required, but it is not readily realized in the actual fabrication process. Thus, as another option, the dielectric RESURF concept was proposed, the narrow p-n junction with its surrounding fringing capacitors could also modulate the potential/electric field distribution in drift region under reverse bias to accomplish a higher breakdown voltage, as shown in **Fig. 1.22** [90].

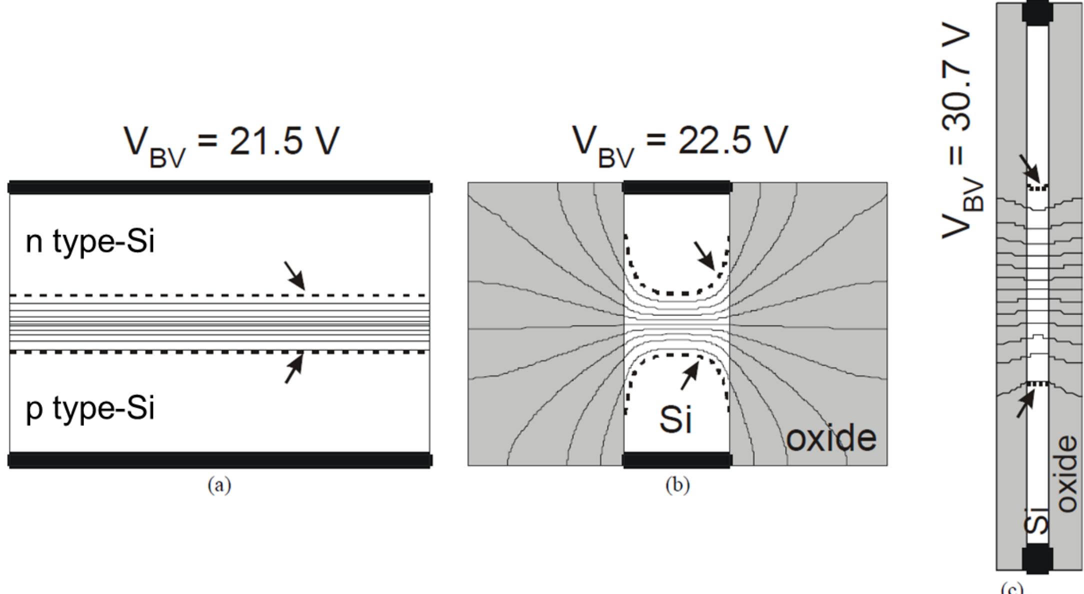


**Figure 1.22:** Potential distributions of (a) a conventional p-n diode, (b) a wide-and (c) a narrow-p/n diode surrounded with an oxide layer. [90].

As discussed in the last section, the device performance of GaN SBDs is typically hindered by high reverse leakage current and premature breakdown. To overcome these shortcomings, a substantial amount of research for high-voltage GaN-SBDs has been devoted to the development of edge termination techniques such as field plate, junction

barrier Schottky diode, trench MOS barrier Schottky diode, and others [76-87]. To further improve the device performance, it is also interesting to note whether GaN SBDs could achieve low reverse leakage current and improved $BV$ by taking advantage of RESURF concept. As another typical semiconductor with a wide bandgap, researches on SJ-based SiC SBDs have been studied and reported, the fabricated devices exhibited the improved reverse device performances [91, 92]. Nevertheless, it is challenging for GaN because of the difficult selective area doping of p-type GaN [93,94] and contaminated interface after epitaxial regrowth [95,96]. Alternatively, taking the full advantage of the dielectric RESURF principle, GaN nano/submicrostructure-based SBDs may provide a viable option for a better electric field management that is comparable to SJ-based power SBDs [97, 98], as illustrated in **Fig. 1.23**. Even though some simulation works and analytical studies were carried out, there are few reports on the practice device fabrication, optimization methods, and the characteristics of dielectric RESURF based-GaN SBDs.

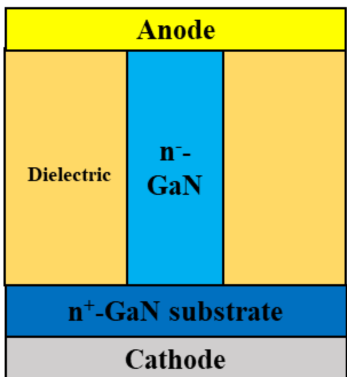


**Figure 1.23:** Schematic structure of dielectric RESURF-based GaN SBD.

In this dissertation, the author studies on NR-based vertical GaN-on-GaN SBD fabricated by top-down approach. In Chapter 1, the background, the outstanding issues, and the motivation for this study are described.

In Chapter 2, a review of the feasible approaches for fabricating GaN nanostructures as well as the relevant process/characterization facilities will be provided.

Chapter 3 proposes an etching-based top-down approach to fabricate GaN NRSBD. Based on Silvaco TCAD simulations, the author indicates GaN NR/NW structures can benefit from the dielectric RESURF effect, and therefore may be considered as an alternative to high-voltage SBDs. Additionally, the practice fabrication of NR (mesa)-SBDs was completed by the top-down approach. The dielectric RESURF effect on NRSBDs is demonstrated, which is consistent with the simulation results.

Due to the adverse effects of the $CF_4/O_2$-based etch-back process, non-ideal carrier transportation is confirmed at the Schottky interface in the fabricated SBDs. As a solution to this problem, an optimization based on a low-damage etch with a low bias voltage and a post-annealing process was utilized. The recovered device performance demonstrated the effectiveness of the optimization process.

Chapter 4 introduces the optimized dry- and wet-etching process, a more deliberated process flow for NR fabrication. The vertical NR with high aspect ratio and distinct non-polar sidewall can be obtained by following the optimizations. Furthermore, the NRSBDs fabricated by new process features improved and competitive device performance. In addition, the evaluation for SBH values of NRSBDs, as well as the importance of wet-etching process are systematically studied by both static and dynamic characteristics.

A brief summary of this study is provided in Chapter 5.

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# Chapter 2 Fabrication of nanostructure and related process techniques

**2.1** Introduction

**2.2** Selection of the fabrication approach of GaN nanorod

**2.3** Process techniques

**2.4** Characterization techniques

References

## 2.1 Introduction

In this chapter, the typical fabrication methods of GaN NRs were firstly discussed. In this study, the top-down approach, which is mainly based on etching process, was selected to fabricate GaN NRs. GaN-on-GaN vertical epitaxial structures was prepared by MOCVD system. The various process equipment involved in the top-down approach were also shortly summarized, including electron-beam (E-beam) lithography, inductively coupled plasma-reactive ion etching (ICP-RIE) and so on. The morphology of GaN NRs was investigated by scanning electron microscopy (SEM). After device fabrication, Current-voltage (*I*-*V*) and Capacitance–voltage (*C*-*V*) characteristics were employed to evaluate the electric properties of epitaxial structures and fabricated devices.

## 2.2 Selection of the fabrication approach of GaN nanorod

As far as what has been discussed in Chapter 1, due to the excellent material properties of GaN, GaN-based devices have been becoming a competitive candidate for future power electronics. And GaN NR is a potential solution to further realize some novel vertical GaN power device concepts. There are two typical methods for the fabrication of GaN NR, one is the selective area epitaxial growth-based bottom-up approach, which is spontaneously synthesizing nanorods according to the nucleation theory, the other one is top-down approaches by combining proper photolithography technology and etching process.

For bottom-up approach, there are several proper systems for the epitaxial growth of NW/NR, such as MOCVD [1, 2], HVPE [3], molecular beam epitaxy (MBE) [4,5]. The biggest advantage of bottom-up approach is that it can almost overcome lattice mismatches between GaN and variety of foreign substrates during growth, offering the GaN NR with high crystalline quality (effective reduction of formation of dislocations) [6-8]. However, despite the excellent material quality in those fabricated GaN nanostructures, there are still some disadvantages to utilize the NRs fabricated by bottom-up method for vertical power devices. Firstly, a large-scale array of NRs with uniform morphology (size, height, non-faceted) is highly desired for vertical power devices. This requirement becomes challenging for bottom-up approach because of the complicated growth conditions. Additionally, high level impurities may be introduced under the optimized growth conditions, causing difficulties to control the carrier concentration in the NRs grown by bottom-up approach [9]. For example, for the epitaxial growth of NRs higher than 5μm, the high flow rate of silane is normally required [10], causing in unprecise control of Si.

And the precise control of net doping concentration is highly required for drift layer of GaN power devices. Besides, a matured technology to precisely measure the doping concentration like Secondary-ion mass spectrometry (SIMS) is still lacked for the nanostructures. Accordingly, the bottom-up approach will be not selected to fabricate GaN NRs in this work. Alternatively, the etching-based top-down approach with the optimized process conditions can basically satisfy the aforementioned requirements, so it will be regarded as a more suitable approach to fabricate the nanostructures for vertical power devices in this thesis.

In the next sections, the equipment, which is frequently used during top-down approach, will be briefly introduced. And some experimental conditions for top-down fabrication will also be listed.

## 2.3 Process techniques

### 2.3.1 MOCVD set-up

One of the most widely used technique for crystal epitaxial growth is the MOCVD system, which has been extensively developed over the past few decades. In this work, the MOCVD built by Nippon Sanso Holdings corporation was employed to accomplish epitaxial growth of GaN. **Figure. 2.1** shows the photograph of the MOCVD system used in this work. The reactor chamber of epitaxial growth inside the MOCVD system is assembled with a horizontal configuration.

**Figure 2.1:** Photograph of MOCVD set-up.

As shown in **Fig. 2.2**, the MO/ammonia ($NH_3$) source and nitrogen ($N_2$)/hydrogen ($H_2$) can firstly be injected into the reactor chamber by gas lines, and the reaction processes (gas reaction and surface reaction) are subsequently proceeded. Finally, the GaN crystal film can be grown on the substrate in the MOCVD system. With the optimized growth conditions, the thickness of flat GaN epi-layer, which is tightly correlated with supply amount of source material, can be well controlled ranging from several nanometer (nm) to the scale of micrometer (μm). Furthermore, the doping concentration of n-type GaN in this MOCVD system can be precisely controlled as low as $\sim 5 \times 10^{15}/cm^3$, which is desired for GaN-based power electronics.

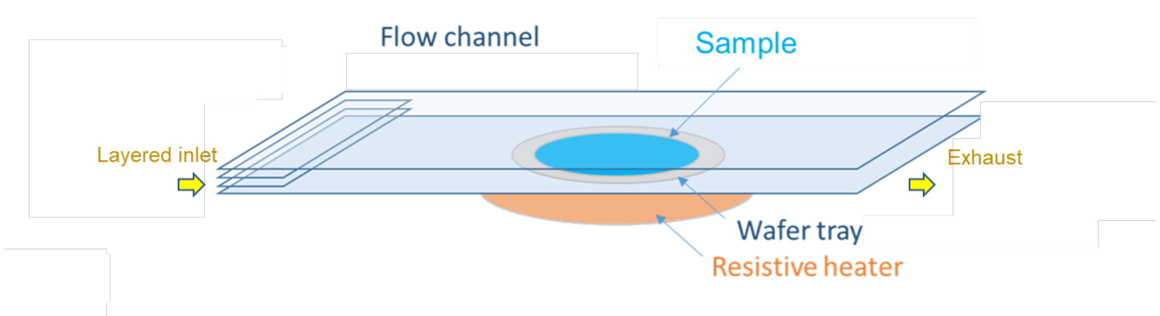



**Figure 2.2:** Schematic diagram of the reactor chamber inside MOCVD system.

### 2.3.2 Electron-beam (E-beam) lithography system

In this thesis, it is difficult to obtain the uniform patterns with the size smaller than 2 μm by our available photolithography facilities including contact aligner photolithography and mask-less photolithography. To fabricate microstructure and nanostructure-based devices, the E-beam lithography is in this work frequently utilized to draw. It is reported that the E-beam lithography system can readily make the patterns with a feature size around 10 nm [11]. **Fig. 2.3** shows the photograph of the E-beam lithography system (JEOL JBX-6300FS) utilized in this work. And the operation steps are summarized as follow:

1. Sample cleaning: the samples were carefully cleaned by following a standard set of wafer cleaning steps (details in section 3.3.1 in Chapter 3) and then dried by pure $N_2$ and hot plate.
2. E-beam resist spin-coating: after waiting the samples to the room temperature, E-beam resist (ZEON ZEP520A) is spin-coated with a rotation speed of 5000 rpm, the thickness of E-beam resist is around 300 nm.
3. Pre-bake: the baking is proceeded on the hot plate with a temperature of 170 ˚C for 5 min.
4. Alignment and exposure: the exposure was completed in the E-beam lithography system, and **Fig. 2.4** depicts simplified schematic structure of JEOL JBX-6300FS [12]. The system can generate a high-density electron beam using a thermal field emission gun with a ZrO/W emitter at 100 kV acceleration voltage. An electron beam with high density can be generated by in this system by a ZrO/W emitter-based thermal field emission gun at an accelerated voltage of 100 kV. The beam current level was adjusted to 2 nA.

5. Development: O-xylene is used as the development solution at room temperature for the E-beam resist after the exposure. The development time is 2 min, and then the samples were rinsed by IPA for 1 min and finally dried by $N_2$.

Figure. 2. 4 shows SEM image of the circle hard mask patterns with a diameter ranging from 200 nm to 800 nm.

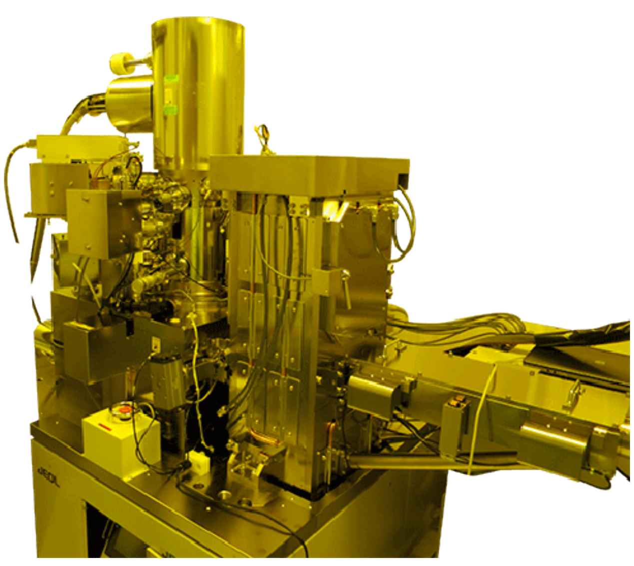


**Figure 2.3:** Photograph of the E-beam lithography system (JEOL JBX-6300FS).

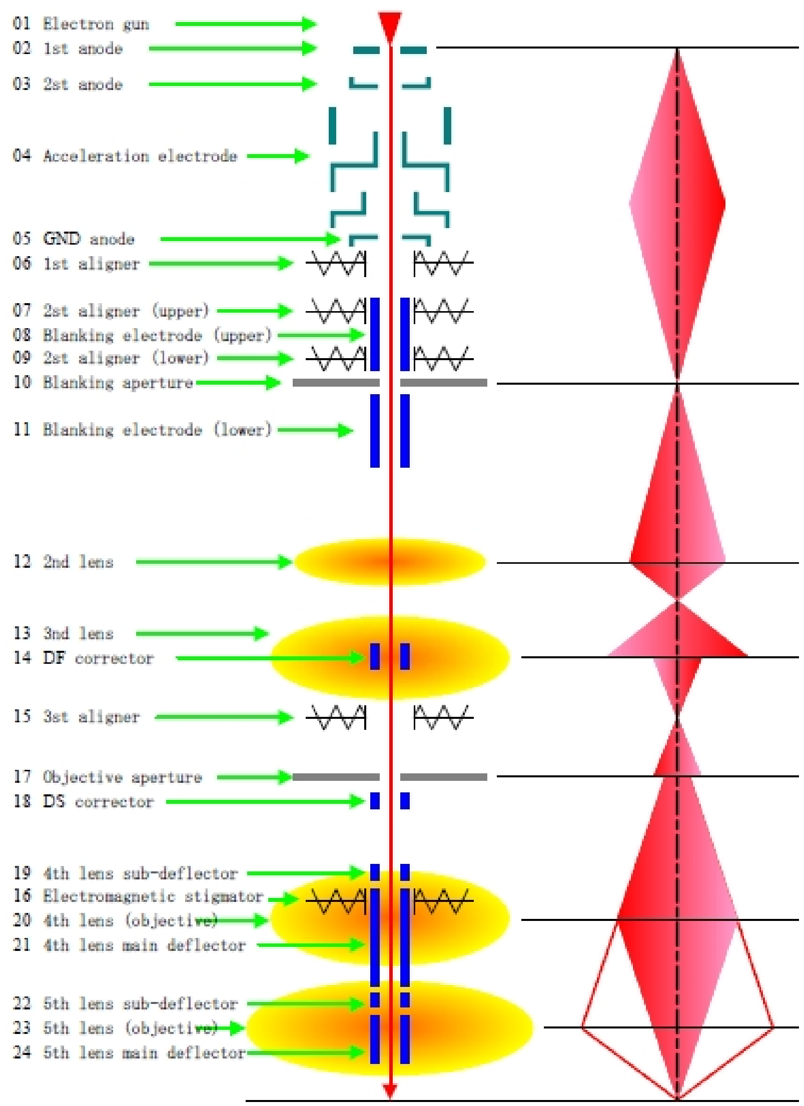



**Figure 2.4:** Simplified schematic structure of JEOL JBX-6300FS.

### 2.3.3 ICP-RIE system

As to GaN nanostructure-based devices fabricated by top-down approach, the reactive ion etching (RIE) system take an important role. As we know, both radicals-based chemical etching and ion-based physical etching can be involved in RIE system. In this work, two kinds of RIE system facilities were frequently utilized. One is the parallel plate reactive ion etching system (RIE-10NR, **Fig. 2. 5 (a)**) from Samco Inc., which is mainly used to etch some dielectrics like SiN, $SiO_2$, and polyimide. The other one is the ICP-RIE system (CE-300I), which is utilized to etch GaN NRs, from ULVAC Inc., as shown in **Fig. 2. 5 (b)**. The biggest difference between two systems is that the plasma with a higher density can be generated by the individual ICP source in ICP-RIE system. Furthermore, unlike a single RF power supply in the parallel plate reactive ion etching system, two RF power supplies inside ICP-RIE system can feature the independent control of radicals and ions, resulting a good balance between chemical and physical etching.

The experimental conditions of $Cl_2$-based dry-etching process for GaN are listed in **table 2.1**. The etching rate is around ~ 2.5/3.3 nm/s with a bias power of 20/30 W.

**Table 2.2(a)** lists the experimental conditions of $CF_4$-based dry-etching process for $SiO_2$. The etching rate is around ~ 40 nm/min. And **table 2.2(b)** lists the experimental conditions of $CF_4/O_2$-based dry-etching process for polyimide. The etching rate is around ~ 200 nm/min.

**Figure 2.5 (a):** Parallel plate reactive ion etching system (RIE-10NR).

**Figure 2.5 (b):** ICP-RIE system (CE-300I).

| **Parameter (unit)** | **Value** |
|---|---|
| Gas chemistry | $Cl_2$ |
| Gas flow rate (sccm) | 30 |
| ICP power (W) | 150 |
| Bias power (W) | 20~30 |
| Chamber pressure (Pa) | 1 |

**Table 2.1:** Experimental conditions of $Cl_2$-based dry-etching process for GaN in ICP-RIE system.

(a)

| **Parameter (unit)** | **Value** |
|---|---|
| Gas chemistry | $CF_4$ |
| Gas flow rate (sccm) | 20 |
| Bias power (W) | 100 |
| Chamber pressure (Pa) | 4 |

(b)

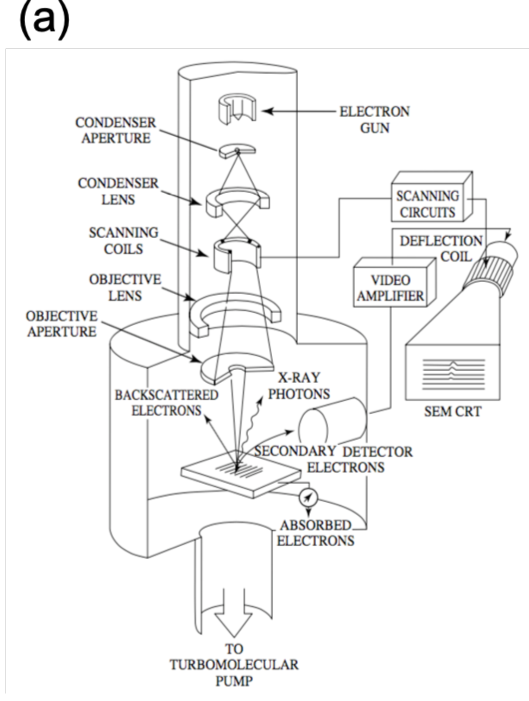
| **Parameter (unit)** | **Value** |
|---|---|
| Gas chemistry | $CF_4/O_2$ |
| Gas flow rate (sccm) | 20/10 |
| Bias power (W) | 150 |
| Chamber pressure (Pa) | 2 |

**Table 2.2:** Experimental conditions of dry-etching process for **(a)** $SiO_2$ and **(b)** polyimide in parallel plate reactive RIE system.

# 2.4 Characterization techniques

## 2.4.1 Scanning electron microscope (SEM)

In the area of material characterization, SEM is one of the most effective and common techniques. **Fig. 2. 6 (a)** shows the simplified schematic diagram of a typical SEM system [13]. Firstly, by applying a given voltage, the electron gun can generate a beam of electrons. These emitted electrons can be focused by condenser lenses, pass through a sequence of lenses, and subsequently begin to scan over the sample surface. Finally, the secondary electrons, which is commonly used to analyze the surface morphology of samples, can be received after the interaction between the primarily emitted electrons and the atoms of measured sample. Besides, other kind of signals can be used to investigate chemical composition and crystal orientation. In this work, the SEM system (Hitachi S4300) is used to check the morphology of GaN NRs and key steps during the fabrication.



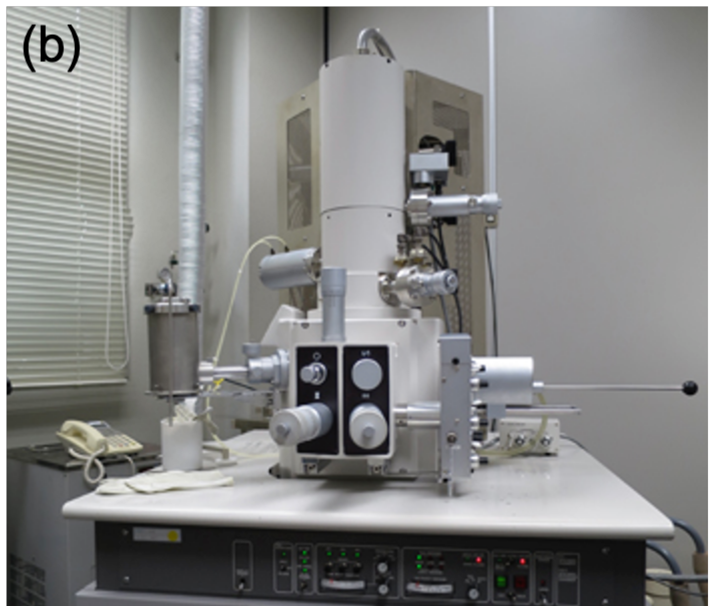
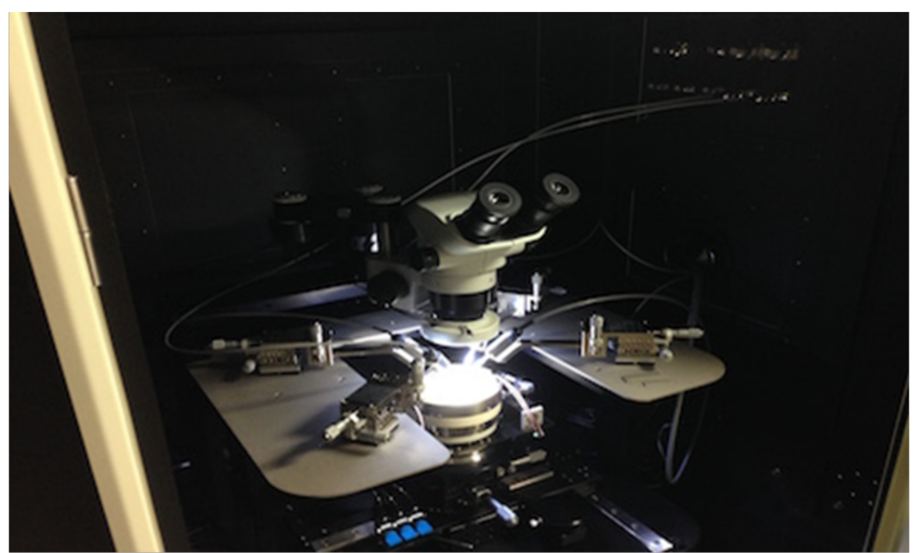



**Figure 2.6:** (a) Schematic of SEM principle with constituting optics [5]. (b) Schematic of electron beam interacts with atoms at the sample surface, resulting in different process [6]. (c) Photograph of Hitachi, S-4300 SEM system used in this work.

### 2.4.2 Electrical characterization

The *I-V* and *C-V* characteristics are carried out to measure the fabricated devices, **Fig. 2.7 (a)** and **(b)** show the photography of power device analyzer and probe used in this work. The Keysight B1505A Power Device Analyzer/Curve Tracer could enable precise evaluations and characterizations for power devices with a high voltage up to 10 kV and a high current up to 1500 A. The B1505A offers a series of measurement capabilities for

power devices, including a broad voltage and current range, fast pulsing capability, sub-pA level current measurement and on-resistance measurement resolution at a μΩ level.



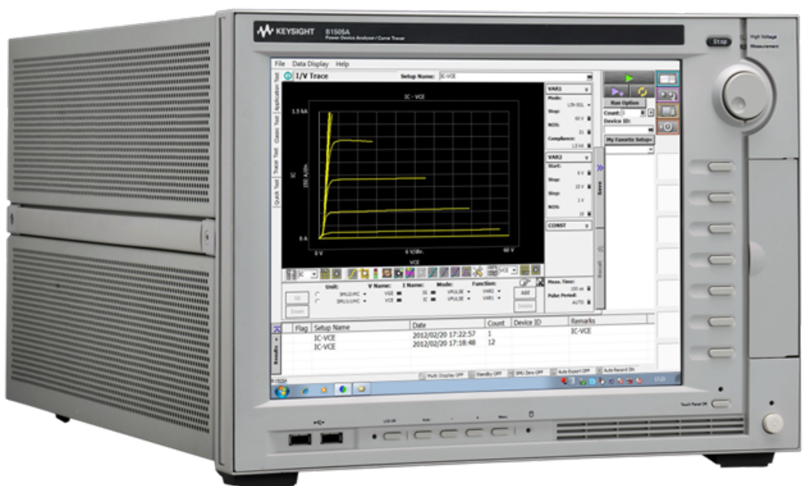



**Figure 2.7:** Photography of Keysight B1505A Power Device Analyzer and Probe.

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# Chapter 3 Dielectric Reduced Surface Field Effect (RESURF) on Vertical GaN-on-GaN Nanorod Schottky Barrier Diodes (SBDs)

**3.1** Introduction

**3.2** Dielectric RESURF effect on NRSBDs

**3.3** Fabrication of vertical GaN-on-GaN NRSBDs

**3.4** Consideration and optimization for device fabrication

**3.5** Summary

References

## 3.1 Introduction

Previously, the researches about nanoscale GaN structures, including nanowire/nanorod (NW/NR) and Fin structures, were mainly related to the research about extraction of intrinsic electrical properties [1-2], LEDs [3-5], and lateral GaN devices [6, 7]. With the emergence of high-quality free-standing GaN substrate, NW/NR and Fin structures have enabled the implementation of vertical GaN device concepts such as E-mode MOSFETs [8,9], FinFETs [10,11], and superjunctions (SJs) [12]. Furthermore, it is also interesting to note that the NR-based structure could serve as another choice to achieving low reverse leakage current and improved $BV$ for SBDs, because this structure can readily take full advantage of dielectric RESURF principle [13,14], as discussed in Chapter 1.

In the Chapter 2, it has been briefly discussed that the bottom-up approach-based selective area growth of nanostructures is not suitable for vertical GaN power devices. On the other hand, the etching-based top-down approach has been regarded as a more proper method to fabricate the GaN nanostructures-power devices because of the capability to precisely control doping concentration in the drift region.

In this chapter, the reason why GaN NRSBDs could exhibit an improved device performance under the reverse bias is firstly discussed based on simulation studies. Furthermore, the GaN NRSBDs were fabricated, a suppressed leakage current and an enhanced $BV$ can be confirmed in the GaN NRSBDs, compared with large-diameter/planar SBDs (fabricated simultaneously using a top-down fabrication), providing the evidence of the dielectric RESURF effect on GaN NR structures. However, a relatively large ideality factor (n) and a high $V_{ON}$ were presented in these devices, which are likely caused by an $CF_4/O_2$-based etch-back process prior to the deposition of top Schottky contacts. The

mentioned drawbacks indicate that further optimization of device fabrication of NRSBDs is required.

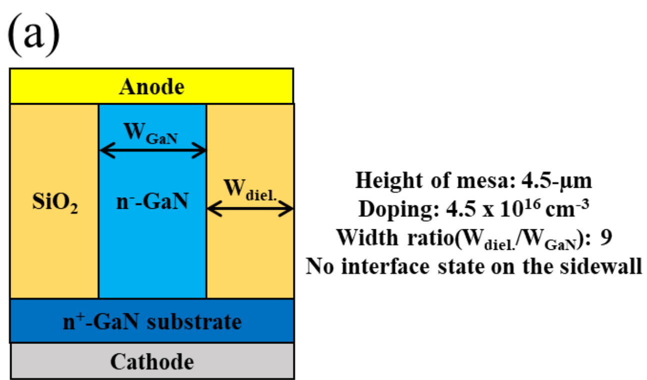
To solve the negative effect from etch-back process and obtain a better Schottky contact with a higher quality, a low-bias-power $Cl_2$-based plasma etching is applied to the top area after $CF_4/O_2$-based etch-back process, followed by post-metallization rapid thermal annealing (RTA). It was confirmed the NRSBDs treated with the additional optimized processes could deliver the recovered device performance.

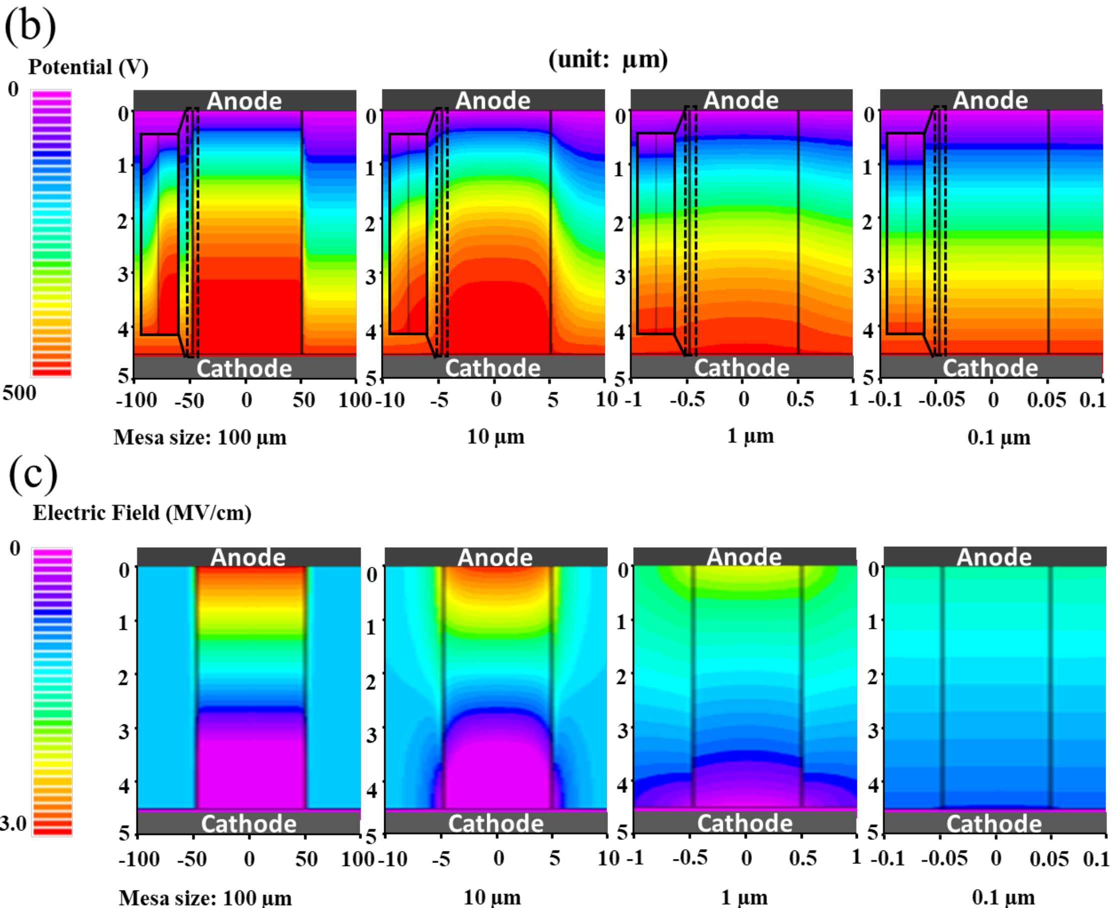
## 3.2 Dielectric RESURF Effect on NRSBDs

As what has been discussed in the Chapter 1, G. Sabui et al. reported the work about simulation for GaN NWSBDs by Sentaurus TCAD [15], this simulation was mainly focusing on how the width of GaN and adjacent $SiO_2$ affects the device performance. In this work, the simulation of SBDs is also carried out using Silvaco TCAD, but the primary target is to investigate how NRSBDs can take advantages from dielectric RESURF effect under a given reversed-bias voltage.

**Figure 3.1 (a)** depicts a schematic diagram of device model in the simulation, where the thickness and the net doping concentration of GaN were set to be 4.5 μm and $4.5 \times 10^{16}/cm^3$, respectively. Four different widths of GaN were selected to be 100, 10, 1, 0.1 μm. To investigate the size dependence of dielectric RESURF effect on NW/NR and larger-size mesa structure, the width of surrounding dielectric was fairly adjusted to keep the same width ratio ($W_{GaN}/W_{diel.} = 1/9$). This low width ratio of GaN to dielectric was aimed to induce a strong dielectric RESURF effect. When a high reverse bias (500 V in this simulation) was applied, with shrinking GaN width to submicro/nanoscale dimensions, the electric potential distribution within GaN was susceptible to be modulated by the surrounding dielectrics, as shown in **Fig. 3.1 (b)**. Moreover, **Fig. 3.1 (c)** delineates the distribution of electric field, where the electric field gradient along axial direction of GaN nanowire was reduced as a result of the fringing effect between GaN and surrounding dielectric material. **Figure 3.1 (d)** shows the extracted electric field strength at the interface of Schottky junction for different cases, in which the simulated values were obviously

reduced from 3 MV/cm to 1.6 MV/cm when the width of GaN region was scaled down from 100 to 0.1 μm, resulting in greatly reduced reverse leakage current.



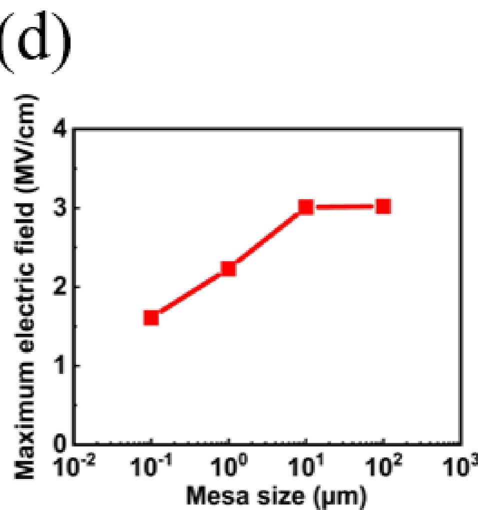



**Figure 3.1:** (a) Schematic structure in Silvaco TCAD simulation. (b) Simulated electric potential distribution at a reverse bias of 500 V, where the narrow areas delineated by the dotted lines are enlarged in the black-line boxes on the left side to show more clearly the distribution of electric potential across the GaN/dielectric interface. (c) Simulated electric field distribution at a reverse bias of 500 V. (d) Electric field strength at the interface of Schottky junction for different widths of the GaN region.

## 3.3 Fabrication of vertical GaN-on-GaN NRSBDs

### 3.3.1 Sample preparation

Firstly, the epitaxial structure used in this chapter featured a 4.5-μm-thick $n^-$-GaN drift layer on 2-inch HVPE-grown $n^+$-type (Si-doped to $2 \times 10^{18}/cm^3$) GaN substrate. After the epitaxial growth, the samples were strictly cleaned following to an RCA clean procedure as follow:

1. Acetone for 5 min in an ultrasonic bath.
2. Methanol for 5 min in an ultrasonic bath.
3. Semicoclean for 10 min in an ultrasonic bath.
4. Piranha solution for 10 min at 120 ˚C and rinse in DI water.
5. First step of standard clean (SC-1) for 10 min at 80 ˚C and rinse in DI water.
6. Aqueous HF for 1 min and rinse in DI water.
7. SC-2 for 10 min at 80 ˚C and rinse in DI water.
8. Rinse in DI water.

**Figure 3.2 (a)** shows the schematic illustration of an un-terminated reference SBD (UTR-SBD), the net doping concentration ($N_D$-$N_A$) in the n$^-$-GaN drift layer is extracted to be ~ 4.5 × 10$^{16}$/cm$^3$ from the capacitance-voltage (*C*-*V*) characteristics (**Fig. 3.2 (b)**) at a frequency of 1 MHz, according to

$$N_D - N_A = -\frac{2}{q\varepsilon_s\varepsilon_r}\cdot\frac{dV}{d(1/C^2)}$$

where $q$, $\varepsilon_r$, $\varepsilon_s$, $N_D$ and $N_A$ are the electron charge, the permittivity of vacuum, the relative permittivity of GaN, donor and acceptor concentration in the n$^-$-GaN drift layer., respectively.

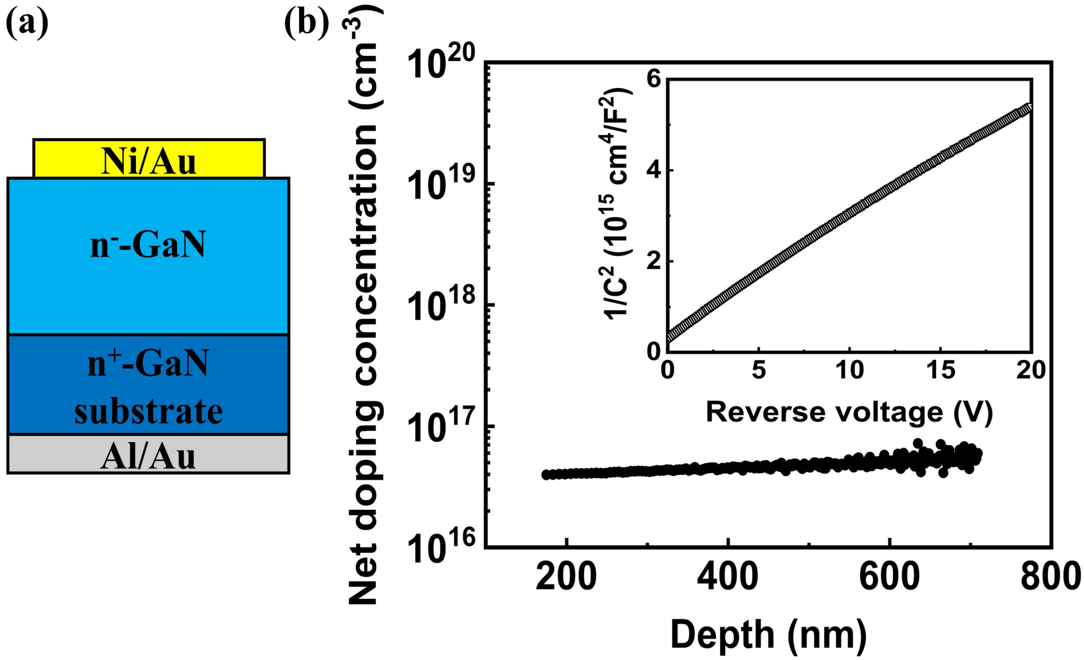



**Figure 3.2:** (a) Schematic structure of the UTR-SBD. (b) Extracted net doping concentration ($N_D$-$N_A$) in the drift layer. Inset: *1/C²* versus reverse voltage.

### 3.3.2 Device fabrication

**Figure 3.3** shows the basic fabrication process flow of the SBD by top-down approach. At the beginning, an E-beam lithography was utilized to form circular patterns with 1-µm-diameter/10-µm-pitch size and 10-µm-diameter/100-µm-pitch size in a square-array arrangement for NRSBD and single-mesa SBD, respectively. A 150-nm-thick Ni film was deposited by E-beam evaporation as a hard mask for dry etch. After lift-off process, a pure $Cl_2$-based ICP-RIE dry etch with a bias power of 30 W was performed to form NR or mesa structures with a height of 4.5-µm. Subsequently, 80°C alkali-based developer AZ400K was used to trim down the NR and mesa by removing the plasma-damaged surface layer on the sidewalls and the diameter of NR was shrunk to be 800-nm. After removal of hard mask, polyimide was spun on the sample to fill the gaps adjacent to the NWs. Polyimide was cured at 350°C for 4 hours. Afterwards, a $CF_4/O_2$-based plasma etch-back process in RIE with an RF power of 150W was employed to remove the polyimide on top and expose the top area of the NRs array. Finally, Ni/Au and Al/Au stacks were deposited on the top and backside of GaN substrate, respectively, as the Schottky and Ohmic contacts. As a result, two kinds of SBDs: 100 × 800-nm-diameter NWs SBD (denoted as 800-nm-NRSBD), and 10-µm-diameter single-mesa SBD (denoted as 10-µm-mesa SBD) were fabricated simultaneously.

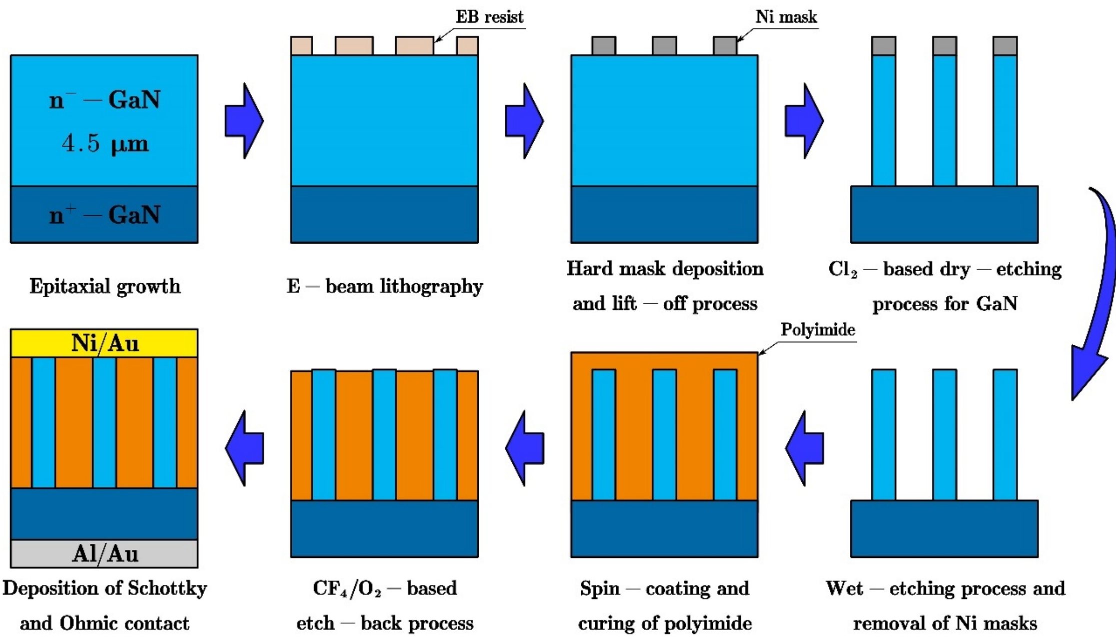



**Figure 3.3:** The basic fabrication process flow of the SBD by top-down approach.

### 3.3.3 Experimental results

**Figure 3.4** shows the linear-scale forward current-voltage (*I-V*) characteristics of the 800-nm-NRSBD and 10-μm-mesa SBD. The current density and differential $R_{on}$ are normalized by the active device area (top area of 100 × 800-nm-diameter NRs and single 10-μm mesa), which is approximately equal to 5.03 × $10^{-7}$ /7.85 × $10^{-7}$cm$^2$ for NRSBD/mesa SBD, respectively. Both SBDs can be successfully turned on with a high degree of consistency, exhibiting a forward current density over 1 kA/cm$^2$ under 2.2 V.

Relatively low differential $R_{on}$ of 0.15 and 0.13 m$\Omega$·cm$^2$ were calculated for the 800-nm-NRSBD and 10-µm-mesa SBD, respectively, at a forward bias of 3 V.

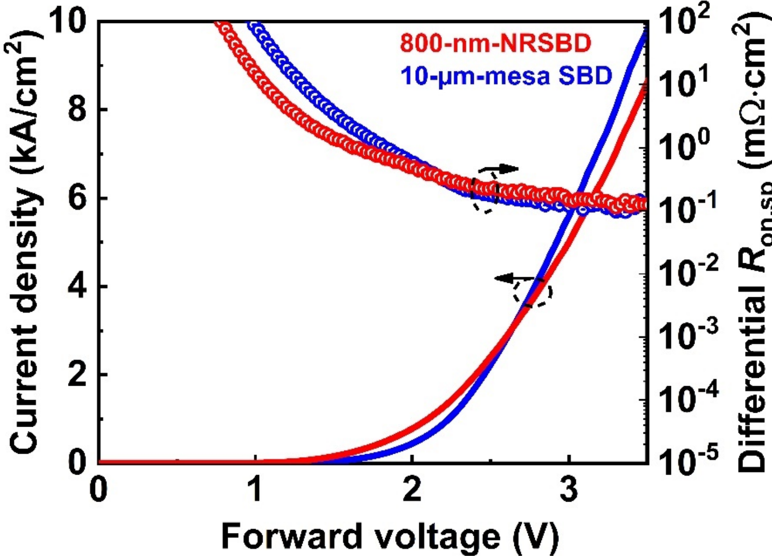



**Figure 3.4:** Left y-axis: Current-voltage (*I-V*) characteristics in linear scale of 800-nm-NRSBD (red) and 10-µm-mesa SBD (blue). Right y-axis: Extracted differential $R_{on}$ of both SBDs.

However, relatively large, quickly increased ideality factors from unity are extracted at low forward bias for both SBDs as shown in **Fig. 3.5**, indicating an unexpected carrier transport mechanism. Generally, the electrical performance of a Schottky contact is tightly determined by its interface quality and a non-unity ideality factor can be attributed to several reasons including Schottky barrier tunneling current, interface inhomogeneity, series resistance of quasi-neutral region [16-18]. For a reasonable assumption, the increased ideality factor in our case is more likely to be caused by $CF_4/O_2$-based plasma

etch-back process because the top GaN surface is directly exposed to the plasma during the etch-back process.

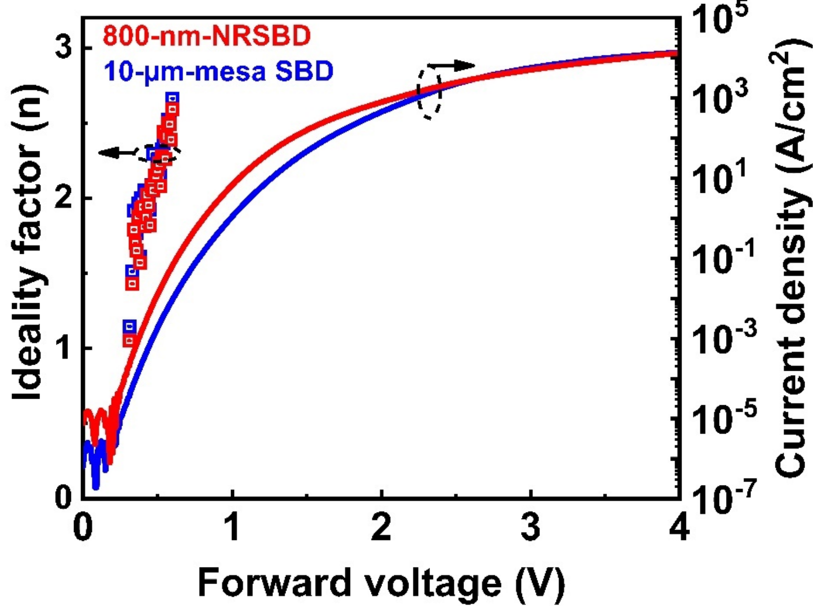



**Figure 3.5:** Left y-axis: Extracted ideality factor of both SBDs. Right y-axis: Comparison of *I-V* characteristics in semi-log scale of 800-nm-NRSBD (red) and 10-μm-mesa SBD (blue).

Both 800-nm-NRSBD and 10-μm-mesa SBD exhibit a similar forward conduction performance. Intriguingly, in the representative reverse *I-V* characteristics, as shown in **Fig. 3.6**, the 800-nm-NRSBD shows greatly suppressed leakage current (~ $10^4$ lower at around 200V) and improved soft *BV* (defined at the current density over 0.05 A/cm$^2$) of ~515 V

compared with the 10-µm-mesa SBD (~143 V in *BV*), which is consistent with the simulation result. The improved reverse performance indicates NR/NW-based SBD can favorably take an advantage from dielectric RESURF principle.

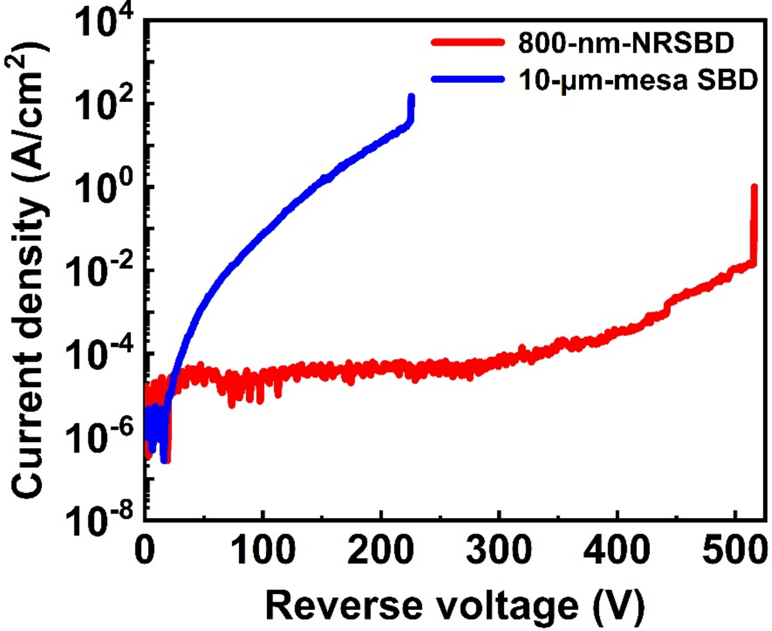



**Figure 3.6:** Reverse *I-V* characteristics of 800-nm-NRSBD (red) and 10-µm-mesa SBD (blue).

# 3.4 Consideration and optimization for device fabrication

## 3.4.1 Influence of $CF_4/O_2$-based etch-back process on GaN surface

To clarify the impact of $CF_4/O_2$-based etch-back process on the GaN surface, two un-terminated reference SBDs (UTR-SBD) were prepared, a 1-min-plasma treatment with the identical experimental parameters of etch-back process in the RIE system was just applied to one UTR-SBD prior to the Schottky contact deposition. **Figure 3.7** plots the forward current-voltage (*I-V*) characteristics of the UTR-SBD with plasma treatment and the ideal UTR-SBD without plasma treatment. The untreated UTR-SBD distinctly delivers a much higher current level, and a near-unity n of 1.02 can be extracted, while the UTR-SBD treated with the etch-back process exhibits an apparent reduction of current level at low forward bias with a much larger n, which is similar to the fabricated SBDs by top-down approach.

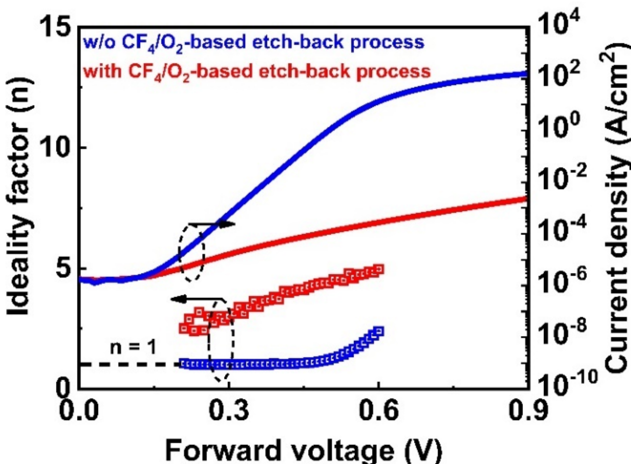



**Figure 3.7:** Right axis: forward *I-V* characteristics of the UTP SBD with etch-back process (red) and ideal UTR-SBD (blue) in semi-log scale. Left axis: extracted n of two UTR-SBDs.

Previous studies demonstrated that the etch rate of GaN in $CF_4$ or $O_2$ plasma is quite low [19,20], thus the negligible change of thickness in the drift layer after 1-min-plasma treatment is not considered as a main factor causing the deviation of current density and extracted n. It has been reported that the $O_2$ plasma treatment is effective to improve the Ohmic characteristics of n-GaN before contact deposition, because the oxygen (O) atom is generally regarded as a shallow donor in GaN [21,22]. On the contrary, the fluorine (F) ions induced by $CF_4$ plasma tend to be stabilized at interstitial sites in GaN and a single F ion at the interstitial site tends to capture a free electron and become a negative fixed charge, resulting in the depletion of electrons [23,24]. **Figure 3.8 (a) and (b)** show the changes in O and F concentrations before and after 1min etch-back process by secondary ion mass spectrometry (SIMS) measurements, respectively. Both O and F concentration are increased after plasma treatment, but the change in the F concentration is more significant because of large ratio of $CF_4$ in the process gas. Therefore, it is plausible that an insulating-like thin layer may be formed on the GaN surface [18,25]. By characteristics above, this thin layer is most likely attributed to the electron depletion by $F^-$ ions induced during the etch-back process. A portion of the forward biased voltage will drop across the insulating-like thin layer, increasing the extracted n and limiting the maximum current density.

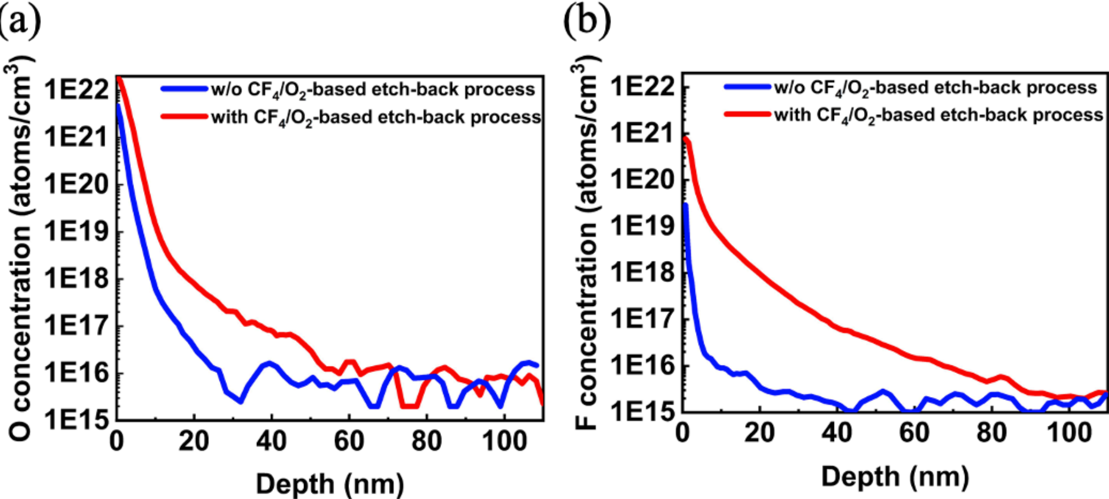



**Figure 3.8:** (a) O and (b) F concentration before (blue) and after (red) 1-min $CF_4/O_2$-based etch-back process near the top surface of GaN measured by SIMS.

### 3.4.2 Process optimization

In the previous section, the effect of the etch-back process on the GaN surface was studied by the characteristics of UTR-SBDs. Thus, the consideration on how to remove the adverse impact from the etch-back process during fabrication of NRSBD is highly required. It has been reported that the annealing process at a high temperature (> 600°C) will make part of F ions escape from GaN top surface [26]. However, such high temperature is not desired for the subsequent curing process of polyimide dielectric. Alternatively, it has been reported a low-bias-power $Cl_2$-based plasma etching in ICP-RIE system could obviously improve surface quality of damaged GaN layer [27]. And it is interesting to investigate

whether this method could be applied to remove the GaN layer affected by $CF_4/O_2$-based etch-back process. Thus, the aforementioned fabrication process flow could be optimized, as shown in **Fig. 3.9**.

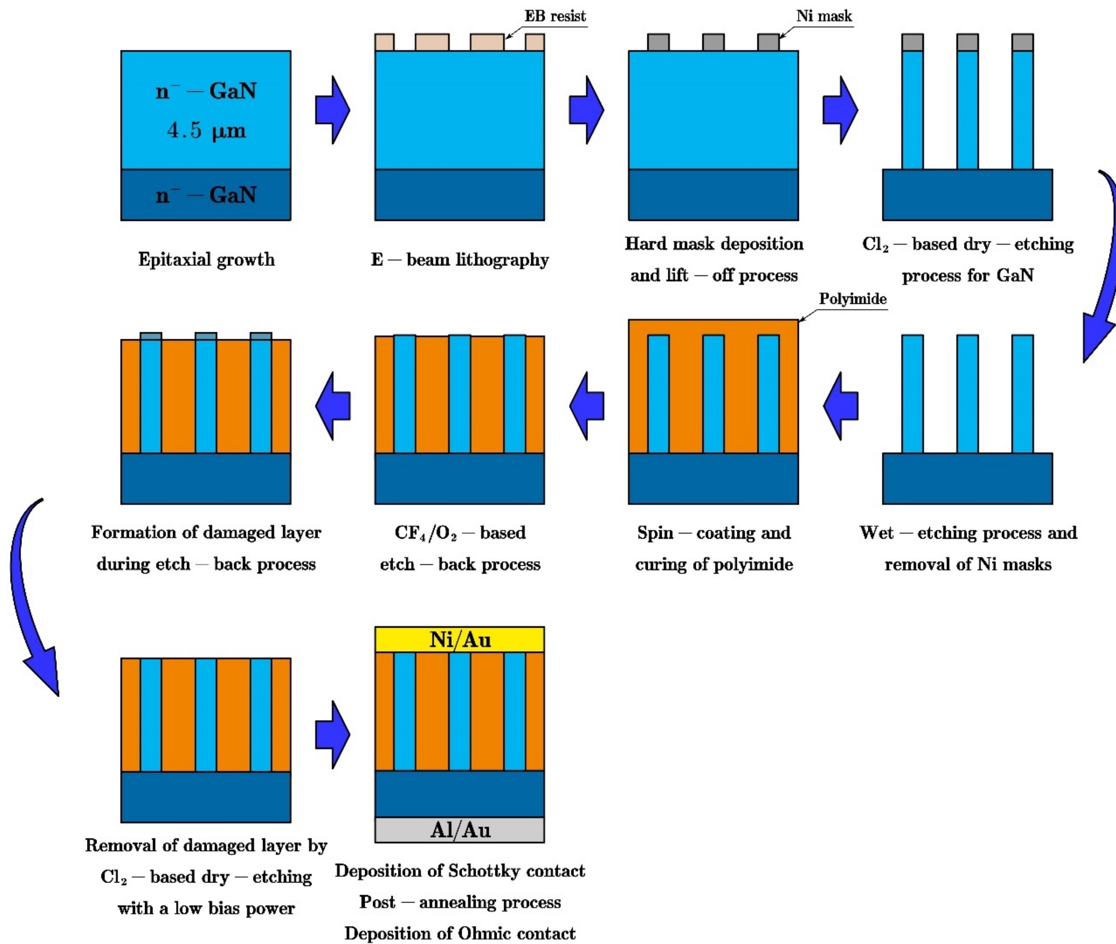



**Figure 3.9:** Optimized fabrication process of NRSBD through $Cl_2$-based dry-etching process with a low bias power.

A schematic illustration of the NRSBD fabricated using the optimized top-down technique is shown in **Fig. 3.10 (a)**. This time, the optimized fabrication was consistent with previous fabrication until completing the etch-back process. The fabrication was commenced with the design of circular patterns in square-array arrangement by E-beam lithography. Following that, a Ni film with a thickness of 150 nm was deposited in an E-beam evaporation system, and hard masks were formed after lift-off. Subsequently, a $Cl_2$ (30sccm)-based dry etching in an ICP-RIE system with an antenna power of 150W and a bias power of 30W was performed to form NWs with a height of 4.5-μm. **Figure 3.10 (b)** shows that the NWs with relatively smooth sidewall can be obtained by the wet etching process, in the 80°C alkali-based developer (AZ400K) for 30 min. After removing the hard mask, spin-on polyimide was coated and then cured at 350°C in $N_2$ ambient for 4 hours as the planarization step, as shown in **Fig. 3.10 (c)**. Afterwards, a $CF_4/O_2$ (30sccm/5sccm)-based etch-back procedure in an RIE system with an RF power of 150W was deployed to strip the redundant polyimide on top and open the top region of the NWs (**Fig. 3.10 (d)**). Most importantly, a $Cl_2$(30sccm)-based dry etch in an ICP-RIE system at a low bias power of 2.5W was performed to trim a 100-nm GaN layer from the top surface of NWs. After that, Ni/Au deposition and lift-off were carried out to form the top Schottky contact, which includes 100 GaN pillars with a diameter of 800 nm (simplified as 800-nm-NWSBD) as shown in **Fig. 3.10 (e)**, and a rapid thermal annealing (RTA) was followed at 400°C for 3 min. Finally, Al/Au was deposited by Sputtering on the backside of GaN substrate to form the Ohmic contact to the diode's cathode.

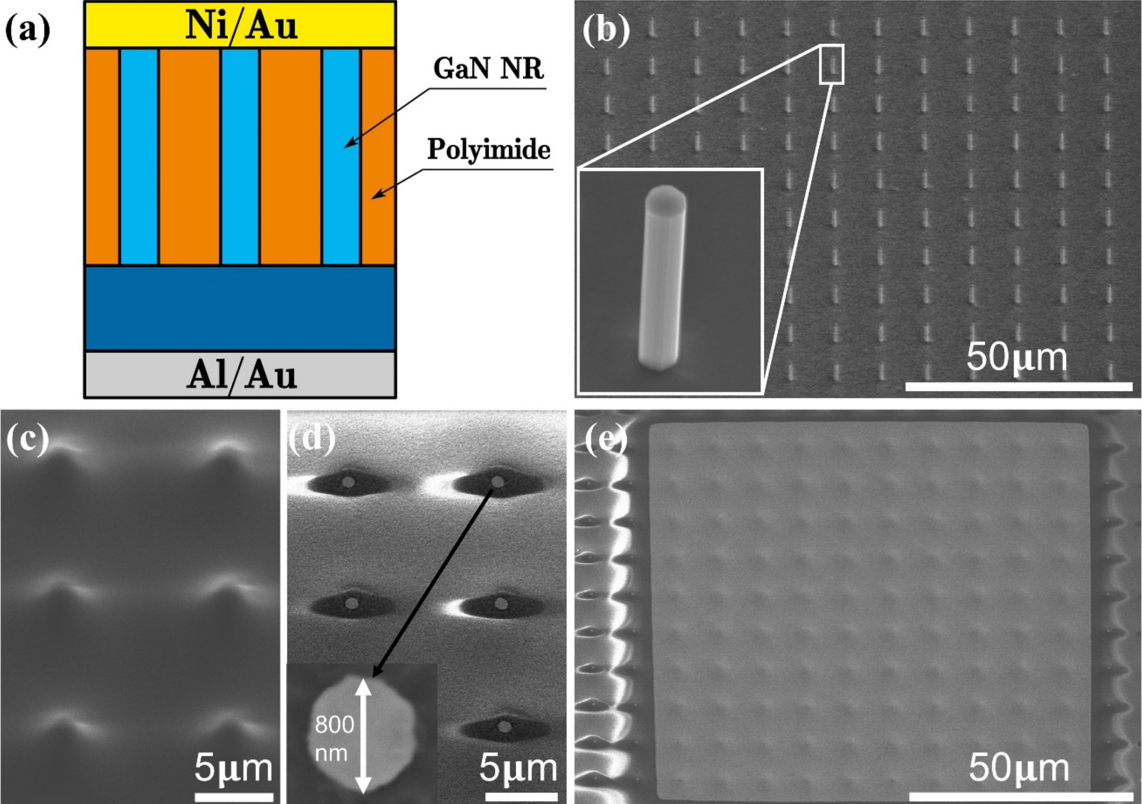



**Figure. 3.10:** (a) Schematic illustration of the NRSBD. (b) Tilted SEM image of NW array after hot developer-based wet etching process. Inset: enlarged image of single NR. (c) Tilted SEM image of NRs coated by cured polyimide. (d) Tilted SEM image of the exposure of NRs. Inset: No tilted SEM image of single NR (800 nm in diameter). (e) Tilted SEM image of one anode electrode including 100 NRs.

### 3.4.3 Experimental results after optimized fabrication

The current density and differential $R_{ON}$ are also normalized by the effective Schottky contact area (the area of top surface of 100 NWs), which is approximately equal to $5.03 \times 10^{-7}$ cm$^2$. **Figure 3.11 (a)** plots the representative forward *I-V* characteristics of the previously non-optimized 800-nm-NRSBD and the new 800-nm-NRSBD with optimization, both of which exhibit a high forward current density over 10 kA/cm$^2$ and a low differential $R_{ON}$ of ~ 0.16 mΩ·cm$^2$ around 3 V. However, as shown in **Fig. 3.11 (b)**, an increased n and a high $V_{ON}$ (@100 A/cm2) of 1.4 V were extracted from the previous 800-nm-NRSBD without optimization, as a result of the existence of the insulating-like thin layer by etch-back process.

On the contrary, around 100-nm GaN layer including the thin layer damaged by etch-back process on the top surface of NWs was removed in the ICP-RIE system with a bias power of 2.5 W for chlorine plasma, in which the extremely low bias power is to avoid inducing more plasma damages. As-optimized 800-nm-NRSBD delivers a recovered n (1.04 ~ 1.09) and a reduced $V_{ON}$ of ~ 0.80 V. The near-unity n verifies that the mechanism of carrier transportation through Ni/n$^-$-GaN Schottky interface of the optimized 800-nm-NRSBD is determined by thermionic emission model, indicating additional $Cl_2$-based dry etch with low bias power and post-Schottky RTA processes could recover the adverse effect caused by $CF_4/O_2$ based etch-back process. Compared with the high voltage GaN-on-GaN SBDs without inserting an AlGaN tunneling barrier layer, the measured $V_{ON}$ is a relatively lower value, due to the relatively high net doping concentration in the drift region.

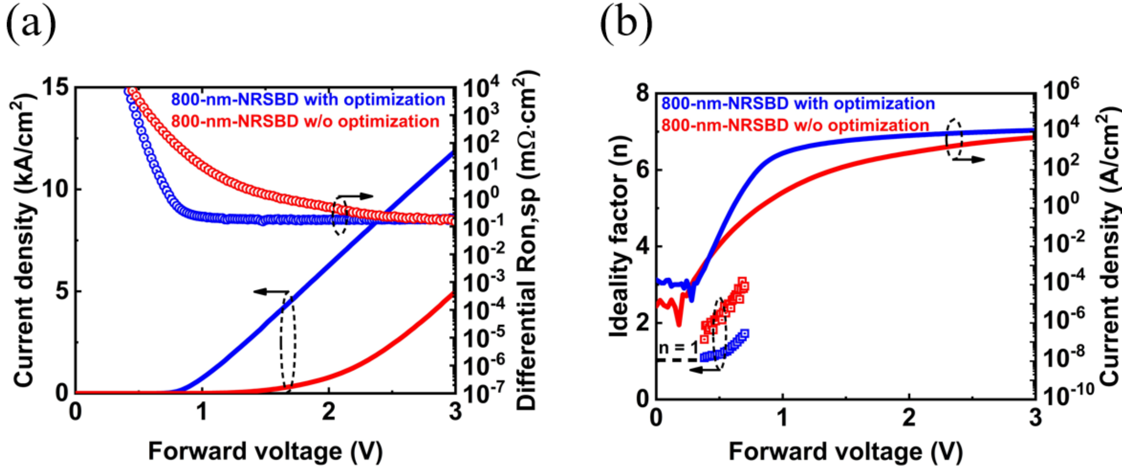



**Figure. 3.11:** Forward *I-V* characteristics in (a) linear scale and (b) semi-log scale of 800-nm-NWSBD with (blue) and without (red) optimized processes.

Furthermore, **Fig. 3.12** plots the representative reverse *I-V* characteristics of the well-optimized 800-nm-NRSBD and the UTR-SBD without plasma treatment, the 800-nm-NRSBD could still deliver a greatly suppressed leakage current and a higher soft *BV* (at a current density of 0.05 A/cm$^2$) of ~ 480V in comparison with the UTR-SBD with a soft *BV* of ~ 65V.

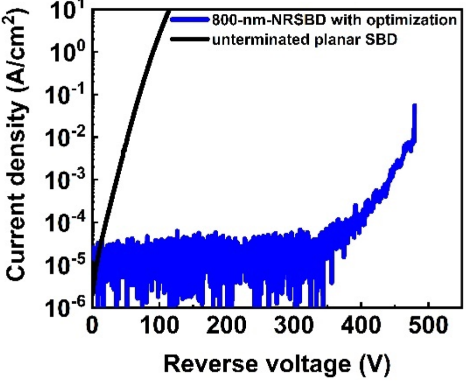



**Figure. 3.12:** Representative *I-V* characteristics of ideal UTR-SBD (black) and the 800-nm-NRSBD with optimization (blue) as a function of reverse bias.

**Figure 3.13** shows the benchmark of net doping concentration versus *BV* for some reported GaN-on-GaN diodes [28-35], in which different kinds of edge terminations have been employed, especially, including PNDs with good avalanche capability [28, 29]. Apparently, the measured soft *BV*s of the SBDs are lower in comparison with the avalanche *BV*s of the PNDs featuring a similar value of net doping concentration in the drift region. But it is remarkable that the enhanced soft *BV* for 800-nm-NRSBD presented in this work, mainly by virtue to dielectric RESURF effect, can be comparable with the avalanche BV for the PND with a net doping concentration around $4.5 \times 10^{16}/cm^3$.

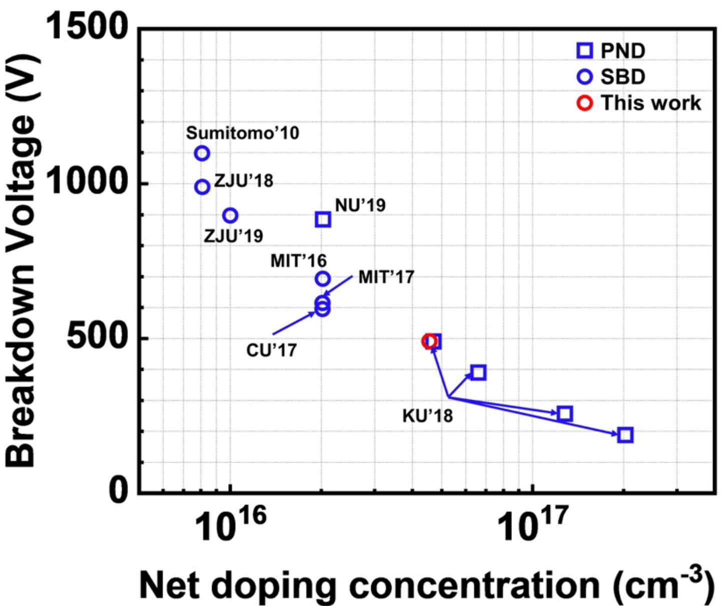



**Figure. 3.13:** Benchmark of net doping concentration v.s. *BV* for vertical GaN-on-GaN diodes.

## 3.5 Summary

In this chapter, by TCAD simulations, the author investigated that the dielectric RESURF effect is present on vertical GaN NW/NR-based SBDs, resulting in suppressed leakage current and enhanced $BV$. As the first step, 800-nm-NRSBD and 10-µm-mesa SBD were fabricated by utilizing top-down approach, and the improved device performance for the 800-nm-NRSBD was congruous with the simulation result, providing the proof of the dielectric RESURF effect on NRSBD. However, owing to adverse effect from $CF_4/O_2$-based etch-back process, the fabricated SBDs deliver a non-ideal ideality factor and a higher $V_{ON}$. To solve this problem, the additional processes based on the low-bias-power $Cl_2$-based etching and post-metallization RTA were performed. It is confirmed the 800-nm-NRSBD fabricated by new process flow features several recovered device performances, including a low $V_{ON}$ of ~ 0.80 V and a near-unity n (typically 1.04 ~ 1.09) was added, and still along with a soft $BV$ of ~480 V, showing the considerable potential for nanostructure-based power electronics.

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# Chapter 4 Improved Device Performance of Vertical GaN-on-GaN NRSBDs with Etching Optimizations

**4.1** Introduction

**4.2** Optimization of dry-etching process

**4.3** Optimization of wet-etching process

**4.4** Fabrication of the NRSBDs with optimized process flow

**4.5** Characteristics of the NRSBDs with optimizations

**4.6** Summary

References

## 4.1 Introduction

The profile and surface morphology of the nanostructures fabricated by top-down approach are strongly influenced by dry- and wet-etching processes, so it is significant to optimize the experimental conditions of the etching processes.

As discussed in the Chapter 3, the $CF_4/O_2$-based etch-back process negatively impacts the forward performance of GaN SBDs. Moreover, from the perspective of top-down approach, an effective optimization was proposed, inducing the additional low-damage dry etching process and subsequent rapid thermal annealing. And it was confirmed the new 800-nm-NRSBD with the optimization could exhibit a recovered device performance. However, the secondary $Cl_2$-based dry-etching process, even with an extremely low bias power, may increase more plasma damages as well as fabrication difficulty [1,2]. Consequently, it would be desirable if a more reasonable top-down method could be proposed for the fabrication of NW/NRSBDs.

In this chapter, it will be discussed how to obtain the NR with a well-shaped profile. Additionally, a more rational top-down approach was employed to fabricate NRSBD. As-fabricated NRSBD could achieve improved device performance such as a low $V_{ON}$, high $BV$, along with not severe current collapse.

## 4.2 Optimization of Dry-etching Process

There has been a significant development in dry etching of GaN by ICP-RIE system over the past decades. Especially, $Cl_2$-based plasma, generated by ICP, has been extensively investigated to etch GaN [3-7]. For GaN nanostructure fabricated by top-down approach, Paramanik et al. reported comprehensive studies on how each parameter (antenna power, bias power, chamber pressure, substrate temperature, gas chemistry and flow rate) in ICP-RIE system individually affected etch rate and morphology of nanopillars [8].

Towards to the vertical GaN nano/submicrostructure-based power devices, the requirements of dry-etching process are mainly focused on etch depth, sidewall roughness, and structure morphology. In a similar way, the NW/NR structure with a high aspect ratio, smooth sidewall without roughness, a good perpendicularity is highly desired. In this chapter, the primary target of optimization about dry-etching process is to fabricate the NRs with the aforementioned characteristics.

Except for the parameters mentioned above, the selection of hard mask material is quite important for optimization of dry-etching process. The hard mask material with a high selectivity could enable a deep etch for GaN. Furthermore, as shown in **Fig. 4.1**, the mask erosion during plasma etching is a major reason causing the formation of tapered NR [8]. Consequently, compared with $SiO_2$ or photoresist, the Ni was usually selected as the mask material for GaN NR fabricated by top-down approach. However, the surface roughness on the sidewall (typically represented as striations) was observed by using Ni mask [9-11], typically induced by unsmooth edge of hard mask after lift-off.

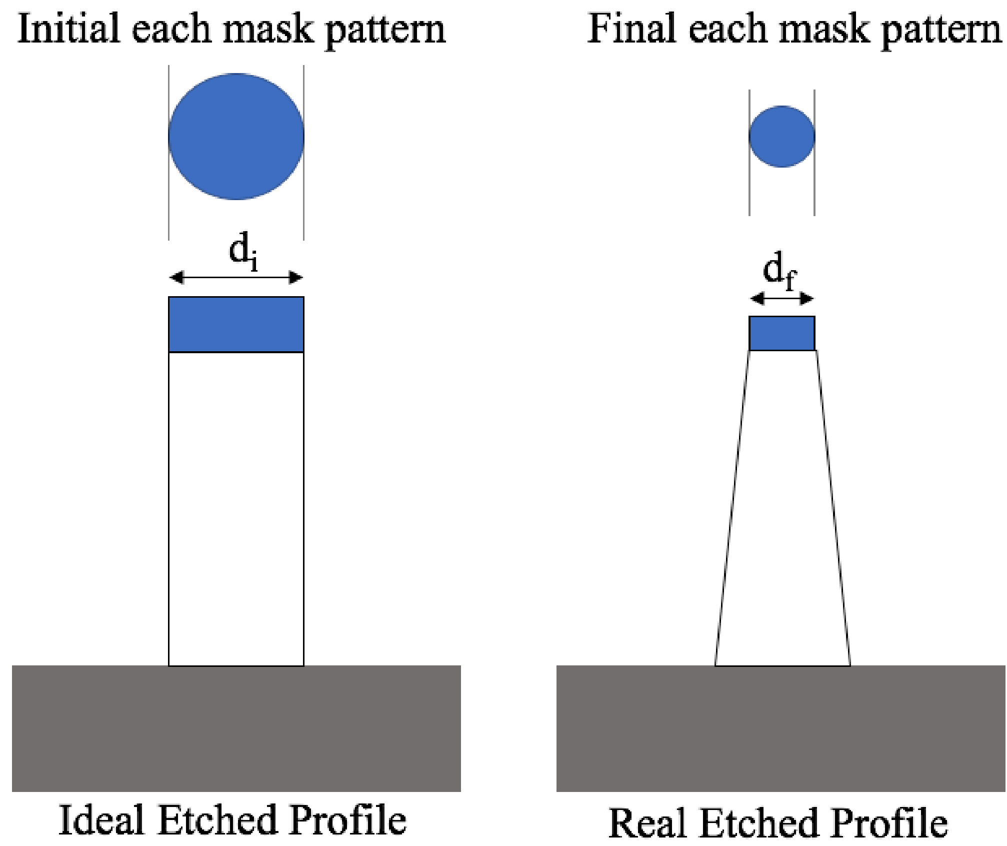



**Figure 4.1:** Schematic of ideal and real dry-etching process in ICP-RIE system.

Accordingly, the first optimization of dry-etching process is to deposit one film layer of $SiO_2$ (by PECVD) before E-beam lithography. After dry etch, the structure with Ni/$SiO_2$/GaN three-layers near the top region of NR will be observed, as illustrated in **Fig. 4.2**. Another importance of this inserted dielectric layer will be discussed in the latter section. The second optimization is to reduce the hard mask erosion by properly increasing the thickness of metal hard mask (250-nm-Ni) and reducing the RF power (20 W) in ICP-RIE system. Based on what discussed above, the vertical NRs with a high aspect ratio and smooth sidewall were obtained, as shown in **Fig. 4.2**.

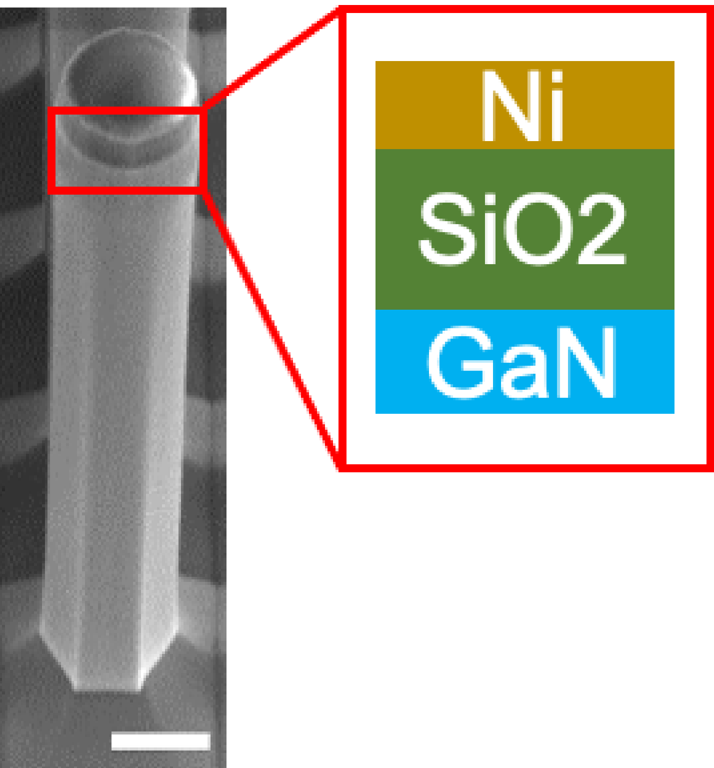



**Figure 4.2:** Bird-viewed SEM image of the optimized NR after dry etch, the length bar is 1 μm.

## 4.3 Optimization of Wet-etching Process

For most etchants, it is difficult to wet etch GaN due to its superior chemical stability. However, lots of research indicated that GaN could be wet etched in hot alkaline-based solution over the past couple of decades, the reaction between the GaN and $OH^-$ ion can be explained by the following equation [12]:

$$2GaN + 3H_2O \xrightarrow{OH^-} Ga_2O_3 + 2NH_3$$

Here, there are two functions of $OH^-$, one function is serving as a catalyst for reaction, and the other is dissolving the product of reaction which is correspond with $Ga_2O_3$ [13, 14]. Furthermore, for a given etchant, temperature and solution concentration are commonly regarded as the most influential parameters to determine the etch rate, especially, the high temperature could largely promote the wet-etching process. Furthermore, it was reported that the etch rate was tightly related to crystallographic plane of GaN [12]. Lai et al. proposed that the different wet etch rate of etch GaN facets could be explained by etching barrier index (EBI), which is equal to the product between number of N-dangling bonds N atom and planar density [15], as shown in Table 4. 1. A small value of EBI represents that facet is easier to be wet-etched.

| Orientation of planes | (0001) | $(11\bar{2}0)$ | $(1\bar{1}00)$ | (0001) | $(10\bar{1}\bar{1})$ | $(10\bar{1}2)$ |
|---|---|---|---|---|---|---|
| | **+c-plane** | **a-plane** | **m-plane** | **−c-plane** | | **r-plane** |
| Planar density (number of atoms/Å$^2$) | 0.1138 | 0.1398 | 0.1211 | 0.1138 | 0.0534 | 0.0414 |
| Number of dangling bonds on N atom | 3 | 2 | 1, 2 | 1 | 2 | 2 |
| EBI | 0.3414 | 0.2796 | 0.1211, 0.2422 | 0.1138 | 0.1068 | 0.0828 |

**Table 4.1:** Etching capability of etch crystallographic plane on GaN [15].

Most importantly, recent reports have shown that the hot alkali-based wet-etching process has assisted in reforming the geometry of GaN structures and resulting in an improved device performance [16,17]. However, despite the high surface-to-volume ratio is one of the most distinct features of the submicro/nanostructure, research into the impacts of the wet-etching process is rarely reported for the vertical nanoscale GaN power devices. Generally, the alkaline development-based (2.38% TMAH/AZ400K) wet-etching process at a high temperature over 80 ℃ was used to shrink the size and reshape the non-polar sidewall morphology of NW/NR [18], as well as the previous results in the Chapter 3.

Thanks to the optimizations in our ICP-RIE system, the GaN NRs with hexagonal shape and good perpendicularity directly comes from the deep dry-etching process, as shown the last section, so the TMAH-based wet-etching process is proceeded at a relatively low temperature of 50 ℃ for 10 min. The aim of this optimization is to solely reduce the interface state density on the sidewall of NW/NR, but not to change the size.

## 4.4 Fabrication of NRSBDs with optimized process flow

On the basis of optimizations about etching process in the previous sections, a more rational top-down approach was employed to fabricate NRSBDs.

### 4.4.1 Sample preparation

This time, an 8-µm-thick lightly Si-doped GaN epilayer was grown on a GaN freestanding substrate ([Si]: $2 \times 10^{18}/cm^3$) by MOCVD. Just like what the discussion in Chapter 3, **Figure 4.3 (a)** depicts the schematic structure of an UTR-SBD, the net doping concentration ($N_D$-$N_A$) in the $n^-$-GaN drift layer by this structure is confirmed to be around ~ $5.5 \times 10^{16}/cm^3$ as shown in the **Fig. 4.3 (c)**, according to the *C*-*V* characteristics of the UTR-SBD at a frequency of 1 MHz (**Fig. 4.3 (b)**).

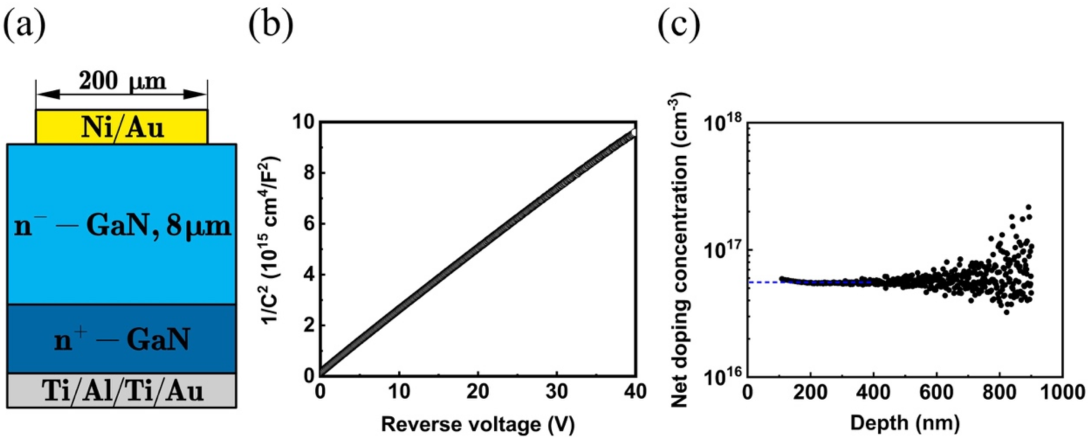
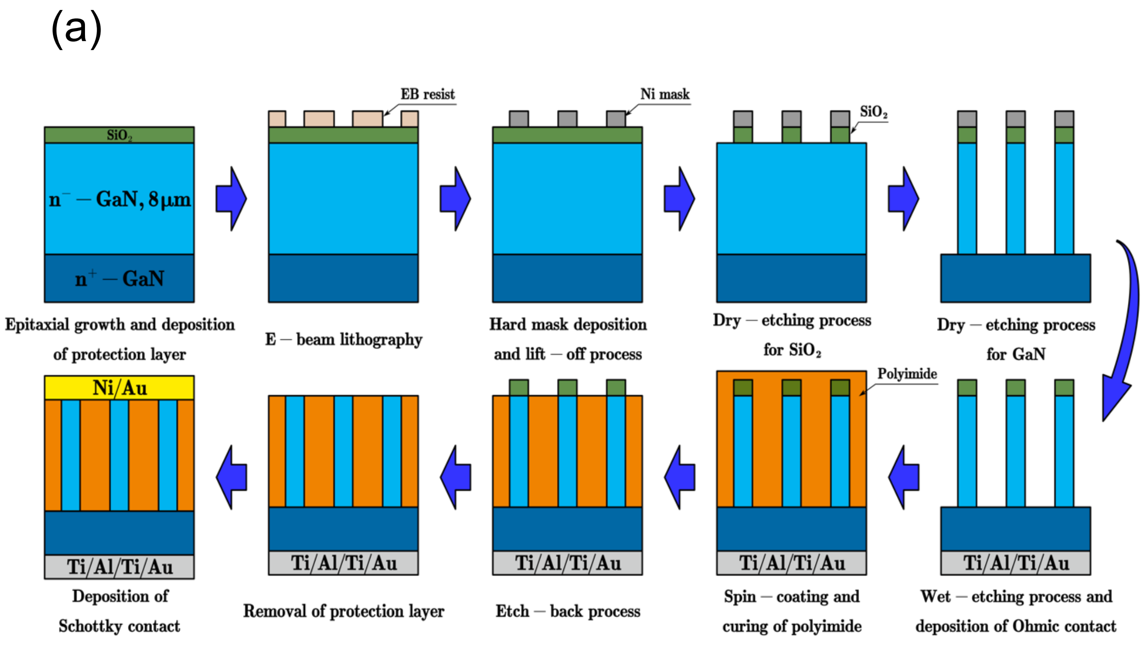



**Figure 4.3:** (a) The schematic structure of an UTR-SBD for *C*-*V* characteristics. (b) $1/C^2$ versus reverse voltage plot of the UTR-SBD. (c) The extracted plot of net doping concentration versus depletion depth for the UTR-SBD.

### 4.4.2 Detailed top-down approach with optimizations

**Figure 4. 4 (a)** delineates the optimized fabrication process of NRSBD through a two-step etching-based top-down approach. At first, a 300-nm-thick $SiO_2$ layer was deposited using a plasma-enhanced chemical vapor deposition (PECVD) system to serve as a PL layer. The sample was then patterned by E-beam lithography and a 250-nm-thick Ni film was deposited via E-beam evaporation as etch-mask. Following the metal lift-off, circular Ni masks (diameter: 1.3-μm) in square arrays with a pitch size of 10-μm were obtained. Furthermore, $CF_4$-based RIE and $Cl_2$-based ICP-RIE systems were carried out successively, the $SiO_2$ and GaN uncovered by Ni masks were totally etched away and the NR arrays with a height of 8-μm were formed. After removing the metal masks, the NR arrays were treated with a wet-etching process, in the 50°C 2.38%-TMAH solution for 10 min. Next, a Ti/Al/Ti/Au (20 nm/100 nm/20 nm/150 nm) metal stack was deposited on the backside of substrate and subsequently annealed at 650 °C for 5 min to form the Ohmic contact to $n^+$ type GaN. To fill in the gaps among NRs and to achieve planarization, polyimide (Toray, SP-341) was spun onto the samples and hard baked at 350 °C in $N_2$ ambient for 4 h. Afterwards, the polyimide on the top was etched in the RIE system using $CF_4/O_2$ (20 sccm/10 sccm flow rate)-based plasma with an RF power of 150 W until the $SiO_2$ PL was just exposed. Following that, the exposed PL layer was peeled in a diluted 10%-hydrogen fluoride solution. Finally, Ni/Au deposition and lift-off were performed to create the top Schottky contact, exactly covering 100 NRs. **Figure 4. 4 (b)** shows the SEM images before and after the removal of PL.

(a)




(b)

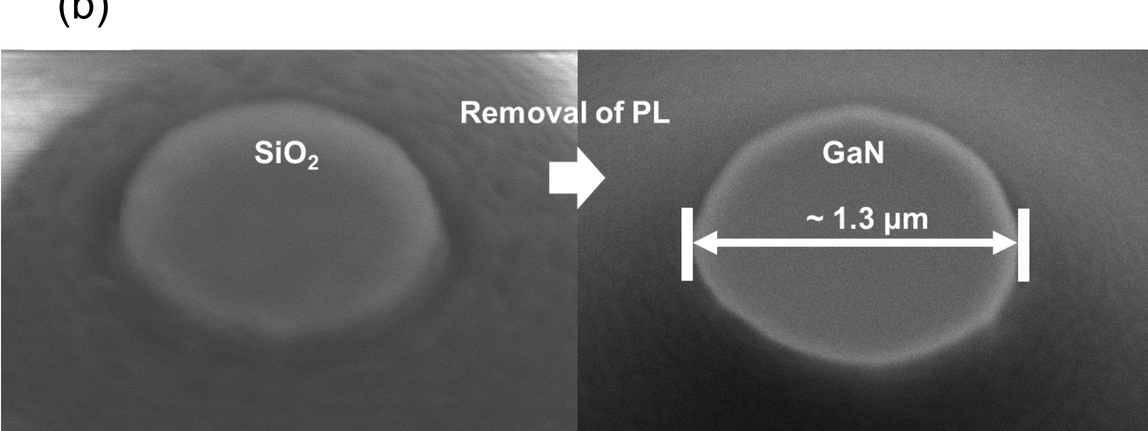



**Figure 4.4 (a):** Fabrication process of NRSBDs through an optimized top-down approach. **(b)**: Bird-viewed SEM images of removal of PL.

## 4.5 Characteristics of the NRSBDs with optimizations

### 4.5.1 Forward *I-V* characteristics of fabricated NRSBDs

To study the impact of the wet-etching process on the device performance of NRSBDs, the NRSBDs with the same diameter and pitch size was simultaneously fabricated except that the TMAH-based wet-etch process before filling polyimide is absent. As-discussed optimizations in the previous sections, by a well-optimized pure $Cl_2$-based (30 sccm in flow rate) dry-etching process with a bias power of 20 W, the as-etched NR features a good perpendicularity and distinct smooth non-polar a-plane sidewalls, as shown in **Fig. 4.5 (a)**.

Furthermore, a relatively moderate TMAH-based wet-etching process at a low temperature of 50 ℃ and a low concentration of 2.38 % was deployed only to restore smoothness of the sidewall surface after the plasma dry-etching process. It was reported the wet-etching rate with a similar TMAH solution is less than 1 nm/min [19, 20]. Such inconspicuous etching rate is confirmed by SEM images of the GaN NR from **Fig. 4.5 (a)** and **(b)**, where obvious morphology changes and size shrinking of NR were not observed after 10 min wet-etching process and thus were not taken into account in the subsequent analyses. Instead, this wet-etching process may play a dominant role in sharply reducing the surface state at the sidewall of NRs.

**Figure 4.5 (c)** plots the forward *I-V* characteristics in a semi-log scale of two NRSBDs at room temperature, the current density was herein calculated by effective Schottky area (top area of 100 NRs), which was calculated to be $1.33\times10^{-6}$ $cm^2$. Both of NRSBDs exhibit a high forward current density over 10 $kA/cm^2$ at 4 V and a low leakage current density ~ $10^{-9}$ $kA/cm^2$ at −2 V, resulting a high ON/OFF ratio over $10^{10}$. Furthermore, the mechanism of forward conduction of SBD is generally determined by thermionic emission (TE) model, represented as

$$J = J_s[\exp(qV/nkT) - 1], \quad (4.1)$$

$$\phi_b = \frac{kT}{q}\ln\left(\frac{A^*T^2}{J_s}\right), \quad (4.2)$$

where $J$ is the current density, $J_s$ is the saturate current density, $q$ is the electron charge, $\phi_b$ is the Schottky barrier height, $A^*$ is the Richardson constant, and $T$ is the absolute temperature. According to equation (4.1), the ideality factors ($n$) of NRSBDs with and without the wet-etching process were extracted to be 1.03 and 1.04, respectively. These near-unity values verify the inserted PL could effectively prevent the top surface of GaN NR array from plasma damage, which is induced by $CF_4/O_2$-based etch-back process. Furthermore, according to equation (4.2), by assuming the theoretical value of Richardson constant of GaN is 26.64 $A\cdot cm^{-2}\cdot K^{-2}$ [21], the SBHs of NRSBDs with and without the wet-etching process were evaluated to be 0.86 eV and 0.83 eV, respectively.

**Figure 4.5 (d)** plots the forward *I-V* characteristics in the linear scale. The NRSBDs with/without the wet-etching treatment deliver the almost same $V_{ON}$ (defined at a current density level of 100 A/cm$^2$) of 0.65 V, and the specific differential on-resistance ($R_{on,sp}$) of 0.23/0.30 mΩ·cm$^2$, respectively. The low $V_{ON}$ in NRSBDs could be ascribed to a relatively high doping level in drift region. The deviation of current density after turning-on SBDs could be caused by different surface state density at the sidewall of two NRSBDs. It has been reported that surface states at the sidewall could capture electrons inside n-type GaN NR bulk, forming a depleted space charge region [22]. And the increased surface state in GaN induced by dry-etching process has been also studied [23]. Moreover, it is demonstrated that the GaN surface after TMAH-based wet-etching process could deliver a relative low interface state density (~ $1 \times 10^{11}$ cm$^{-2}$·eV$^{-1}$) in both non-polar GaN MOS interfaces formed on trench sidewalls and vertical GaN wrap-around gated nanowire MOSFET with non-polar a-plane sidewall [24, 25]. As a result, the effective area of conduction channel in the NRSBD without the wet-etching process is reduced, represented as a higher $R_{on,sp}$, as illustrated in **Fig. 4.5 (e)**.

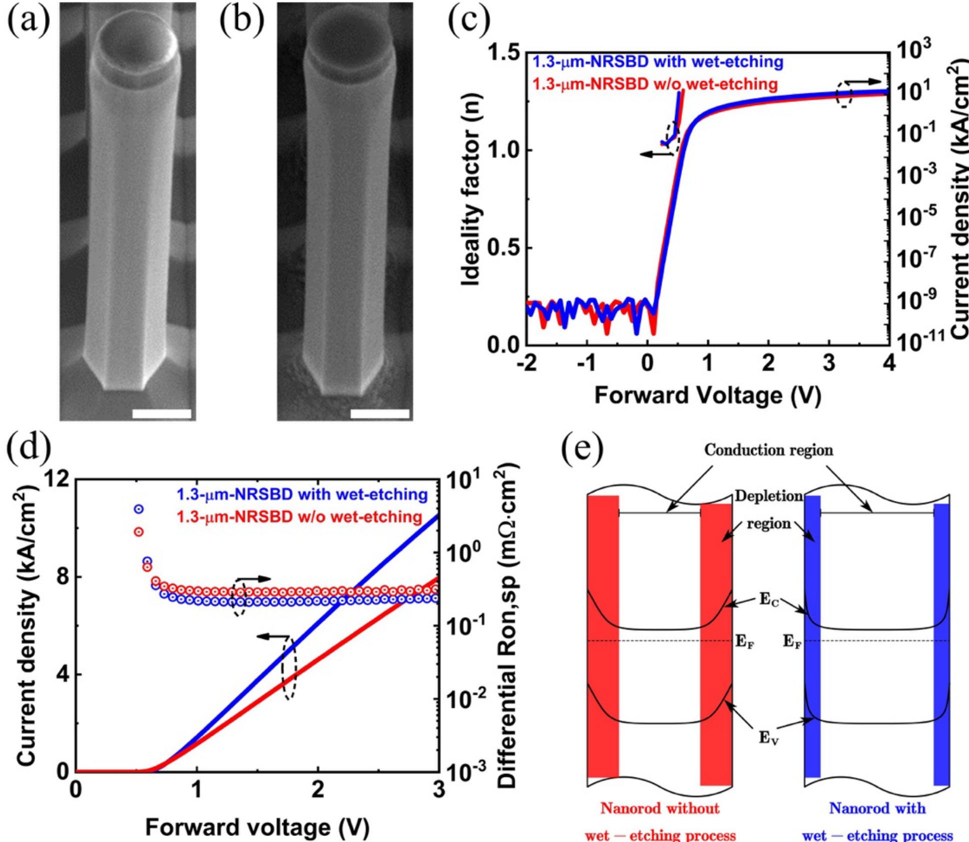



**Figure 4.5:** a single NR with a diameter of 1.3-µm after (a) dry-etching process and (b) wet-etching process. The scale bar is 1-µm. Forward *I-V* characteristics in the (c) semi-log scale and (d) linear scale of the 1.3-µm-NRSBD with (blue) and without (red) wet-etching process. (e) Schematic model of conduction and depletion regions inside NR with/without the wet-etching process.

### 4.5.2 Evaluation of Schottky barrier height for NRSBDs

To further investigate the property of Schottky interface of optimized NRSBD, an accurate extraction of SBH is necessary. Generally, compared with aforementioned calculation from *I-V* characteristics at a certain temperature, a Richardson plot approach based on temperature-dependent *I-V (I-V-T)* characteristics is commonly used for SBH extraction by eliminating the possibility of inaccuracy owing to the uncertainty of $A*$. **Figure 4.6 (a)** plots the *I-V-T* characteristics of the NRSBD with wet-etching process, the Richardson plot of the NRSBD can be carried out by following the

$$ln\left(\frac{J_s}{T^2}\right) = -\frac{q\phi_b}{kT} + ln(A^*) \quad (4.3)$$

The SBH and $A*$ are determined to be 0.75 eV and 0.26 $A{\cdot}cm^{-2}{\cdot}K^{-2}$, based on of the slope and intercept of linear fitting curves in **Fig 4.6 (b)**. However, a significant deviation from the theoretical value of $A*$ is obtained. Moreover, if the SBH and the *n* value at each temperature are separately extracted by the aforementioned single *I-V* approach, it is found the SBH is increased while the *n* value is decreased with elevated temperatures, as shown in **Fig 4.6 (c)**. This temperature-dependent *n*/SBH and inconsistence of $A*$ have been also reported in other practical SBDs and are expected to be attributed to the spatial inhomogeneities of Schottky contact [26, 27]. Werner and Güttler proposed a model considering Schottky barrier inhomogeneity by assuming the Gaussian distribution of

potential fluctuations/SBH under Schottky contact [28]. And the temperature-dependent apparent SBH ($\phi_{b,app}$) is concluded to associate with a mean SBH and a standard inhomogeneity, as described in

$$\phi_{b,app} = \overline{\phi_b}\,(T = 0K) - \frac{q\sigma_0^2}{2kT} \quad (4.4)$$

With this consideration, a modified Richardson plot method could be derived as

$$ln\left(\frac{J_0}{T^2}\right) - \frac{q^2\sigma_0^2}{2k^2T^2} = ln\,(A^{**}) - \frac{q\overline{\phi_b}}{kT} \quad (4.5)$$

by substituting equation (4.4) into equation (4.2). As shown in **Fig 4.6 (d)**, a mean SBH of 1.04 eV with a standard deviation of 0.095 V of the NRSBD can be obtained, according to equation (4.4). In particular, the $A^{**}$ of 26.86 A·cm$^{-2}$·K$^{-2}$ was extracted by the modified Richardson plot of the NRSBD in **Fig 4.6 (e)**, which is very close to the theoretical value, indicating this method is a reasonable characterization for NRSBDs.

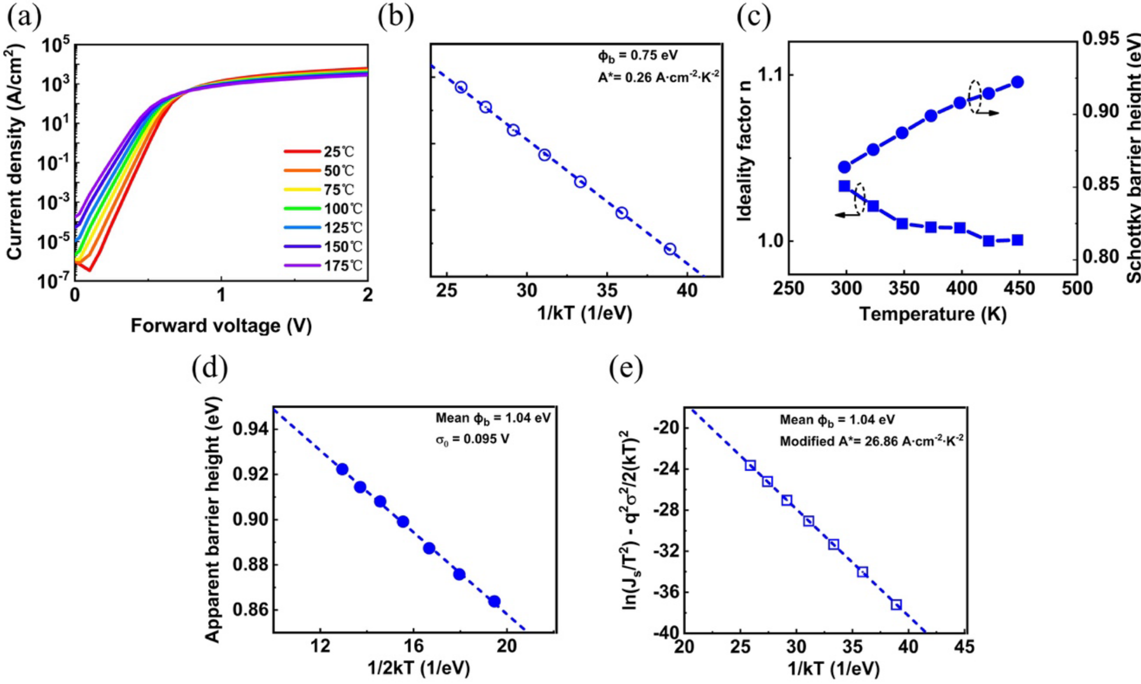



**Figure 4.6:** (a) Forward *I-V-T* characteristics of the NRSBD with wet-etching process. (b) Normal Richardson plot of the NRSBD with wet-etching process. (c) Extracted SBH and n at the elevated temperature. (d) Extracted apparent SBH versus *1/2kT*, where *k* is the plank constant and *T* is the absolute temperature. (e) Modified Richardson plot of the NRSBD with the wet-etching process.

### 4.5.3 Pulse *I-V* characteristics of the fabricated NRSBDs

The dynamic performance of NRSBDs is evaluated by pulse *I-V* measurements. The anode voltage switches from a reverse quiescent bias (0, −10, −20, −30, −40, −50, −100, −150, −200, −250, −300, and down to −350 V) to a forward voltage of 3 V with a pulse width of 3 ms and a pulse period of 5 ms. As shown in **Fig. 4.7 (a)**, an apparent current collapse for the NRSBD without the wet-etching process can be obtained with the elevated quiescent voltage, an on-resistance ($R_{on}$) degradation of 60.13% can be extracted at a stress voltage of −350 V. It is plausible that the electrons ejected from anode could be trapped by surface states on the sidewall at a certain stress voltage, whereas the surface states with deep energy level are unable to release the trapped electrons instantly when the NRSBD is forward-biased, resulting in an obvious current collapse. On the other hand, as shown in **Fig. 4.7 (b)**, unlike the NRSBD without the wet-etching process where sidewall trapping could easily degrade the $R_{on}$, the NRSBD with the wet-etching optimization shows no apparent degradation of $R_{on}$, proving the wet-etching process is an effective optimization method for improving the dynamic performance of NRSBD.

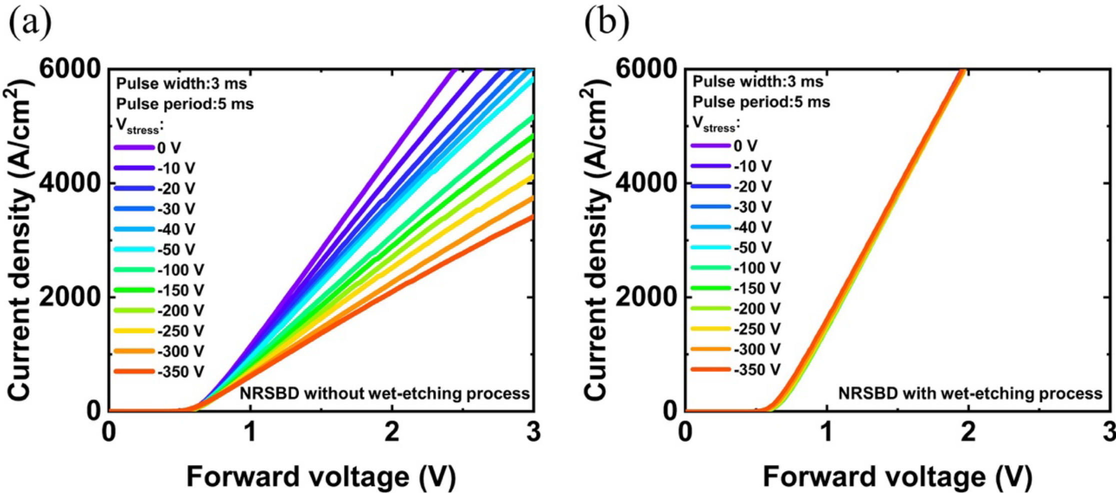



**Figure 4.7:** Pulse *I-V* characteristics of the NRSBD without (a) and with (b) the wet-etching process.

### 4.5.4 Reverse *I-V* characteristics of the fabricated NRSBDs

To study the impact of the wet-etching process on the device performance of NRSBD, another NRSBD with the same diameter and pitch size was simultaneously fabricated **Figure 4.8 (a)** shows the reverse leakage current density of two NRSBDs and UTR-SBD with same epi-structure. Compared with UTR-SBD, the two kinds of NRSBDs deliver a significantly suppressed leakage current and improved *BV* (at a current density of 0.05 A/cm$^2$) by taking advantage of the dielectric RESURF effect. Compared with the *BV* of 707 V in the NRSBD without wet-etching process, the mechanisms of further improved *BV* of 772 V in the NRSBD with wet-etching optimization might be attributed to mitigated

trap-assisted tunneling, space charged limited current, and others [29-31], which will be further investigated in the future work. Intriguingly, there is a tradeoff between SBH-related $V_{ON}$ and reverse leakage current. **Figure 4.8(b)** shows the benchmark of $BV$ versus $V_{ON}$ for previously reported vertical GaN SBDs [31-38], and the fabricated NRSBDs. The fabricated NRSBDs show the potential to achieve a low $V_{ON}$ and a high $BV$ at the same time.

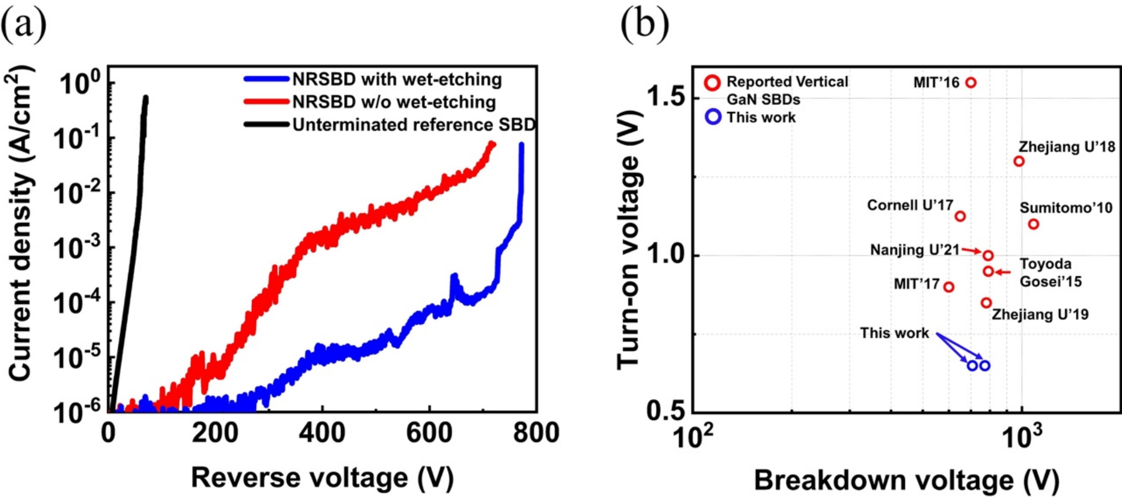



**Figure 4.8:** (a) Reverse *I-V* characteristics of ideal UTR-SBD (black) and the NRSBD without (red) and with (blue) wet-etching process. (b) Benchmark of $V_{ON}$ v.s. $BV$ for previously reported vertical GaN-on-GaN SBDs and the fabricated GaN NRSBDs.

## 4.6 Summary

In conclusion, we proposed an optimized etching-based top-down approach for fabricating GaN NRSBDs by adding a PL prior to etching-back process. In addition, the impact of wet-etching process during the fabrication on device performance was investigated. It has been verified that the wet-etching process could modify surface condition of GaN NR sidewall, leading to an improvement of device performance of NRSBD. The fabricated NRSBD with wet-etching process enabled a low $V_{ON}$ and a high $BV$ simultaneously with negligible current collapse, showing the huge potential of RESURF-reinforced GaN power device.

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# Chapter 5 Conclusions

**5.1** Summary

**5.2** Contributions

**5.3** Future perspectives

## 5.1 Summary

Firstly, we studied GaN NRSBDs with suppressed leakage current and enhanced $BV$ compared with large-diameter SBD using a top-down fabrication, providing the evidence of the dielectric RESURF effect on vertical GaN NR structures. However, relatively large ideality factor (n) and a high $V_{ON}$ were presented in these devices, which are likely caused by an $CF_4/O_2$-based etch-back process before the top Schottky contacts of NWSBD were formed.

Furthermore, effect of the etch-back process on the GaN surface was studied by the characteristics of UTR-SBDs. To obtain a better quality in the Schottky contacts to the top of the NRs, a low-bias-power $Cl_2$-based plasma etching is applied to the top area after $CF_4/O_2$-based etch-back process, followed by post-metallization rapid thermal annealing. It is confirmed the NWSBDs with aforementioned optimized processes could deliver a recovered forward performance.

In spite of the ultra-low bias power employed, the additional $Cl_2$-based dry-etching process increases fabrication complexity and may induce extra plasma damage. Thus, we further adopted a more reliable and feasible top-down fabrication process for NRSBD by adding one $SiO_2$ layer as a protection layer (PL) to mitigate plasma damage from the etch-back process. It is confirmed that a high-quality Schottky contact could be formed by this inserted PL. Moreover, wet-etching process, as a crucial step during the fabrication, the effect of this process on NRSBD was investigated in detail using both static and dynamic current-voltage ($I$-$V$) characteristics. The result indicates that the wet-etching process plays an important role in achieving improved device performance

## 5.2 Contributions

- The author proposes an etching-based top-down approach to fabricate GaN NRSBDs.
- Successfully demonstrate GaN NR/NW structure can benefit from the dielectric RESURF effect.
- Investigation on adverse effect from $CF_4/O_2$-based etch-back process
- Effective optimized top-down approach, which is based on low-damage etch with a fairly low bias voltage and post annealing process.
- Development of a more reliable and feasible top-down approach.
- Large-scale NR array with high aspect ratio and distinct non-polar sidewall directly from dry-etching process.
- Investigations on the importance of wet-etching process and evaluation of SBH for NRSBDs

## 5.3 Future perspectives

### 5.3.1 Integration

In this thesis, the top-down approach with etching optimizations was proposed in Chapter 4. As-fabricated NRSBDs could deliver some competitive device performances in some aspects rather than the reported works. However, a relatively large pitch size of 10-µm was typically used in this work, under the premise of keeping a reasonable dielectric RESURF effect, it is significant to integrate more dense NRs to achieve a high total current level. A large-scale NR array with a pitch size of 2-µm, a high aspect ratio, smooth sidewall without roughness, a good perpendicularity could be achieved, as shown in **Fig. 5.1(a)**. Even though some spin-on dielectrics including different types of polyimides and spin-on-glass were used to integrate dense NRs, the NRs near the edge of NR array with a smaller pitch size were totally destroyed during the curing process, as shown in **Fig. 5.1(b)**. This undesired result largely hinders the subsequent device fabrication. Even though the NRs near the center of array could be used, the deposition of contact in precise location become quite difficult because of the smaller pitch size. However, once the contact was deposited in a wrong site, the effect of dielectric RESURF will be influenced, resulting in an undesired device performance. Therefore, it is meaningful to optimize the integration process of dense NW/NRs towards to high-performance nanostructure-based vertical power devices.

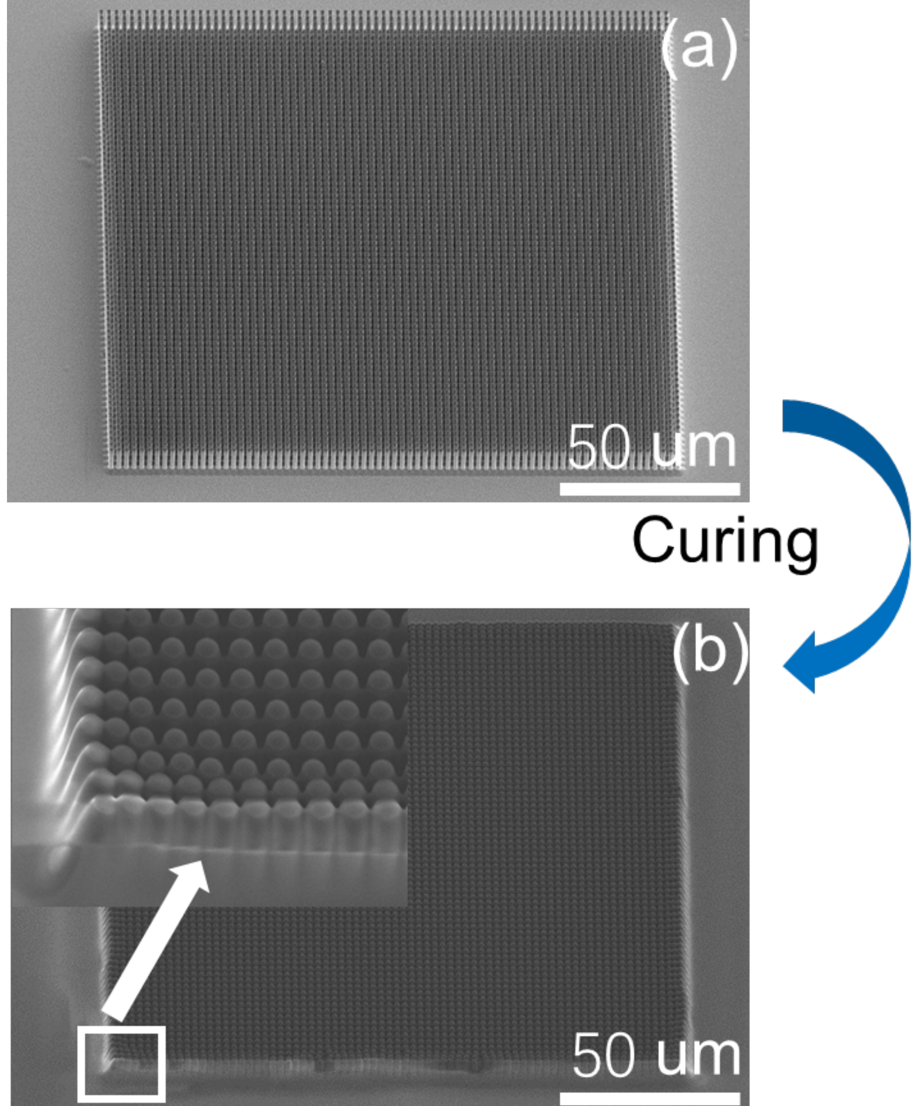


**Figure 5.1: (a)** SEM image of a NR array before filling polyimide. (b) SEM image of a NR array after curing the filled polyimide. Inset: enlarged SEM image of destroyed NRs near the edge of NR array.

### 5.3.2 RESURF-based vertical GaN power devices

For the RESURF-based vertical GaN power devices, the related researches just situate the initial stage. Towards to the further development, it is significative to learn experience from other semiconductors. As another typical WBG semiconductor, the RESURF-based vertical SiC power devices have been extensively studied in the past decade. In terms of manufacturing technology, there are two major methods available for commercial SJ devices nowadays: multiple epitaxial technology **(Fig. 5.2(a)**) and trench fabrication (**(Fig. 5.2(b)**) [1].

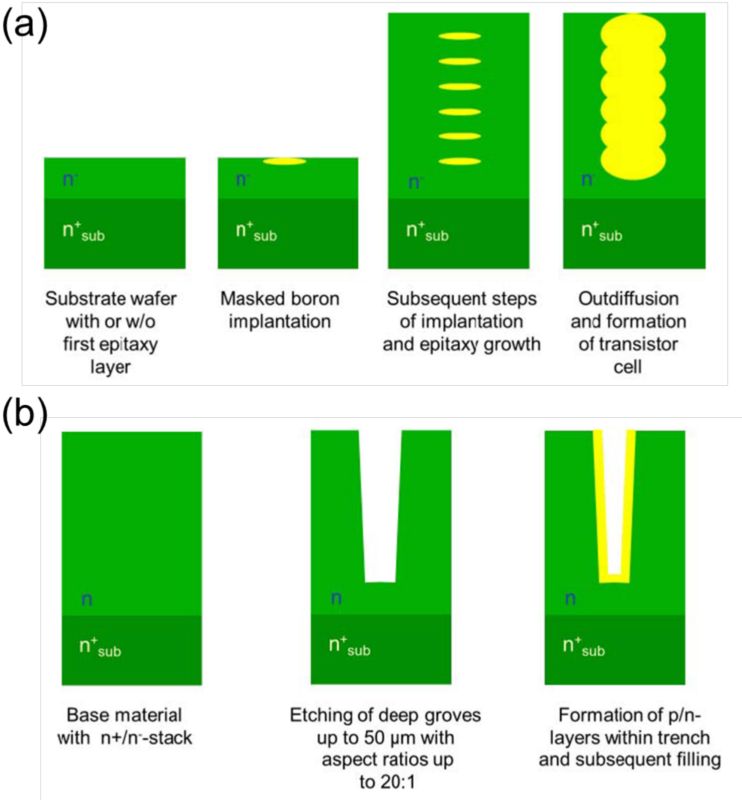


**Figure 5.2:** Fabrication process flow for SJ-based SiC power devices: **(a)** Multiple epitaxial technology. **(b)** Trench technology.

As mentioned in the Chapter 1, it is challenging for GaN because of the difficult selective area doping of p-type GaN [2,3] and contaminated interface after epitaxial regrowth [4,5]. Once major issues for selective area doping of p-type GaN and contaminated regrowth interface could be improved in the future. Sequentially, the RESURF-based vertical GaN power devices will be promptly developed. At that time, the optimized top-down approach presented in this thesis can be regarded as possible option to fabricate the RESURF-based vertical GaN power devices.

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# Publications in PhD Course

## Journals and conference papers

1. **Yaqiang Liao**, Tao Chen, Jia Wang, Wentao Cai, Yuto Ando, Xu Yang, Hirotaka Watanabe, Atsushi Tanaka, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Aman, "Improved device performance of vertical GaN-on-GaN nanorod Schottky barrier diodes with wet-etching process", Appl. Phys. Lett. 120, 122109 (2022).
2. **Yaqiang Liao**, Tao Chen, Jia Wang, Yuto Ando, Wentao Cai, Xu Yang, Hirotaka Watanabe, Jun Hirotani, Atsushi Tanaka, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Aman, "Vertical GaN-on-GaN nanowire Schottky barrier diodes by top-down fabrication approach", Jpn. J. Appl. Phys. 60, 070903 (2021).
3. **Yaqiang Liao**, Tao Chen, Jia Wang, Yuto Ando, Xu Yang, Hirotaka Watanabe, Jun Hirotani, Maki Kushimoto, Manato Deki, Atsushi Tanaka, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Aman, "Dielectric Reduced Surface Field Effect on Vertical GaN-on-GaN Nanowire Schottky Barrier Diodes," in IEEE 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2020, pp. 349-352.
4. Jia Wang, Shun Lu, Wentao Cai, Takeru Kumabe, Yuto Ando, **Yaqiang Liao**, Yoshio Honda, Ya-Hong Xie, and Hiroshi Amano, "Ohmic Contact to p-Type GaN Enabled by Post-Growth Diffusion of Magnesium", IEEE Electron Device Lett. 43, 150 (2022).
5. Jia Wang, Guo Yu, Hua Zong, **Yaqiang Liao**, Weifang Lu, Wentao Cai, Xiaodong Hu, Ya-Hong Xie, and Hiroshi Amano, "Non-polar true-lateral GaN power diodes on foreign substrates", Appl. Phys. Lett. 118, 212102 (2021).
6. Geoffrey Avit, Yoann Robin, **Yaqiang Liao**, Hu Nan, Markus Pristovsek, and Hiroshi Amano, "Strain-induced yellow to blue emission tailoring of axial InGaN/GaN

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8. Yoann Robin, **Yaqiang Liao**, Markus Pristovsek, and Hiroshi Amano, “Simultaneous Growth of Various InGaN/GaN Core-Shell Microstructures for Color Tunable Device Applications”, Phys. Status Solidi A 215, 1800316 (2018).

## International conference (first author)

1. **Yaqiang Liao**, Tao Chen, Jia Wang, Yuto Ando, Xu Yang, Hirotaka Watanabe, Jun Hirotani, Maki Kushimoto, Manato Deki, Atsushi Tanaka, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Aman, "Dielectric Reduced Surface Field Effect on Vertical GaN-on-GaN Nanowire Schottky Barrier Diodes," 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), ISPSD-32, September 13-19, 2020, Virtual conference
2. **Yaqiang Liao**, Jia Wang, Yuto Ando, Xu Yang, Jun Hirotani, Maki Kushimoto, Manato Deki, Atsushi Tanaka, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Aman, "Fabrication of GaN-on-GaN Vertical Nanowire Schottky Barrier Diode by Top-down Approach," ICNS-13, July 7-12, 2019, Bellevue, Washington (the United States).
3. **Yaqiang Liao**, Yuto Ando, Xu Yang, Jun Hirotani, Maki Kushimoto, Atsushi Tanaka, Yoann Robin, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Amano, "GaN-on-GaN Vertical Nanowire Schottky Barrier Diode Fabricated by Top-down Approach," IWN2018, November 11-16, 2018, Kanazawa (Japan)
4. **Yaqiang Liao**, Yuto Ando, Xu Yang, Hirotaka Watanabe, Jun Hirotani, Maki Kushimoto, Manato Deki, Atsushi Tanaka, Shugo Nitta, Yoshio Honda, Kevin J. Chen, and Hiroshi Aman, "Fabrication of Uniform GaN Nanowire Array with Smooth Non-polar Facets by Top-down Approach," ISPlasma-10, March 4-8, 2018, Nagoya.

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