Study on Common-Mode Noise Reduction Methods in Non-Isolated DC–DC Converters

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Best Regards

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ABSTRACT

This paper discusses common mode (CM) noise reduction methods in non-isolated DC–DC converters.

Recently, the demand for switched-mode power supplies (SMPSs) has been increasing because of increasing power generation in renewable energy generations and power consumption in electrified transportation and data centers. Especially in SMPSs, non-isolated DC–DC converters are employed in various applications. But, on the other hand, the electromagnetic noise emitting from SMPSs becomes problematic.

SMPSs are demanded to have high power density. Therefore, the operation frequency of SMPSs is increasing to achieve higher power density. Wide band gap (WBG) devices utilizing silicon carbide and gallium nitride are employed in SMPSs for high-frequency operation because of the high dv/dt and di/dt ratio. However, the high-frequency operation and the high dv/dt and di/dt ratio increase electromagnetic noise. Especially, Common mode (CM) noise that flows through the ground is difficult to suppress. Therefore, many studies have been made on CM noise reduction methods.

Thus, the purpose of this paper is to propose CM noise reduction methods in non-isolated DC–DC converters for high-power density. First, CHAPTER 1 explains the social background of increasing demand for SMPSs and the background of CM noise in SMPSs. The purpose of the dissertation and the research subject area are also explained at the end of CHAPTER 1. CHAPTER 2 explains the technical background of noise evaluation in SMPSs. Then, three CM noise reduction methods are proposed in CHAPTER 3, 4, and 5. The summaries of the chapters are described below.

In CHAPTER 3, the CM noise reduction method with an auxiliary winding is proposed for a multiphase interleaved DC–DC converter with a coupled inductor. The proposed method

decreases CM noise by adding an auxiliary winding and a capacitor not to degrade the power density. In this chapter, the CM noises in the conventional multiphase interleaved DC–DC converter and the proposed circuit are compared mathematically. Then the limitation of the CM noise reduction performance and the design guidelines for the auxiliary winding is indicated. Finally, the experiment verifies that the proposed circuit shows the CM noise reduction performance as expected.

In CHAPTER 4, the CM noise reduction method with reversed circuit configuration is proposed for the non-isolated boost DC–DC converter. The circuit components do not change, but the circuit configuration changes in the reversed circuit configuration. In this chapter, the CM noises in the conventional non-isolated boost DC–DC converter and the proposed circuit are compared, and the CM noise reduction performance is analyzed mathematically. Then, the implementation method to verify the CM noise reduction effect is explained. Lastly, the CM noise reduction effect is verified in the circuit simulation and the experiment. Additionally, the conditions where the proposed circuit configuration is effective are discussed.

In CHAPTER 5, the combination of thermal pads in switching devices is proposed to reduce the CM noise in the non-isolated DC–DC converter. The proposed method increases the impedance of the CM noise propagation path and decreases the CM noise by arranging the thermal pads of switching devices. In this chapter, the CM noise in the non-isolated DC–DC converter is first analyzed, and the impedance of the CM noise propagation path is clarified. Additionally, the influence of the thermal pad of the switching device on the CM noise is discussed. Then, the circuit implementation method to compare the influences of thermal pads on the CM noise is explained. Finally, the circuit simulation and the experiment verify that the combination of thermal pads reduces the CM noise.

CHAPTER 6 compares the strong and weak points of the abovementioned methods and

summarizes this dissertation.

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CHAPTER 1: RESEARCH BACKGROUND

1.1. Glowing Demand for Switched-Mode Power Supplies

Owing to the rising global concern for energy and environmental issues, energy generation and consumption have been reconsidered worldwide. Electrified transportation, such as electrified vehicles and aircrafts, has attracted attention as a viable solution. Power generation using renewable energy, such a photovoltaic and wind energies, is not dependent on exhaustible resources and greenhouse gas emissions. In addition, the data traffic has been increasing exponentially, due to which the increased consumption of electric energy for data processing and transmission in data centers has drawn considerable attention over the years. Switched-mode power supplies (SMPSs) are the most commonly used power electronics systems in transportation, renewable energy generation, and data centers to manage the consumption of electric energy. Therefore, SMPSs must have high power density and be highly efficient to meet the growing demand. Hence, in this chapter, the global trends of electrified transportation, renewable energy generation, and data centers as well as the SMPSs utilized in these systems are reviewed.

1.1.1. Electrified Transportation

The number of electric vehicles (EVs) has increased in the past decade worldwide[1]. The governments of several countries have set goals for EV sales and installation of EV chargers to increase EV penetration rates for a sustainable society[2]-[8]. An example of a power electronics system in a battery-operated EV is shown in Fig. 1-1[9]-[11]. Two types of chargers are for EVs (Fig. 1-1): on-board chargers and quick chargers. As shown in the right half of Fig. 1-1, the power is supplied to a motor through the non-isolated DC–DC converter and inverter to move the car. Furthermore, the power is converted into lower voltage with isolation to power the accessories.

An electrified aircraft (EA) is also considered as a type of electrified transportation. Currently, the governments are attempting to pave the way for the development, production, and operation of EAs[12]-[14], and several manufactures have already produced EAs[14]-[17]. An example of a power electronics system in an EA is shown in Fig. 1-2[18]-[20]. The power density of EAs is more weight-directed to fly longer distances. From the weight perspective, the use of a battery as an energy source is disadvantageous because the weight of the battery does not decrease depending on the state of charge, whereas a fuel tank becomes lighter as the fuel is consumed.

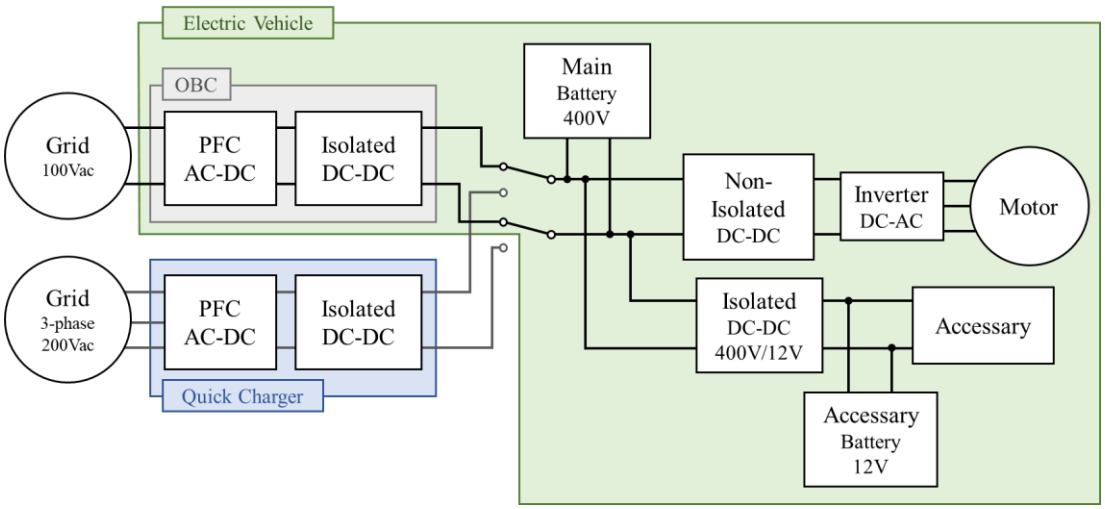


Fig. 1-1. Example of power electronics system in EV[9]-[11].

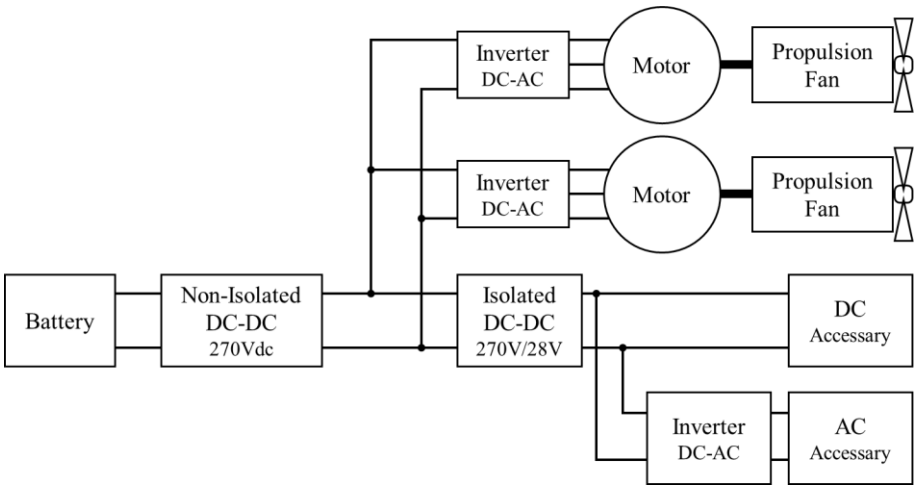


Fig. 1-2. Example of power electronics system in EA[18]-[20].

1.1.2. Renewable Energy Generation

Renewable energy generation is considered as a substitute for exhaustible energy to save resources such as fossil fuels and helps prevent air pollution. Owing to these advantages, renewable energy production has been increasing worldwide[21]. Furthermore, the improvement in the production of renewable energy using wind and photovoltaic energies is remarkable. The penetration rate of renewable energy is also increasing and has drawn considerable attention similar to that of EVs. An example of a power electronics system in photovoltaic energy generation is shown in Fig. 1-3[22]-[24]. The DC–DC converters associated with the PV modules are connected in series to output high voltage such as 400 V to the DC bus. In addition, the grid interconnection inverter is connected to the DC bus. However, wind and photovoltaic power generation systems have unstable power supplies depending on weather and period. Therefore, to overcome this problem, renewable energy generation systems include an energy storage system to maintain constant power supply[25]–[28]. The use of SMPSs in energy storage systems has been increasing because they are bidirectional to charge and discharge. Among the SMPSs, non-

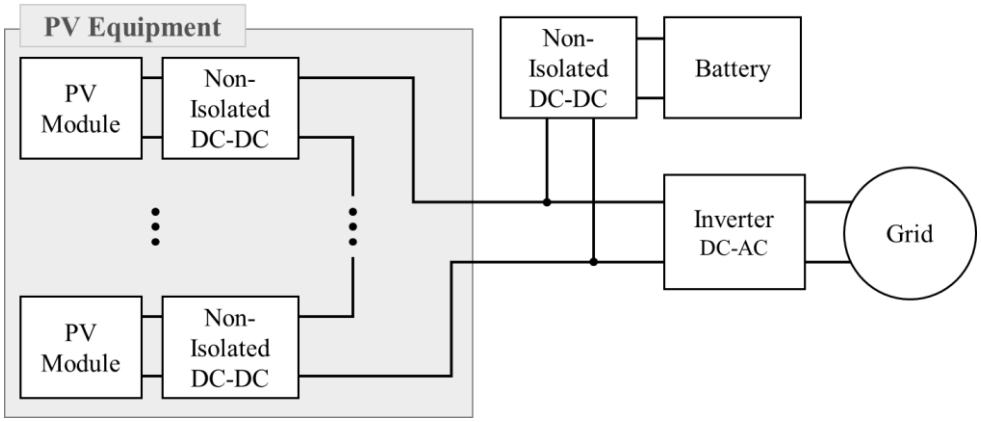


Fig. 1-3. Example of power electronics system in photovoltaic generations[22]-[24].

isolated DC–DC converters or dual active bridge (DAB) converters are the typically employed systems[25]-[28].

1.1.3. Data Centers

The world's internet traffic was forecasted to increase by more than triple from 1.46 zettabytes in 2017 to 4.75 zettabytes in 2022[29]. Thus, the amount of energy consumption to process and transmit the data was estimated to increase[30]-[32], and several companies issued a specification for server racks to improve the efficiency of data centers[33], [34].

An example of a power electronics system used in data centers is shown in Fig. 1-4[35]-[38]. These power electronics systems maintain the electric power in low voltage and large current because the system consists of several low voltage energy consumers such as computer processing units connected in parallel. Therefore, electrical energy is distributed through a higher voltage bus as long as possible and converted into lower voltage through several steps to decrease copper loss. For example, as shown in Fig. 1-4, an isolated DC–DC converter in a server rack, a switched tank converter[37] on a server board, and point of load converters for information technology loads work as step-down converters.

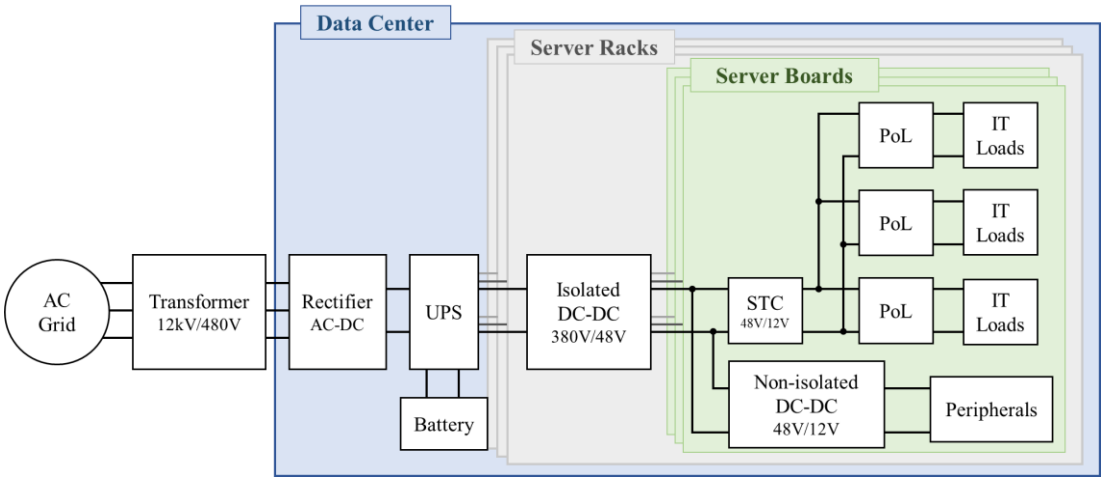
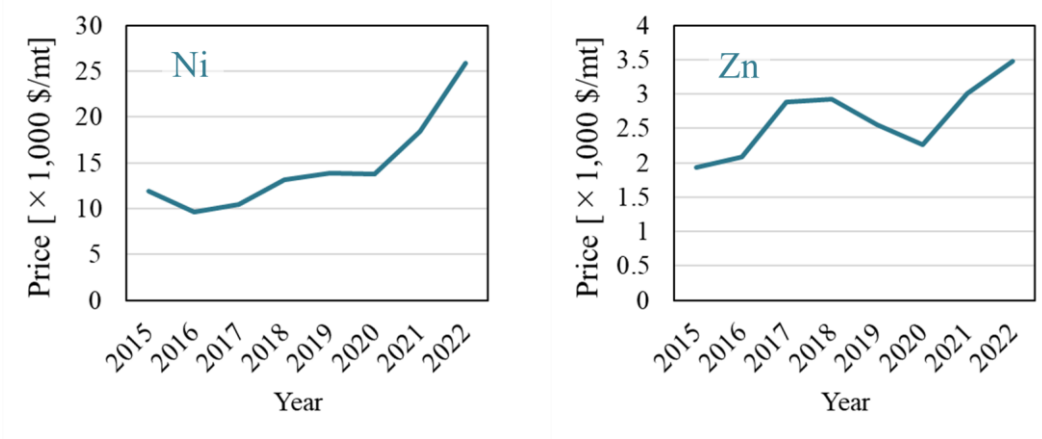


Fig. 1-4. Example of power electronics system in data centers[35]-[38].

1.2. Requirements for SMPSs

As reviewed in Sections 1.1.1 to 1.1.3, the demand for SMPSs has been increasing owing to global energy and environmental concerns. However, SMPSs have a few challenges in terms of limits on the installation space and materials. Typically, the space containing an SMPS is decided at the early stage of system design. Therefore, an SMPS must be designed to fit in the appointed space. In addition, the cost of the materials used in an SMPS, especially that of magnetic materials such as nickel and zinc, has increased in recent years. The price trends of nickel and zinc are shown in Fig. 1-5 (a) and (b)[39]. Hence, the use of these materials should be reduced to make the SMPS more cost-effective. Furthermore, the challenges in terms of space and materials can be solved by reducing the volume and weight of the SMPS.



(a) (b)

Fig. 1-5. Price trends of (a) nickel and (b) zinc[39].

One method to reduce the volume and weight of SMPS is high-frequency operation. A typical on-board non-isolated DC–DC converter, shown in Fig. 1-6, has passive components such as inductors and a capacitor that occupy a large space, which contribute to its large volume and weight. However, high-frequency switching downsizes the volume and weight of the passive

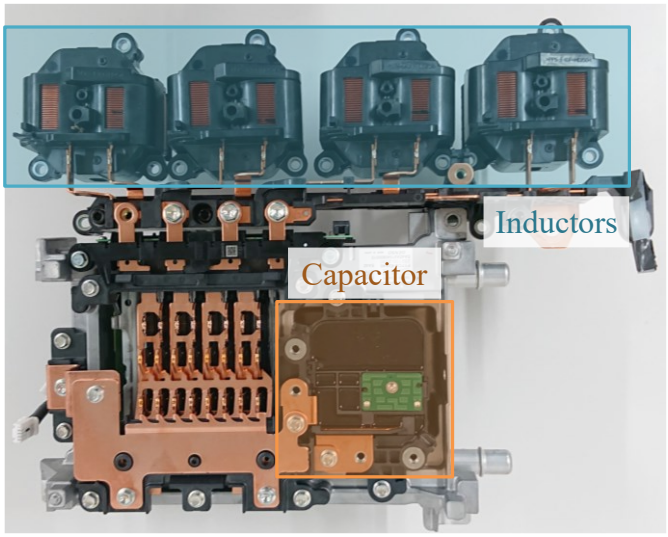


Fig. 1-6. On-board non-isolated DC-DC converter.

components. Therefore, the high-frequency operation of SMPSs reduces the volume and weight by downsizing the passive components. In addition, the use of magnetic materials decreases by downsizing the magnetic components such as inductors.

Consequently, high-frequency operation solves the abovementioned problems of limited space and materials. Then, the following section states a method to realize high-frequency switching.

1.3. Wide Bandgap Semiconductor Devices in SMPSs

Several wide bandgap (WBG) devices such as gallium nitride (GaN) and silicon carbide (SiC) are utilized in SMPSs. WBG devices achieve highly efficient power conversion because of the high dv/dt and di/dt ratio and low switching loss. The typical use range map of the WBG devices is shown in Fig. 1-7[40]-[53]. Compared with Si devices, SiC devices are power-oriented and commonly used in higher voltage conversion to achieve low switching loss in high-power applications[40]-[47], whereas GaN devices are frequency-oriented and used for higher frequency conversion to achieve low switching loss in high-frequency applications[48]-[53]. The high-power

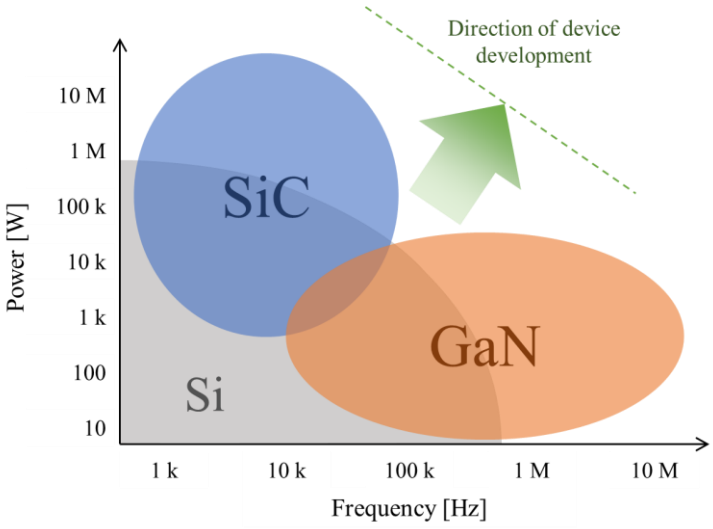


Fig. 1-7. Typical use range map of WBG devices[40]-[53].

and high-frequency operation results in the downsizing of SMPSs. Thus, WBG devices significantly contribute to the high power density and efficiency of SMPSs.

However, the high-frequency switching operation and high *dv*/*dt* and *di*/*dt* ratio result in significant electromagnetic noise, also called "electromagnetic interference" (EMI). EMI is reported to cause severe malfunctions in power electronics systems. For example, SMPSs in electric vehicles cause EMI that degrades the performance of controller area network communication systems adjacent to power lines[54], [55]. In a grid, EMI in high-voltage power lines is reported to induce a current in nearby buried gas pipelines. The induced current causes coating defects and derates the insulation flange in the pipeline[56], [57].

Furthermore, medical devices experience EMI. For example, cardiac pacemakers and electrocardiographs are reported to experience EMI when placed near communication devices or other power networks[58]-[60]. Therefore, EMI should be reduced for the efficient use of WBG devices and to achieve high-power-density SMPSs. Furthermore, considerable research has been conducted on reducing common mode (CM) noise[61]-[69]. CM noise propagates through the

ground and has attracted attention because it dominates the frequency band, wherein WBG devices increase the noise. Therefore, reducing CM noise while operating WBG devices is essential.

1.4. Common-Mode Noise Reduction Methods

CM noise reduction methods are classified into several types in accordance with a previous study [70] as follows: methods against the noise sources and methods against the propagation paths. The classification of CM noise reduction methods is shown in Fig. 1-8. Then, each category is explained in the following sections.

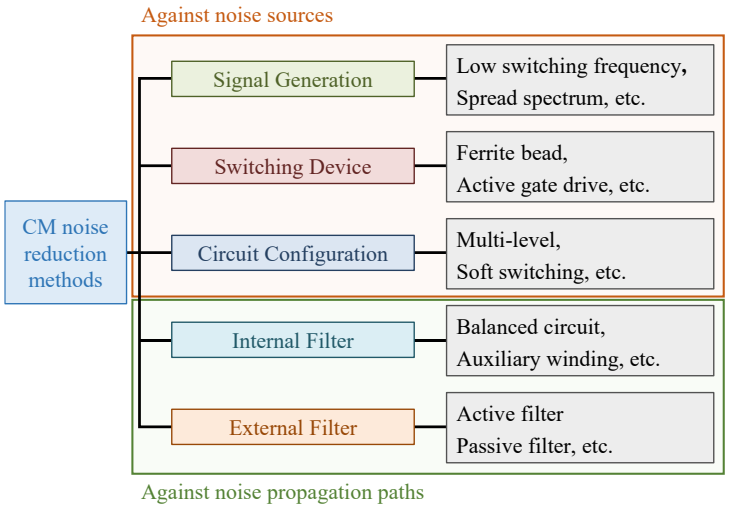


Fig. 1-8. Groups of CM noise reduction methods[70].

1.4.1. Noise Reduction Methods Against Noise Sources

Noise reduction methods against noise sources change the waveform of the noise voltage or current sources. These methods are further divided into three types: signal control, switching devices, and circuit configuration. The applications of these methods in a circuit configuration are illustrated in Fig. 1-9.

Noise can be reduced by modifying the signal input of gate drive circuits, and the simplest

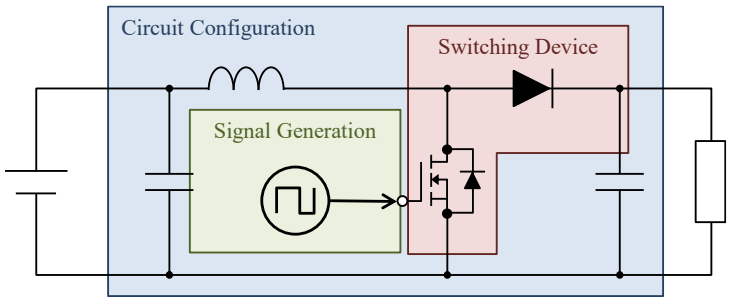


Fig. 1-9. Noise reduction methods against noise sources.

example is lowering the switching frequency. The switching frequency of a noise source greatly influences the spectrum. Noise in high frequency decreases when the switching frequency is lowered, although the amplitude and duty ratio are stable. However, lowering the switching frequency results in larger passive components. To overcome this, pulse width modulation (PWM) methods for noise reduction are proposed. For example, spread spectrum methods achieve reduced switching frequency harmonics by randomly changing the switching frequency or the duty ratio in each period[71], [72]. The simplified frequency characteristic of the noise source with the spread spectrum method is shown in Fig. 1-10. The harmonics elements decrease with the spread spectrum method. In addition, the PWM method switches a pair of switching nodes in a 3-phase inverter simultaneously but symmetrically such that the generated noise currents cancel

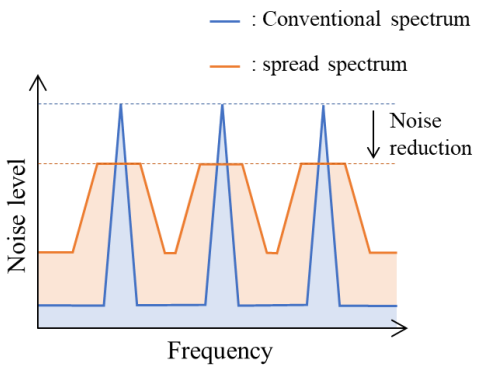


Fig. 1-10. Simplified spectrum with spread spectrum method[71], [72].

each other[73]. The PWM method rarely increases the volume of SMPSs but requires high-performance controllers, and the frequency band in which noise reduces is limited depending on the drive frequency of the controller.

Moreover, noise reduction methods that arrange components around the switching devices are available. For example, a snubber circuit or a large gate resistance attenuates noise by decreasing the *dv*/*dt* ratio. However, a low *dv*/*dt* ratio leads to a large switching loss. Therefore, there is a trade-off between noise and switching loss. To overcome this, active gate drive circuit configurations are proposed to change the waveform of the noise voltage source and reduce harmonics while stably maintaining or even reducing the switching loss[74]. However, the active gate drive circuit requires additional components to modify gate input. Furthermore, switching module structures are used for noise reduction, for example, the reduction of loop inductance using an inductance canceling structure, flip chip structure, and internal decoupling capacitor[75]-[77]. Loop inductances around the switching devices are shown in Fig. 1-11. Loop inductances often cause resonance and switching surges when the switches are turned on and off. Therefore, these devices reduce the loop inductances to avoid voltage breakdown and noise; however, employing the new switching module structure is expensive.

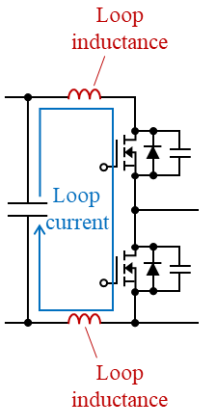


Fig. 1-11. Loop inductances around switching devices[75]-[77].

The noise source can also be changed by using the circuit structures of SMPSs. For example, a multi-level converter structure reduces the voltage stress on a switch and reduces harmonic distortion of the output voltage. Therefore, a multi-level configuration can downsize the output filter. Moreover, a circuit configuration that enables soft switching also reduces noise, for example, zero voltage switching waveform (Fig. 1-12). Soft switching reduces noise because the soft switching noise source has lower *dv*/*dt* and *di*/*dt* ratios and includes smaller harmonics than hard switching and simultaneously decreases the switching loss[78]. However, the number of circuit structures that are required to achieve multi-level structure or soft switching is limited.

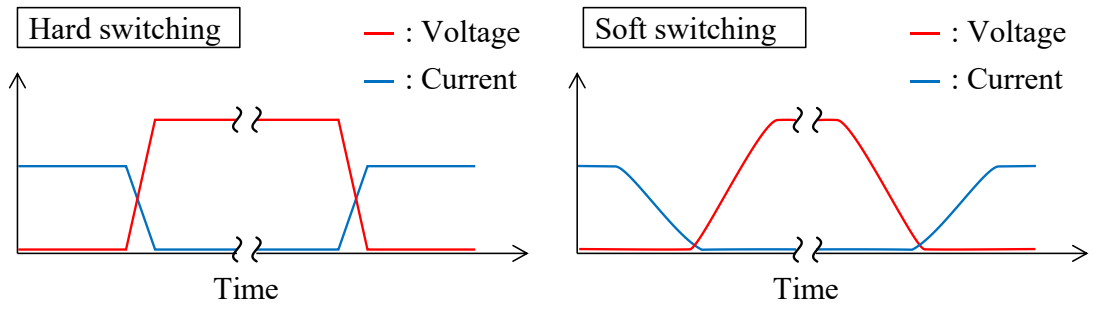


Fig. 1-12. Waveform in hard switching and soft switching[78].

1.4.2. Noise Reduction Methods Against Propagation Paths

Noise reduction methods against propagation paths do not change the waveform of noise voltage sources or current sources but prevent the noise from emitting out of the system. These methods are further divided depending on the type of filter used: internal or external. Application areas of these methods in a circuit configuration are illustrated in Fig. 1-13.

Internal filters are modified circuit structures that also function as EMI filters, for example, a non-isolated boost DC–DC converter with a balanced circuit configuration (Fig. 1-14). The balanced technique cancels CM noise by equally distributing the impedance among power lines [61]-[63]. A non-isolated boost DC–DC converter with an auxiliary winding is shown in Fig. 1-15.

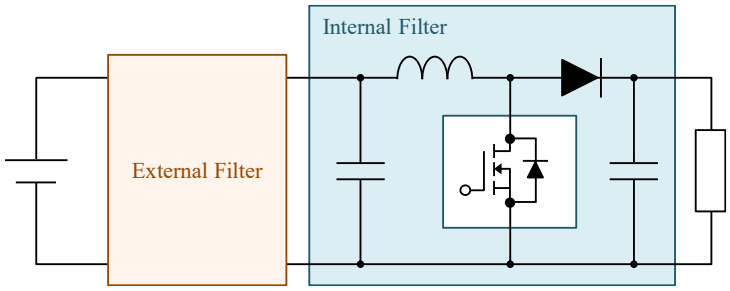


Fig. 1-13. Noise reduction methods against noise propagation paths.

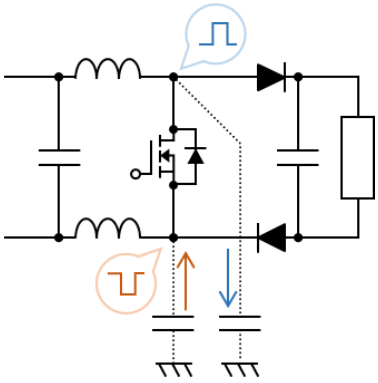


Fig. 1-14. Boost converter with balanced circuit configuration[61]-[63].

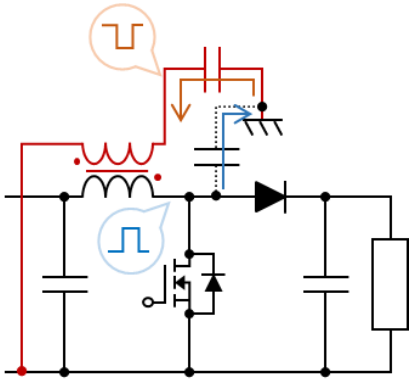


Fig. 1-15. Boost converter with an auxiliary winding[64], [65].

Auxiliary windings are added to the boost inductor or output choke coil to generate an anti-phase noise voltage source and cancel the CM noise current[64], [65].

External filters do not change the circuit structures but filter EMI using additional components. External filters are typically designed and added at the final stage after the EMI of SMPSs is measured; therefore, they can be easily adjusted by trial and error. Passive filters consist

of passive components such as inductors and capacitors, which have a large volume[79]-[81]. Therefore, passive filters often degrade the power density of SMPSs. Several studies on passive filters have been conducted to improve the power density and noise reduction performance by integrating multiple filters, arranging grounding wires, and canceling near magnetic fields[66], [67], [82], [83]. Furthermore, active filters improve the power density of external filters by detecting the noise current in the power line and injecting the canceling current using amplifiers simultaneously[68], [69]. However, the effective frequency band of an active filter strongly depends on the response speed of the amplifier. Therefore, an active filter cannot decrease the noise at a frequency higher than a certain frequency band owing to the performance limitation of the amplifier.

1.5. Purpose of the Dissertation

In response to the EMI problem, various noise measures have been developed in different circuit configurations, as explained in Section 1.4. Simultaneously, SMPSs are intended to achieve high power density with WBG devices. Therefore, the purpose of this dissertation is to propose CM noise reduction methods that are suitable for high-power-density SMPSs without increasing their weight and volume. The proposed methods are applied for non-isolated DC–DC converters that are used in most of the power electronics systems mentioned in Section 1.1.

The proposed CM noise reduction methods are a type of internal filters that reduce the CM noise using few additional components. The associations between the proposed noise reduction methods are shown in Fig. 1-16. In addition, the characteristics of each proposed method are compared in Table 1-1. Each proposed method has suitable conditions for CM noise reduction. This dissertation offers in-depth discussions on multiple CM noise reduction methods, which are useful for the reduction of CM noise under a wide range of conditions.

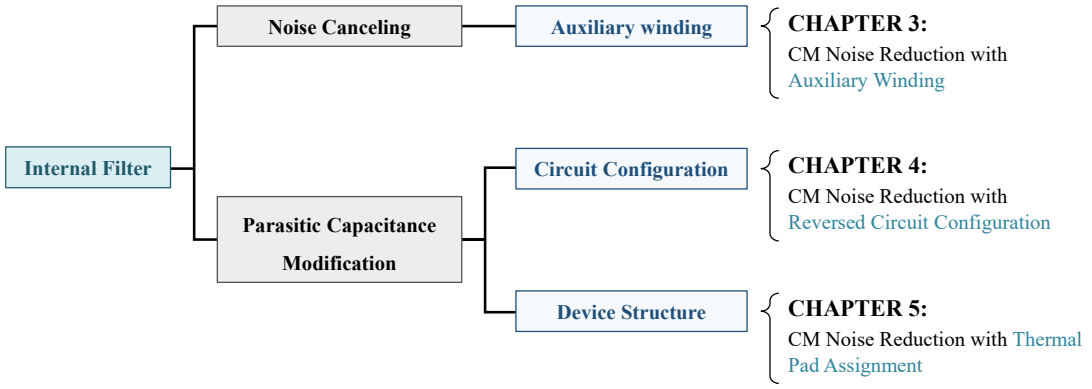


Fig. 1-16. Proposed methods in groups of CM noise reduction methods shown in Fig. 1-8.

Table 1-1 Characteristics of proposed CM noise reduction methods.

	Strong points	Weak points
CHAPTER 3 Auxiliary winding	- Small increase in volume & weight - Available for any number of phases	- CM noise reduction frequency band is limited by leakage inductance L_{lk3}
CHAPTER 4 Reversed configuration	- No increase in volume & weight - No change in circuit components	- Not for MOSFETs with thermal pad connected to source terminals - Thermal pads of diodes are required to be selectable
CHAPTER 5 Thermal pad assignment	- No increase in volume & weight - No change in circuit configuration	- Switching devices with selectable thermal pads are necessary

1.6. Outline of the Dissertation

The remainder of this dissertation is organized as follows: in Chapter 2, the basic knowledge of EMI is explained. In Chapter 3, the CM noise reduction method with auxiliary winding categorized as a noise canceling method is proposed (Fig. 1-16). In Chapters 4 and 5, the CM noise reduction methods that modify the parasitic capacitance are proposed; however, these

methods differ in the implementation method. Reversed circuit configuration to reduce the parasitic capacitance is proposed in Chapter 4, and the influence of the thermal pad assignment on the parasitic capacitance is discussed in Chapter 5. Finally, the dissertation is summarized in Chapter 6.

CHAPTER 2: INTRODUCTION TO EMI

2.1. Electromagnetic Compatibility and EMI

Electromagnetic compatibility (EMC) should be improved to avoid problems originating from unwanted electromagnetic noise. EMC consists of EMI and electromagnetic susceptibility (EMS). The components of EMC are shown in Fig. 2-1. EMI is an influence caused by electrical equipment on the surrounding electromagnetic environment or the ability of the electrical equipment to cause the influence. EMI is also called emission. By contrast, EMS is the tolerance of electrical equipment to the influence originating from the surrounding electromagnetic environment. EMS is also called immunity. Thus, EMC is the ability of electrical equipment not to influence the surrounding electromagnetic environments and not to be influenced by the surrounding electromagnetic environments.

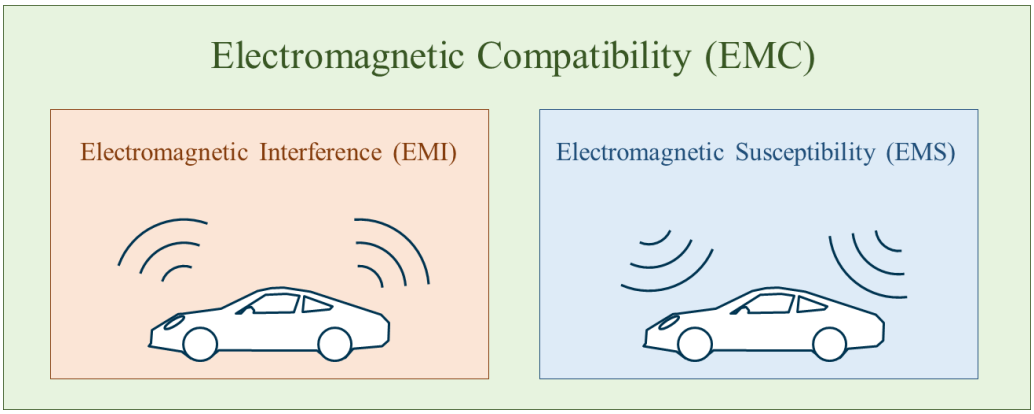
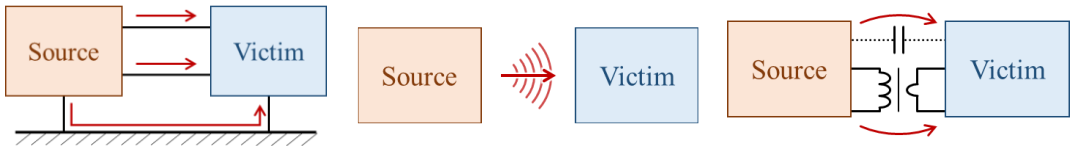


Fig. 2-1. Components of EMC

In power electronics systems, SMPSs mediate between the power sources and the loads. Therefore, SMPSs always handle the largest power and become the most significant noise source in the power electronics system. Owing to this characteristic, most of the research on the EMC of SMPSs is concentrated on the EMI of SMPSs. Typically, EMI is divided into three categories

depending on the propagation path: conductive, radiative, and coupled interferences. Simplified figures of propagation paths are shown in Fig. 2-2 (a), (b), and (c). In conductive interference, electromagnetic noise between the noise source and the noise victim propagates through the conductors such as wires or ground planes in the form of current. In radiative interference, electromagnetic noise propagates through an insulator as an electromagnetic wave and propagates far distances. Finally, in coupled interference, electromagnetic noise propagates through the insulator but in the form of capacitive or inductive coupling and propagates close distances. Generally, conductive interference is evaluated in a lower frequency band compared with radiative interference. For example, in the international standard CISPR 25, which is the standard for vehicles, boats, and internal combustion engines, the limit for conducted disturbances is specified to range from 150 kHz to 108 MHz. By contrast, the limits for radiated disturbances are up to 2.5 GHz. However, coupled interference is usually evaluated in a broad bandwidth but is not specified in standards.



(a) (b) (c)

Fig. 2-2. Categories of EMI: (a) conductive interference, (b) radiative interference and (c) coupled interference.

2.2. Evaluation of EMI

When evaluating EMI, the evaluation system is generally divided into three components: noise sources, propagation paths, and measurement equipment. A simplified noise evaluation system is shown in Fig. 2-3.

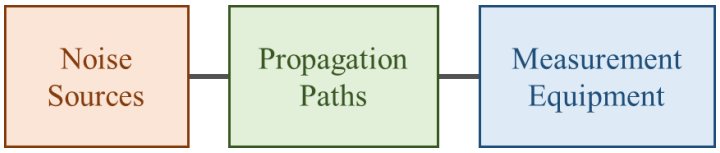


Fig. 2-3. Simplified noise evaluation system.

Noise sources are the nonlinear electric fluctuations that cause EMI and are substituted with voltage or current sources in analysis. Typically, the drain-source voltage of metal oxide semiconductor field effect transistors (MOSFETs), the collector-emitter voltage of insulated gate bipolar transistors (IGBTs), or the reverse voltage of diodes are considered noise sources. However, electric fluctuations such as arc discharge can also be considered as noise sources. Therefore, understanding the frequency characteristics of noise sources is significant for EMI analysis.

The propagation paths mediate between the noise sources and measurement equipment; therefore, propagation paths decide the gain characteristics between these structures. Hence, the EMI can change depending on the propagation paths, although the noise sources do not change. In most cases, equipment under test (EuT) of the EMI analysis consists of noise sources and propagation paths.

Measurement equipment is not included in EuT and the actual application but acts as a substitute for EMI victims in noise evaluation. In the noise evaluation system, line impedance stabilization network (LISN) eliminates the influence from outside the system and secures the reproducibility of the measurement.

In this section, these components of a noise evaluation system are explained in more detail.

2.2.1. Waveform and Spectrum of Noise Sources

The source of EMI should be understood to improve the EMC. For example, a noise source in a non-isolated DC–DC converter circuit is shown in Fig. 2-4. EMI originates from the nonlinear

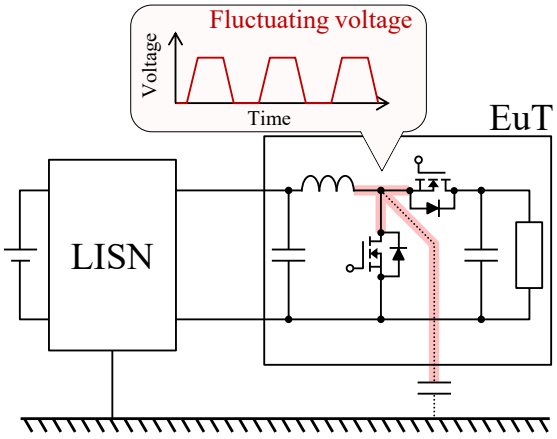


Fig. 2-4. Noise source in non-isolated DC-DC converter.

and steep voltage or current fluctuations caused by the switching devices in SMPSs. Therefore, EMI should increase when the noise source becomes larger. Herein, a complex Fourier series expansion of the noise voltage source is conducted to analyze the influence of the noise source.

The simplified waveform of noise voltage source $v_{\mathrm{noise}}(t)$ is shown in Fig. 2-5. In most cases, the noise voltage source shows a trapezoidal waveform, as in Fig. 2-5, and has parameters such as frequency, amplitude, duty ratio, rise time, and fall time. However, the noise terminal voltage is evaluated in the frequency domain in the case of EMI. Therefore, the relationship between the waveform and the spectrum of the noise voltage source is analyzed in this study to understand the

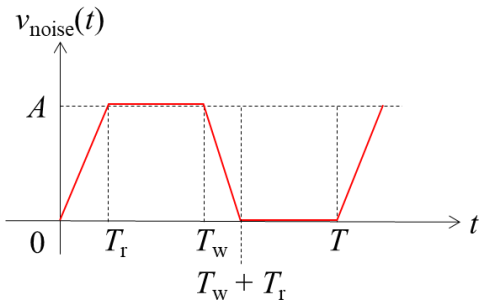


Fig. 2-5. Typical waveform of noise voltage source.

influence of noise voltage sources on EMI. In particular, the influence of short rise and fall time and high switching frequency, which are characteristics of WBG devices, is explained.

In Fig. 2-5, A is the amplitude; both the rise and fall times are denoted as T_r for simplification; T_w is the pulse width; and T is the period. The noise voltage source $v_{noise}(t)$ in Fig. 2-5 is expressed in the following equation:

$$v_{noise}(t) = \begin{cases} \frac{A}{T_r}t, & (0 \le t < T_r) \\ A, & (T_r \le t < T_w) \\ -\frac{A}{T_r}t + \frac{A(T_r + T_w)}{T_r}, & (T_w \le t < T_w + T_r) \\ 0, & (T_w + T_r \le t \le T) \end{cases} \quad \cdots\cdots (2\text{-}1)$$

To perform the analysis in the frequency region, a complex Fourier series expansion is conducted. The noise voltage source $v_{noise}(t)$ is derived with complex Fourier series expansion as follows:

$$v_{noise}(t) = C_0 + \sum_{n=\pm 1}^{\pm\infty} C_n e^{\frac{j2n\pi t}{T}} \quad \cdots\cdots (2\text{-}2)$$

Here, C_0 and C_n are derived as follows:

$$\begin{cases} C_0 = A\frac{T_w}{T} \\ C_n = A\frac{T_w}{T}\mathrm{sinc}\left(\frac{n\pi T_r}{T}\right)\mathrm{sinc}\left(\frac{n\pi T_w}{T}\right)e^{\frac{-jn\pi(T_w+T_r)}{T}} \end{cases} \quad \cdots\cdots (2\text{-}3)$$

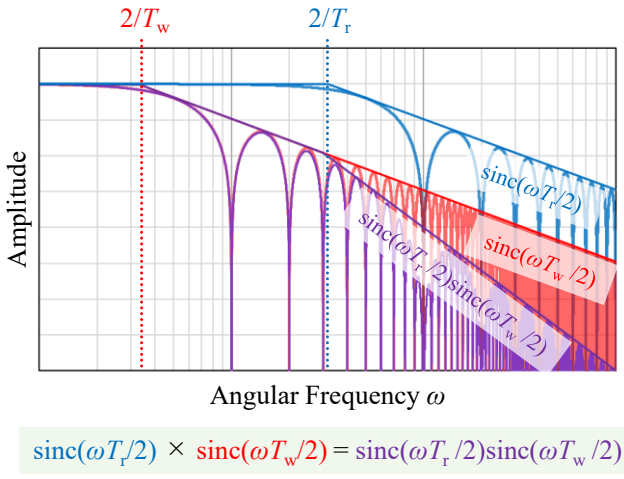
From (2-2) and (2-3), $v_{noise}(t)$ is expressed as follows:

$$v_{noise}(t) = Ad + Ad\sum_{n=\pm 1}^{\pm\infty} \mathrm{sinc}\left(\frac{\omega_n T_r}{2}\right)\mathrm{sinc}\left(\frac{\omega_n T_w}{2}\right)e^{j\omega_n\left\{t - \frac{(T_w + T_r)}{2}\right\}} \quad \cdots\cdots (2\text{-}4)$$

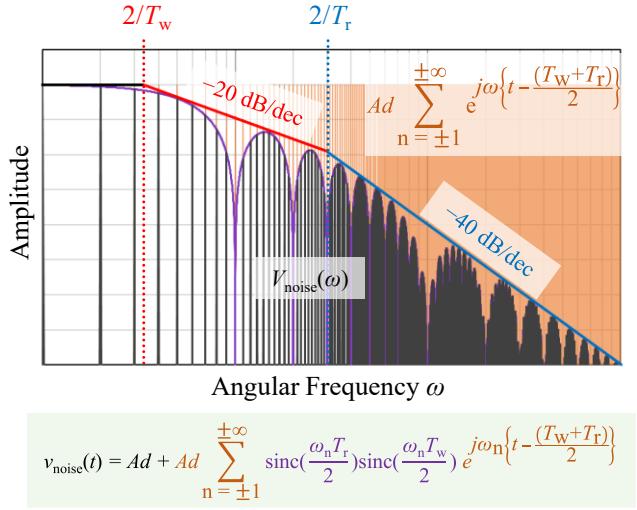
, where d is the duty ratio and $d = T_w / T$, and ω_n is n^{th} harmonics of angular frequency $\omega_1 = 2\pi / T$ and $\omega_n = 2n\pi / T$. An example spectrum of $v_{noise}(t)$ is shown in Fig. 2-6. In (2-4), the first term Ad indicates the DC element of $v_{noise}(t)$. Therefore, the second term decides the frequency characteristic of $v_{noise}(t)$. In the second term, $\mathrm{sinc}(\omega T_r/2)$ indicates the characteristics of the envelope that decreases by 20 dB/dec over $\omega = 2/T_r$. Similarly, the envelope of $\mathrm{sinc}(\omega T_w/2)$ decreases by 20 dB/dec over $\omega = 2/T_w$. As $T_r < T_w$, the envelope of $\mathrm{sinc}(\omega T_r/2)\mathrm{sinc}(\omega T_w/2)$ decreases by 20 dB/dec over $\omega = 2/T_w$ and decreases by 40 dB/dec over $\omega = 2/T_r$, as shown in Fig.

2-6 (a). Furthermore, $Ad\sum_{n=\pm1}^{\pm\infty} e^{j\omega_n\left\{t-\frac{(T_W+T_r)}{2}\right\}}$ indicates the summation of harmonics of ω_1 with stable amplitudes of Ad. Thus, $v_{noise}(t)$ in (2-4) is the summation of harmonics of ω_1 with the envelope that decreases by 20 dB/dec over $\omega = 2/T_w$ and decreases by 40 dB/dec over $\omega = 2/T_r$, as shown in Fig. 2-6 (b).

From (2-4), the dv/dt ratio greatly influences the spectrum of the noise voltage source. As



(a)



(b)

Fig. 2-6. Spectral analysis of (a) $\mathrm{sinc}(\omega T_r/2)\mathrm{sinc}(\omega T_w/2)$ and (b) $v_{noise}(t)$ in (2-4).

examples, several trapezoidal waveforms and the spectra with different T_r are compared in Fig. 2-7. In Fig. 2-7 (a) and (b), all waveforms have the same amplitude, frequency, and duty ratio; however, the rise and fall times differ: T_r = 10.0 ns, 50.0 ns, and 250 ns. As a result of different T_rs, the spectra of the noise voltage sources are different, especially in the frequency band higher than 1 MHz. The spectrum is larger at high frequency when the rise and fall times T_r is smaller. Furthermore, the pulse width or switching frequency greatly influences the noise voltage source spectrum from (2-4). Several trapezoidal waveforms and spectra with different switching frequencies are compared in Fig. 2-8. In Fig. 2-8 (a) and (b), all waveforms have the same duty ratio but differ in frequency: F_{sw} = 20 kHz, 100 kHz, and 500 kHz. As a result, the pulse width T_w

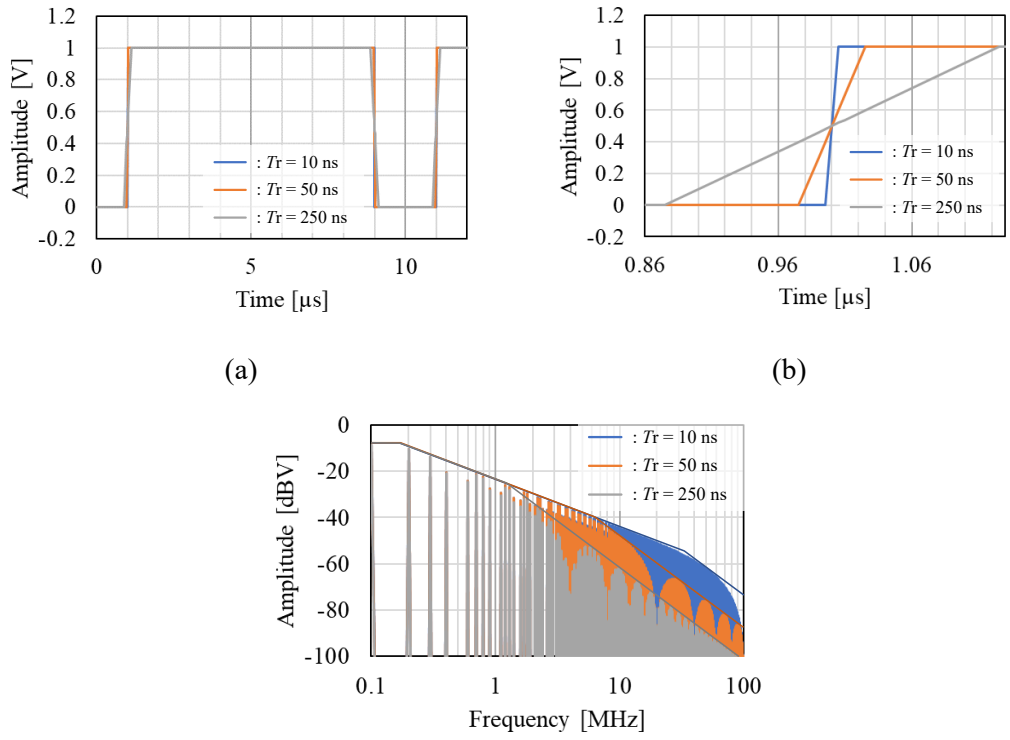
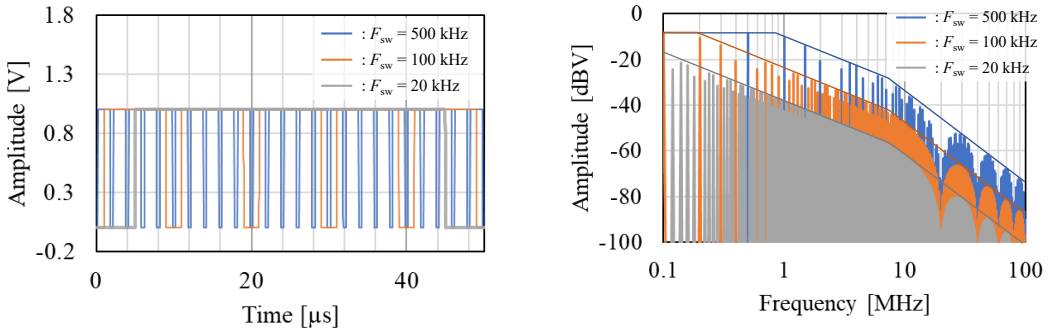


Fig. 2-7. Compared examples of noise voltage sources with different *dv*/*dt* ratio in (a) waveform, (b) enlarged wave form, and (c) spectra.

differs among all cases. The spectra in Fig. 2-8 (b) show that a noise voltage source has a larger spectrum when the switching frequency is higher. Therefore, a high dv/dt ratio and high switching frequency, often used in operating WBG devices, cause significant noise.



(a) (b)

Fig. 2-8. Compared examples of noise voltage sources with different switching frequencies in (a) waveform, (b) spectra.

2.2.2. Propagation Paths of Differential Mode and Common Mode Noise

The conductive EMI is often divided into differential mode (DM) noise and CM noise for analysis. The simplified circuit with DM and CM noise is shown in Fig. 2-9, where $V_{noise}(\omega)$ is the noise source, $Z_{L1}(\omega)$ and $Z_{L2}(\omega)$ are the impedances of power lines, $Z_{c1}(\omega)$ and $Z_{c2}(\omega)$ are the impedances between the EuT and the ground, and ω is angular noise frequency. LISN is substituted with two 50-Ω resistances at measurement terminals, and $V_1(\omega)$ and $V_2(\omega)$ are the noise terminal voltages. DM and CM noise differ in propagation paths and directions. DM noise, which is also called "normal mode noise," flows through the power lines in opposite directions. DM noise current is indicated as $I_{dm}(\omega)$ in Fig. 2-9.

By contrast, CM noise flows through a power line in the same direction and returns through the ground. CM noise current is indicated as $I_{cm}(\omega)$ in Fig. 2-9. The noise terminal voltages $V_1(\omega)$

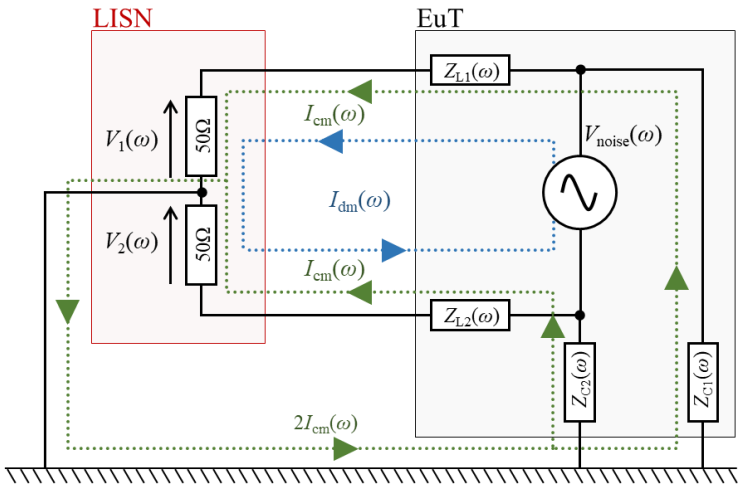


Fig. 2-9. DM noise and CM noise in a simplified circuit.

and $V_2(\omega)$ are expressed in the following equation:

$$\begin{cases} V_1(\omega) = 50\,(I_{dm}(\omega) + I_{cm}(\omega)) \\ V_2(\omega) = 50\,(I_{dm}(\omega) - I_{cm}(\omega)) \end{cases} \quad \cdots\cdots (2\text{-}5)$$

In (2-5), each noise terminal voltage consists of CM and DM noise components. Therefore, when each of the noise terminal voltage components due to CM and DM noise is defined as $V_{cm}(\omega)$ and $V_{dm}(\omega)$, respectively. $V_{cm}(\omega)$ and $V_{dm}(\omega)$ are extracted as follows:

$$\begin{cases} V_{dm}(\omega) = 50I_{dm}(\omega) = \dfrac{V_1(\omega) + V_2(\omega)}{2} \\ V_{cm}(\omega) = 50I_{cm}(\omega) = \dfrac{V_1(\omega) - V_2(\omega)}{2} \end{cases} \quad \cdots\cdots (2\text{-}6)$$

As shown in (2-6), DM and CM noise can be analyzed separately. In the actual measurement, equipment dedicated to decoupling DM and CM noise, such as CM/DM switch, is inserted between the LISN and a spectrum analyzer to extract DM and CM noise separately. Recognizing the dominating noise mode helps identify the cause of EMI and decrease EMI.

The noise countermeasures are often conducted separately to DM noise and CM noise. For example, passive EMI filters, widely used noise countermeasures, are used separately to DM and CM noise. A passive EMI filter consists of a choke coil and a capacitor.

A choke coil reduces the EMI by adding high series impedance to the propagation path. The choke coils for DM and CM noise are shown in Fig. 2-10. Each choke coil consists of a common magnetic core and two windings. Windings in the DM choke coil mutually intensify the magnetic flux when a DM noise current flows, whereas the windings mutually cancel the magnetic flux when a CM noise current flows. The magnetic flux $\Phi_{DM}(\omega)$ in Fig. 2-10 (a) corresponds to the DM noise current. Therefore, a DM choke coil becomes high impedance only to DM noise.

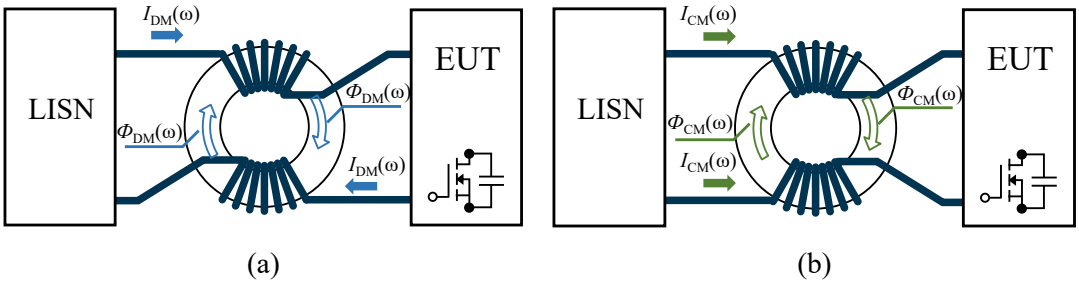


Fig. 2-10. (a) DM choke coil and (b) CM choke coil.

By contrast, windings in the CM choke coil mutually intensify the magnetic flux when a CM noise current flows, whereas the windings cancel the magnetic flux when a DM noise current flows. The magnetic flux $\Phi_{CM}(\omega)$ in Fig. 2-10 (b) corresponds to the CM noise current. Therefore, a CM choke coil becomes high impedance only to CM noise.

On the contrary, the capacitor reduces EMI by adding low parallel impedance to propagation paths. Filtering capacitors for CM and DM noise are shown in Fig. 2-11. An X capacitor is inserted between power lines to provide a low impedance loop avoiding LISN or EMI victims for a DM noise current, and Y capacitors are inserted between the power lines and the ground to provide a low impedance loop avoiding LISN or EMI victim for a CM noise current. These choke coils and capacitors multiply the noise reduction effects by combination. To take advantage of the passive EMI filters, the conducted EMI should be analyzed separately in DM

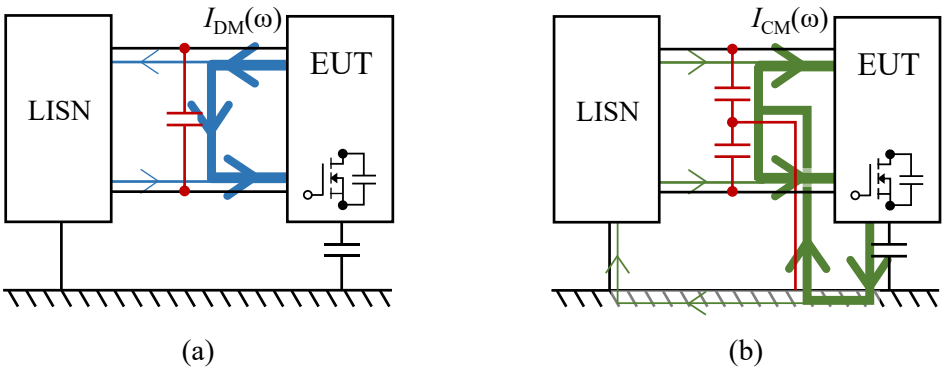


Fig. 2-11. (a) X capacitor and (b) Y capacitor.

and CM noise.

From the noise countermeasure point of view, the impedances necessary for the circuit operation such as power inductors or smoothing capacitors act as noise filters for DM noise current because DM noise current has the same path and direction as the current flowing in the main circuit. However, those impedances do not always act as noise filters for CM noise current. Additionally, the CM noise filter sometimes cannot maintain the ground quality or prevent leakage current because the CM noise propagation path includes the ground. Therefore, various CM noise reduction methods are considered in this study.

2.2.3. Measurement of Conductive EMI

LISN was introduced to measure conductive interference. The circuit diagram of LISN is shown in Fig. 2-12. In addition, the LISN inserted in the measurement system is shown in Fig. 2-13. In the actual measurement, LISN is inserted in each power line between the input power source and the EuT, as shown in Fig. 2-13. LISN provides stable impedance in the loop, including EuT. The equivalent circuits of LISN shown in Fig. 2-12, when the grid side is short and open, are shown in Fig. 2-14 (a) and (b), respectively. The impedances of LISN observed from the EuT side when the grid side is short and open are shown in Fig. 2-14 (c). The difference between the

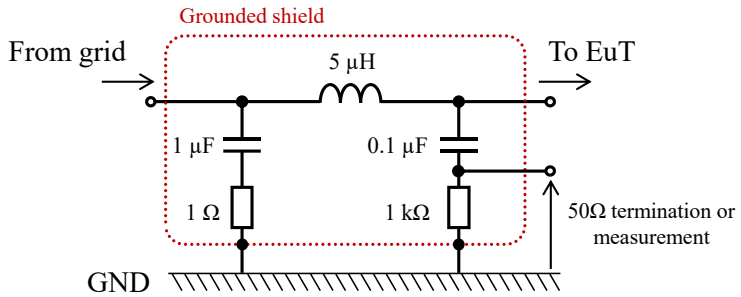


Fig. 2-12. An example of circuit diagram in the LISN.

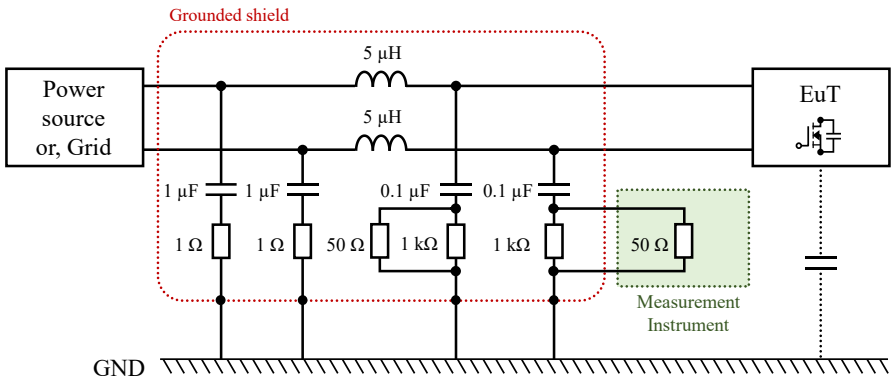
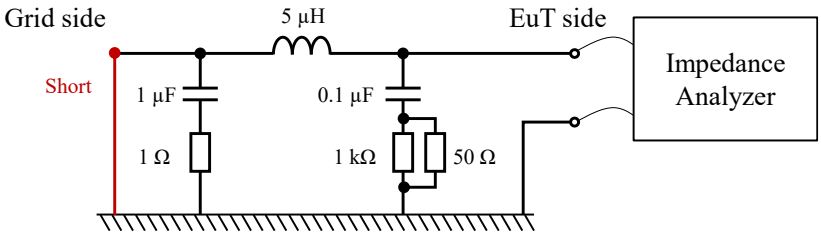
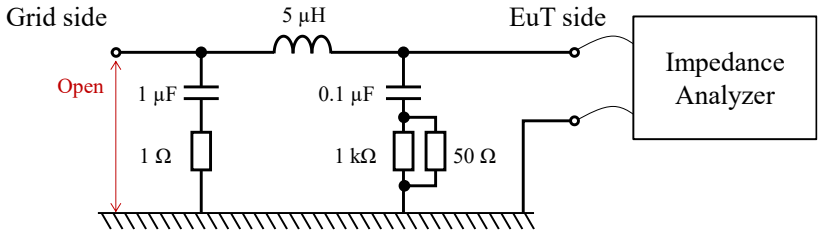


Fig. 2-13. System including the LISN.

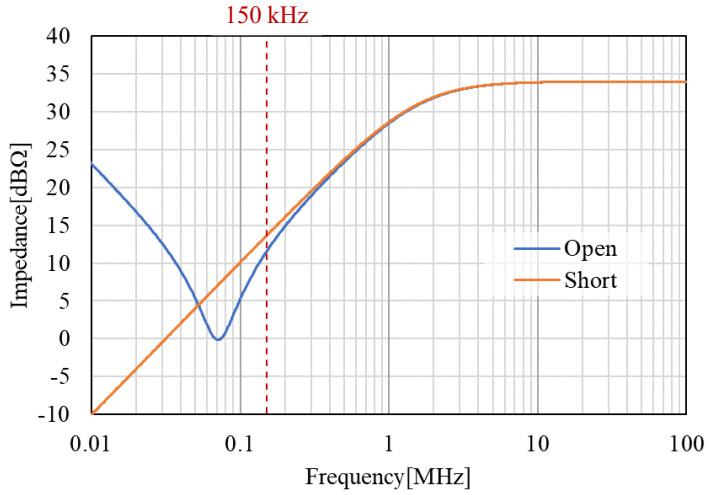
two impedance is less than 2.10 dBΩ at a frequency higher than 150 kHz, which is the bottom frequency of the conductive interference frequency band. Thus, the LISN provides stable impedance to the EuT side in the conductive interference frequency band. In addition, when observed from the grid side, the LISN also acts as a low-pass filter and eliminates the influence of the input power source or grid on the EuT. The insertion loss of LISN shown in Fig. 2-13 from the grid side to the EuT side is shown in Fig. 2-15. The insertion loss is lower than -30 dB at a frequency higher than 150 kHz. Thus, LISN prevents interference from outside of the measurement environment. With stable impedance and low-pass filter characteristics, LISN eliminates the influence from outside the system and secures the reproducibility of conductive EMI measurement.



(a)



(b)



(c)

Fig. 2-14. Equivalent circuit of LISN when grid side is (a) short and (b) open, and (c) impedances of LISN from EuT side.

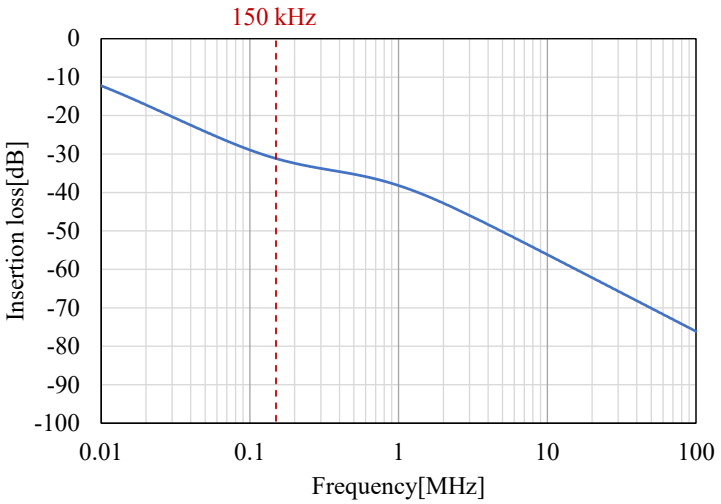


Fig. 2-15. The insertion loss of the LISN from grid side to EuT side.

CHAPTER 3: CM NOISE REDUCTION WITH AUXILIARY WINDING

3.1. Research Background

To manage large currents and improve the power density of SMPS, multi-phase circuit configurations are employed in power electronics applications[86]-[95]. For example, single-phase and three-phase boost DC–DC converter circuits are shown in Fig. 3-1 (a) and (b). Compared with a single-phase converter, a three-phase converter employs a multiple-phase structure connected in parallel to distribute the current and switching loss to multiple devices and to decrease stress on the heat radiator. Additionally, the interleaved switching operation, which is a phase-shifted operation, decreases the output current ripple and the stress on the output smoothing capacitor[84], [85]. As a result, the interleaved switching operation downsizes the output smoothing capacitor. Furthermore, the coupled inductor structure shown in Fig. 3-1 (c) can unite the magnetic

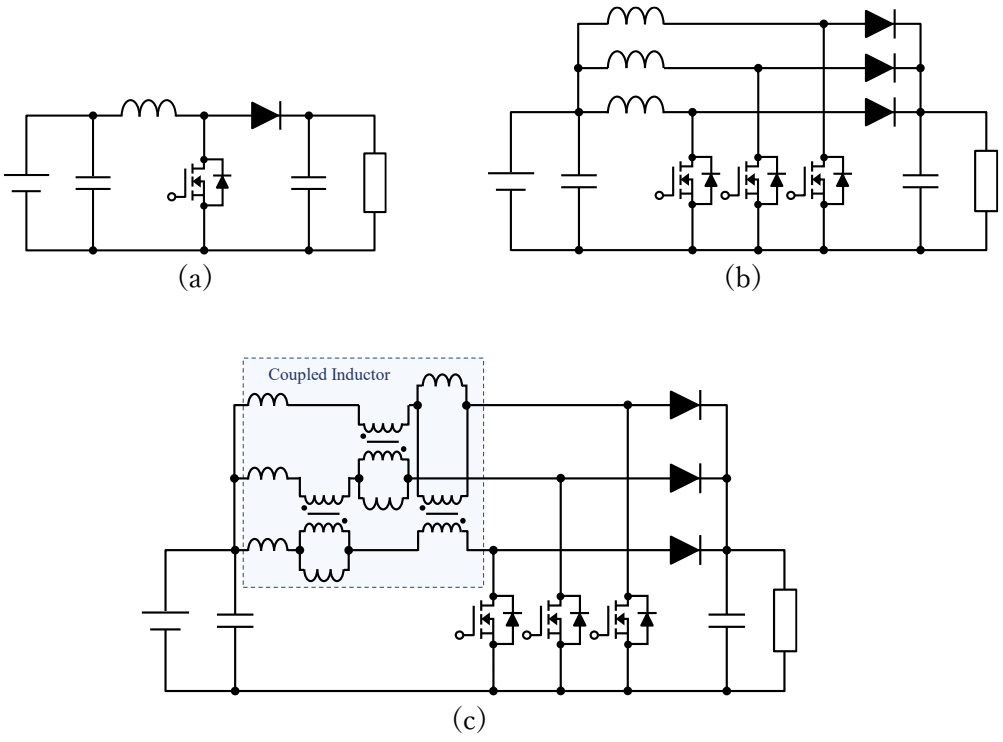


Fig. 3-1. Boost convert with (a) single-phase, (b) three-phase interleaved operation, and (c) three-phase interleaved operation and coupled inductor.

cores. The mutual induction among phases decreases the inductor current ripple and results in downsized magnetic components[86]-[91]. Consequently, a multi-phase circuit structure with an interleaved switching operation and a coupled inductor is utilized to improve the power density of SMPS, especially in large current applications such as photovoltaic energy generation systems[86], [87], [92], fuel cell systems[88], [93], and battery chargers for automobiles[94], [95].

In this chapter, an internal filter structure for a multi-phase DC–DC converter with a coupled inductor is proposed to decrease CM noise. The conventional and proposed circuits are introduced, and the CM noise is analyzed mathematically. Next, the design guideline of the proposed circuit configuration is discussed in detail. Lastly, the CM noise reduction effect of the proposed circuit is investigated in the simulation and experiment.

3.2. Conventional Circuit

3.2.1. Conventional Circuit Configuration

The conventional circuit shown in Fig. 3-2 is a two-phase interleaved boost DC–DC converter with a loosely coupled inductor. The loosely coupled inductor consists of an ideal transformer, magnetizing inductance L_{mg}, and leakage inductances L_{lk}, as shown in the circuit diagram in Fig. 3-2. A parasitic capacitance exists between the MOSFET drain terminal in each phase and the ground. In this dissertation, a parasitic capacitance between the circuit and the ground is defined as CM capacitance, and each CM capacitance corresponding to a drain terminal is defined equally as C_a from the symmetrical circuit configuration. LISN is inserted between the input voltage source and the conventional circuit, and the CM noise emitted from the circuit is evaluated using the LISN.

3.2.2. CM Noise Equivalent Circuit for Conventional Circuit

CM noise is analyzed to understand the mechanism that causes CM noise in the conventional circuit.

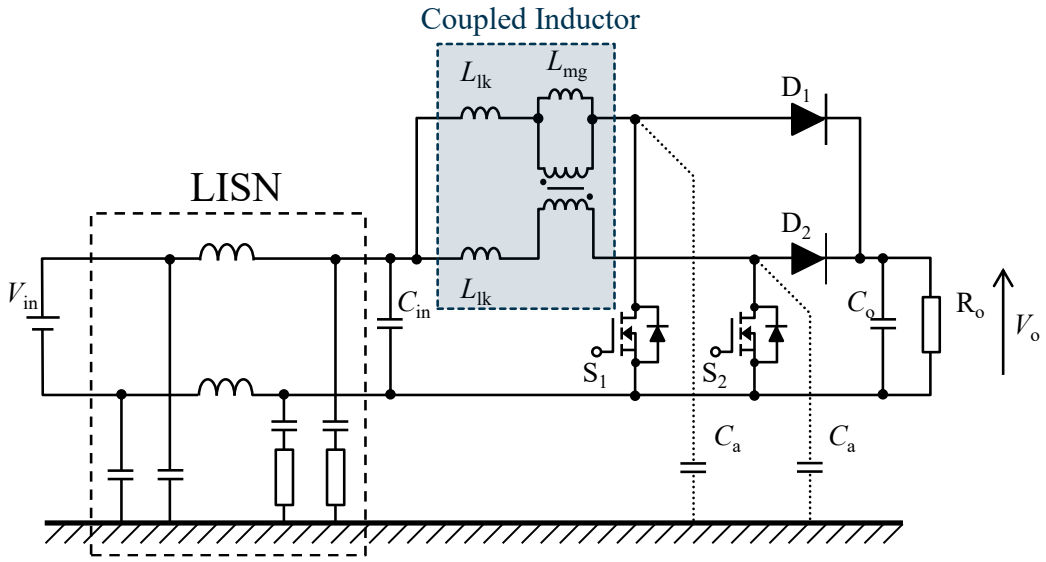
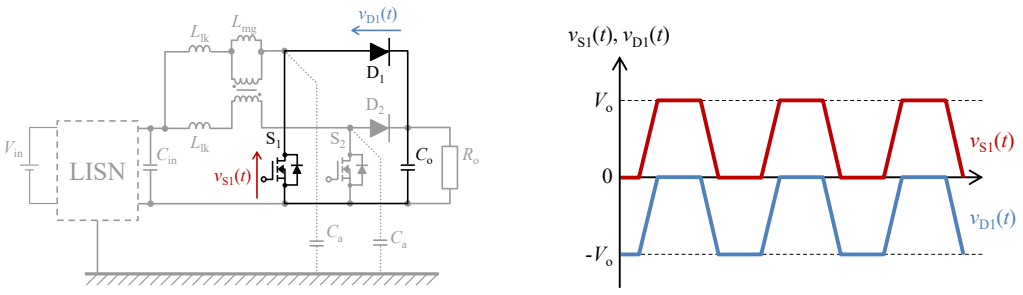


Fig. 3-2. The conventional circuit: two-phase interleaved boost DC-DC converter with a loosely coupled inductor.

As mentioned above, the switching devices become the noise source. When the voltages of S_1 and D_1 in Fig. 3-2 are defined as $v_{S1}(t)$ and $v_{D1}(t)$ shown in Fig. 3-3 (a), the waveforms become similar to those in Fig. 3-3 (b). In this case, $v_{S1}(t)$ and $v_{D1}(t)$ have the same frequency elements other than DC elements. Subsequently, the conventional circuit is converted into a CM noise equivalent circuit for CM noise analysis, which is shown in Fig. 3-4. In the CM noise equivalent circuit conversion procedure, the input and output capacitors C_{in} and C_o are assumed to be short



(a) (b)

Fig. 3-3. Voltage of S_1 and D_1 in (a) circuit diagram and (b) waveform.

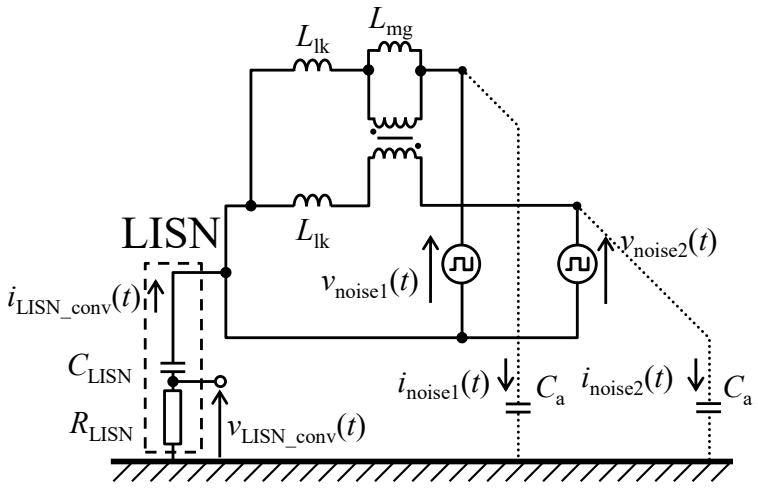


Fig. 3-4. The CM noise equivalent circuit of the conventional circuit.

in the conductive noise frequency band because the capacitances are sufficiently large. Similarly, the inductors in LISN are assumed to be open because the inductance is sufficiently large. S_1 and D_1 are connected in parallel when C_o is short, as shown in Fig. 3-3 (a). Therefore, the pair of S_1 and D_1 is substituted with a noise voltage source $v_{noise1}(t)$. Similarly, the pair of S_2 and D_2 is substituted with a noise voltage source $v_{noise2}(t)$. In the LISN, the resistive element corresponding to CM noise is expressed as R_{LISN}, and the capacitive element corresponding to CM noise is expressed as C_{LISN}. Here, the voltage drop at R_{LISN} is the CM noise terminal voltage $v_{LISN\_conv}(t)$.

Furthermore, the CM noise terminal voltage between the circuits is compared to evaluate the changes in CM noise. The simplified diagram of CM noise propagation in the conventional circuit is shown in Fig. 3-5. Because the CM noise is defined to flow through the LISN, the coupled inductor in the equivalent circuit is connected parallel to the CM noise propagation paths. Therefore, the coupled inductor is assumed to be open and ignored in CM noise analysis, as shown

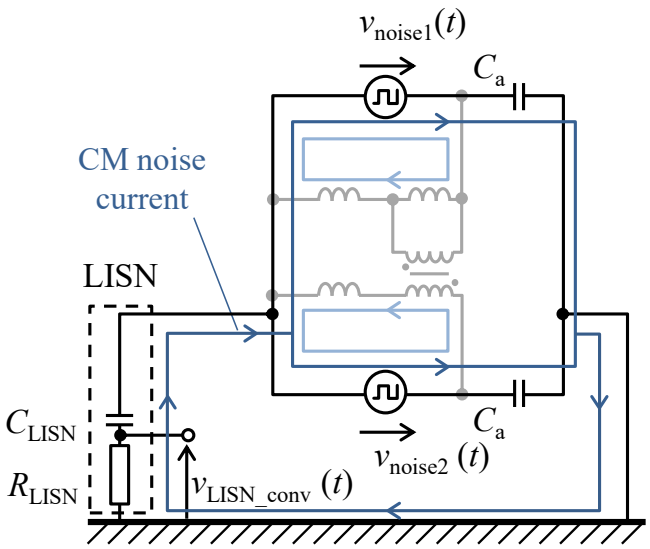


Fig. 3-5. The simplified diagram of CM noise propagation in the conventional circuit.

in Fig. 3-5. In the conventional circuit, the parasitic capacitances C_a's are charged and discharged when MOSFETs and diodes are turned on and off, and the CM noise propagates through the ground.

Here, the current flow through each CM capacitance C_a is defined as $i_{noise1}(t)$ and $i_{noise2}(t)$, respectively, and the CM noise current flowing through the LISN is defined as $i_{LISN\_conv}(t)$. Subsequently, the relationship between $i_{noise1}(t)$, $i_{noise2}(t)$, and $i_{LISN\_conv}(t)$ is expressed as follows:

$$i_{LISN\_conv}(t) = i_{noise1}(t) + i_{noise2}(t) \quad \cdots\cdots (3\text{-}1)$$

The following circuit equations are acquired from Fig. 3-4:

$$\begin{cases} V_{noise1}(\omega) = \frac{I_{noise1}(\omega)}{j\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_conv}(\omega) \\ V_{noise2}(\omega) = \frac{I_{noise2}(\omega)}{j\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_conv}(\omega) \\ V_{LISN\_conv}(\omega) = -R_{LISN} I_{LISN\_conv}(\omega) \end{cases} \quad \cdots\cdots (3\text{-}2)$$

Here, the functions $I_{noise1}(\omega)$, $I_{noise2}(\omega)$, $I_{LISN\_conv}(\omega)$, $V_{LISN\_conv}(\omega)$, $V_{noise1}(\omega)$, and $V_{noise2}(\omega)$ are obtained as the results of the Fourier transformation applied to $i_{noise1}(t)$, $i_{noise2}(t)$, $i_{LISN\_conv}(t)$, CM noise terminal voltage $v_{LISN\_conv}(t)$, and noise voltage sources $v_{noise1}(t)$ and $v_{noise2}(t)$.

Additionally, j is the imaginary unit. The noise voltage sources $v_{noise1}(t)$ and $v_{noise2}(t)$ are shifted by 180° because of the characteristics of a two-phase interleaved DC–DC converter. Therefore, the relationship between $v_{noise1}(t)$ and $v_{noise2}(t)$ is expressed as follows:

$$v_{noise2}(t) = v_{noise1}\left(t - \frac{T_{SW}}{2}\right) \cdots\cdots (3\text{-}3)$$

, where T_{sw} is the switching period. For simplification, $V_{noise}(\omega)$ is defined as follows:

$$V_{noise}(\omega) = V_{noise1}(\omega) + V_{noise2}(\omega) \cdots\cdots (3\text{-}4)$$

Furthermore, $v_{noise}(t)$ is defined as follows:

$$v_{noise}(t) = v_{noise1}(t) + v_{noise2}(t) \cdots\cdots (3\text{-}5)$$

The waveforms of $v_{noise1}(t)$, $v_{noise2}(t)$, and $v_{noise}(t)$ are compared in Fig. 3-6. In a two-phase interleaved converter, the noise voltage sources $v_{noise1}(t)$ and $v_{noise2}(t)$ have a 180° phase shift, which is T_{sw} / 2, as explained above. Subsequently, the summation of the noise voltage source

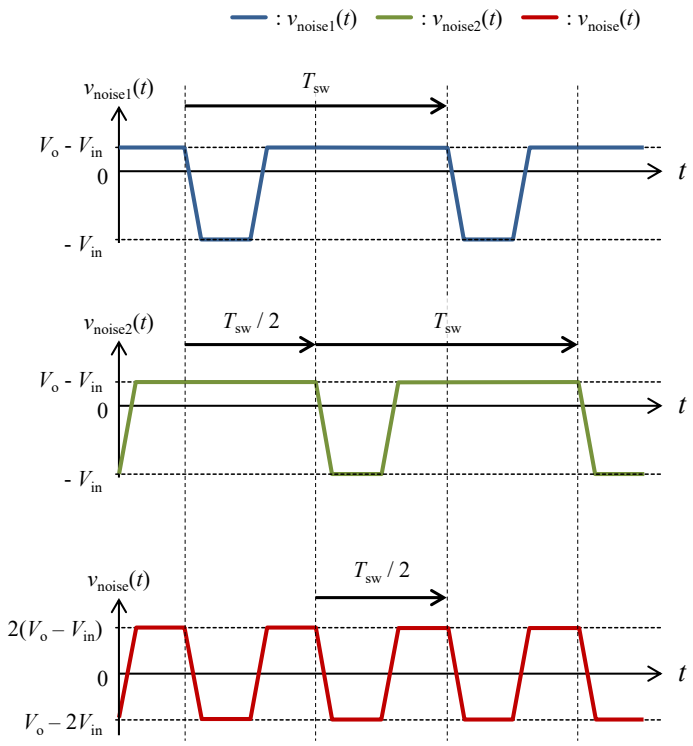


Fig. 3-6. Waveforms of $v_{noise1}(t)$, $v_{noise2}(t)$, and $v_{noise}(t)$.

$v_{noise}(t)$ has the doubled frequency of $v_{noise1}(t)$ and $v_{noise2}(t)$, as shown in Fig. 3-6. From (3-1), (3-2), and (3-4), the relationship between $V_{LISN\_conv}(\omega)$ and $V_{noise}(\omega)$ in the conventional circuit is expressed as follows:

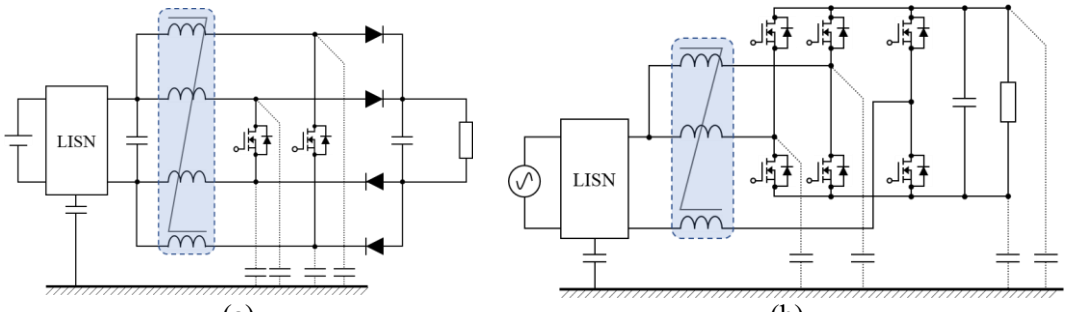
$$V_{LISN\_conv}(\omega) = \frac{-j\omega C_a C_{LISN} R_{LISN} V_{noise}(\omega)}{C_{LISN} + 2C_a(1 + j\omega C_{LISN} R_{LISN})} \quad \cdots\cdots (3\text{-}6)$$

From (3-4) and (3-6), CM noise terminal voltage $V_{LISN\_conv}(\omega)$ is proportional to $V_{noise}(\omega)$. Therefore, $V_{LISN\_conv}(\omega)$ has the doubled fundamental frequency as compared with $V_{noise1}(\omega)$ and $V_{noise2}(\omega)$. The structure of auxiliary winding to cancel the CM noise is proposed in the following section.

3.3. Proposed Circuit

As CM noise reduction methods for the multi-phase interleaved converter, [96] and [97] utilized balanced techniques. In these CM reduction methods, the impedances in the circuit are balanced among the power lines such that the CM noise currents emitting from the drain and source terminals of each MOSFET cancel each other. The proposed circuits in [96] and [97] are shown in Fig. 3-7 (a) and (b). For a balanced circuit configuration, extra diodes are required[96]. However, in [97], the distribution of the windings was adjusted and extra circuit elements were avoided, although the target circuit was a power factor correction (PFC) circuit.

Herein, the circuit configuration with an auxiliary winding is proposed as a noise



(a) (b)

Fig. 3-7. Balanced circuit configuration proposed in (a)[96] and (b)[97].

cancelation method.

3.3.1. Proposed Circuit Configuration

The circuit configuration shown in Fig. 3-8 is proposed to attenuate the CM noise in the conventional circuit. The proposed circuit has a circuit configuration added to the conventional circuit, consisting of an auxiliary winding and a capacitor C'_a, as indicated by the red line in Fig. 3-8. The auxiliary winding is magnetically coupled with each leakage inductance L_{lk}, as shown in Fig. 3-8. Here, the voltages corresponding to the coupled inductor in the proposed circuit are indicated in Fig. 3-9. The voltage corresponding to the magnetizing inductance is defined as $v_{mg}(t)$, and the voltages corresponding to the leakage inductances are defined as $v_{lk1}(t)$ and $v_{lk2}(t)$, respectively. The relationship between the noise voltage sources $v_{noise1}(t)$ and $v_{noise2}(t)$ and the voltages applied to the coupled inductor is expressed as follows:

$$\begin{cases} v_{noise1}(t) = v_{lk1}(t) + v_{mg}(t) \\ v_{noise2}(t) = v_{lk2}(t) - v_{mg}(t) \end{cases} \quad \cdots\cdots (3\text{-}7)$$

From (3-7), the total of the noise voltage sources is expressed as follows:

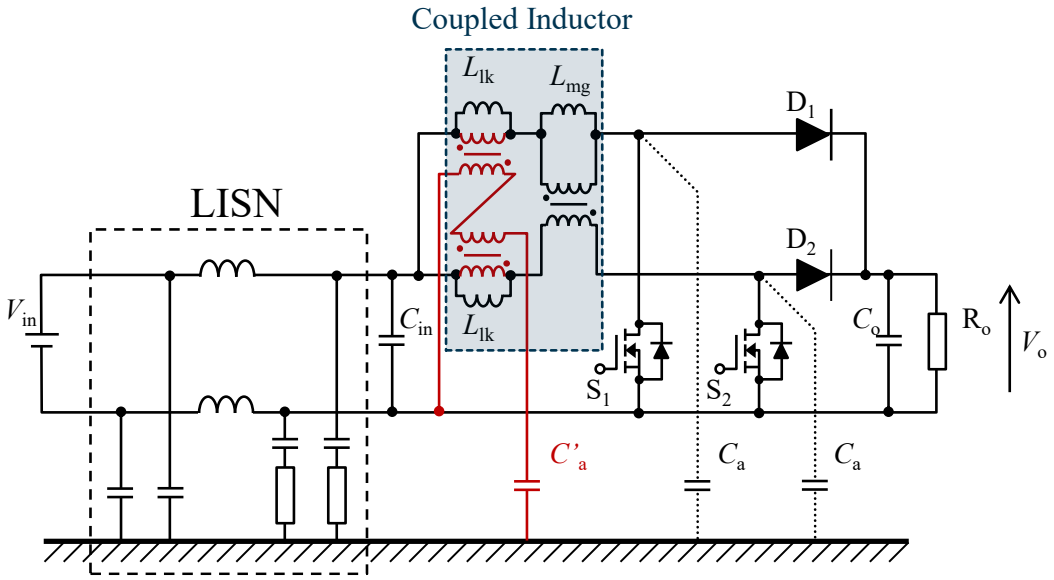


Fig. 3-8. The proposed circuit with an auxiliary winding.

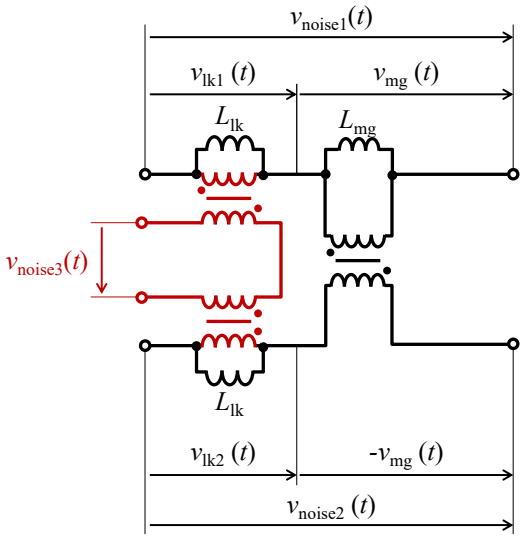


Fig. 3-9. The applied to the coupled inductor in the proposed circuit.

$$v_{noise1}(t) + v_{noise2}(t) = v_{lk1}(t) + v_{lk2}(t) \cdots\cdots (3\text{-}8)$$

As shown in (3-8), the sum of the noise voltage source is equal to the sum of voltages corresponding to the leakage inductances $v_{lk1}(t)$ and $v_{lk2}(t)$. The difference between the noise sources is expressed as follows from (3-2) and (3-7):

$$v_{noise1}(t) - v_{noise2}(t) = 2v_{mg}(t) + (v_{lk1}(t) - v_{lk2}(t)) = \frac{2}{j\omega C_a}\left(\frac{i_{noise1}(t) - i_{noise2}(t)}{2}\right) \cdots\cdots (3\text{-}9)$$

From (3-9), the $(i_{noise1}(t) - i_{noise2}(t)) / 2$ is the noise current that originates from the noise voltage source $2v_{mg}(t) + (v_{lk1}(t) - v_{lk2}(t))$. The noise current path of the $(i_{noise1}(t) - i_{noise2}(t)) / 2$ in the CM noise equivalent circuit of the conventional circuit is shown in Fig. 3-10. The noise current $(i_{noise1}(t) - i_{noise2}(t)) / 2$ emits from $v_{noise1}(t)$ to the ground through the CM capacitance C_a and flows back to the $v_{noise2}(t)$ through the other CM capacitance C_a, as shown in Fig. 3-10. Therefore, the current $(i_{noise1}(t) - i_{noise2}(t)) / 2$ is the noise current that emits to the ground but does not flow through the LISN. Therefore, the noise current $(i_{noise1}(t) - i_{noise2}(t)) / 2$, which originates from the sum of voltages corresponding to the magnetizing inductance $2v_{mg}(t)$ and the difference in voltages corresponding to the leakage inductances $v_{lk1}(t) - v_{lk2}(t)$, is already canceled in the

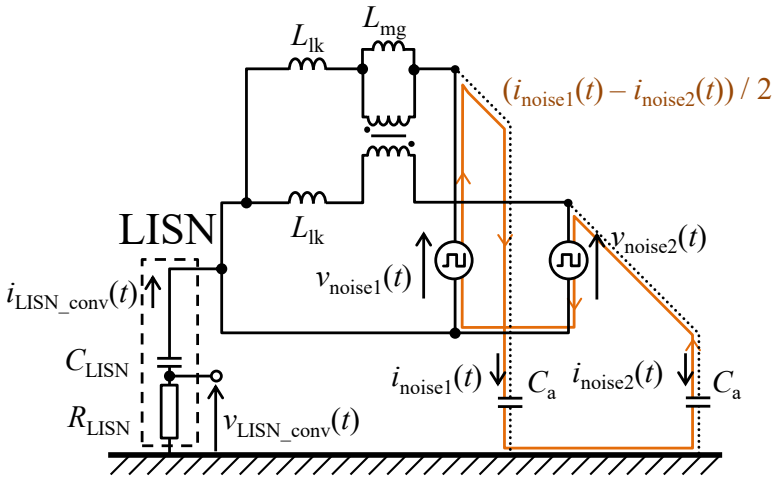


Fig. 3-10. The noise current path of $(i_{noise1}(t) - i_{noise2}(t)) / 2$.

conventional circuit and is not necessarily dealt with in the proposed circuit. The noise current generated in the conventional circuit originates from the total voltage of $v_{lk1}(t)$ and $v_{lk2}(t)$. Therefore, the auxiliary winding coupled only with the leakage inductances L_{lk}s achieves CM noise canceling in the proposed circuit, as shown in Fig. 3-8.

The voltage applied to the auxiliary winding $v_{noise3}(t)$ is expressed as follows:

$$v_{noise3}(t) = -n(v_{lk1}(t) + v_{lk2}(t)) = -n(v_{noise1}(t) + v_{noise2}(t)) \quad \cdots\cdots (3\text{-}10)$$

, where n indicates the turn ratio of the auxiliary winding to the main windings. From (3-10), $v_{noise3}(t)$ is n times larger than $v_{noise1}(t) + v_{noise2}(t)$ and is in a reversed phase. The proposed circuit reduces the CM noise by canceling the noise current by utilizing the reversed phase noise voltage source $v_{noise3}(t)$. The CM noise reduction in the proposed circuit is analyzed mathematically in the subsequent section.

3.3.2. CM Noise Equivalent Circuit for the Proposed Circuit

In this section, the proposed circuit configuration is converted into the CM noise equivalent circuit to understand the CM noise reduction mechanism and establish the design guidelines for auxiliary winding.

The CM noise equivalent circuit of the proposed circuit is shown in Fig. 3-11. The noise voltage source $v_{noise3}(t)$ expressed in (3-10) generates a canceling current $i_{noise3}(t)$. The CM noise terminal voltage in the proposed circuits is defined as $v_{LISN\_prop}(t)$, and the CM noise current flowing through the LISN is defined as $i_{LISN\_prop}(t)$.

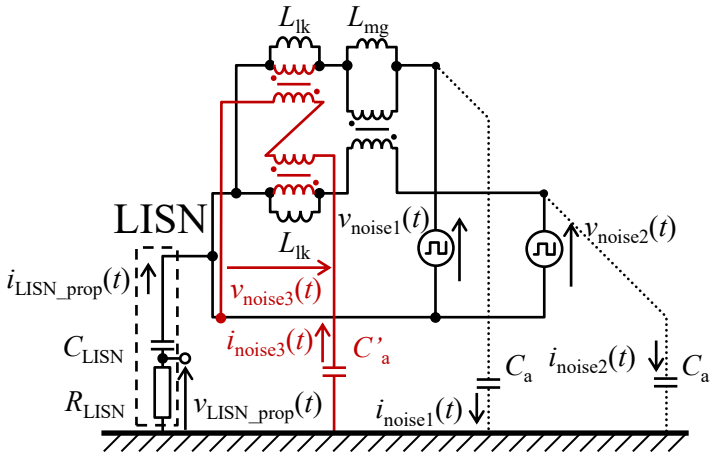


Fig. 3-11. The CM noise equivalent circuit of the proposed circuit.

A simplified diagram of CM noise cancellation in the proposed circuit is shown in Fig. 3-12. The auxiliary winding is substituted with the noise voltage source $v_{noise3}(t)$. The main windings are assumed to be open and ignored in Fig. 3-12 and Fig. 3-5. The CM noise propagates through the ground in the proposed circuit simultaneously with the charge and discharge of C_as, as in the conventional circuit. However, the canceling current flows through the auxiliary winding, as explained in the previous section. The amplitude of the canceling current is adjustable by the turns ratio n and the CM capacitance C'_a connected to the auxiliary winding in series. The CM noise is canceled when the CM noise current flowing through C_as and canceling current flowing through C'_a have the same amplitude but the reversed phase to each other.

CM noise in the proposed circuit is analyzed to establish the design guidelines for CM noise cancellation. The relationship between $i_{LISN\_prop}(t)$, $i_{noise1}(t)$, $i_{noise2}(t)$, and $i_{noise3}(t)$ is expressed

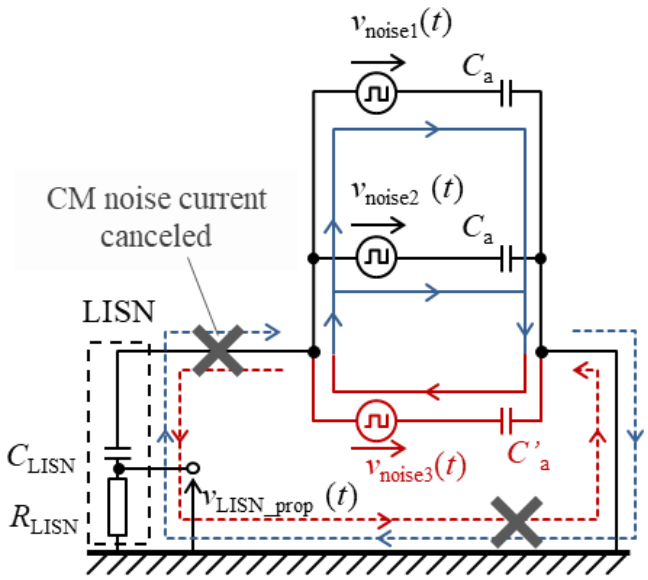


Fig. 3-12. The simplified diagram of the CM noise cancellation in the proposed circuit.

as follows:

$$i_{LISN\_prop}(t) = i_{noise1}(t) + i_{noise2}(t) - i_{noise3}(t) \quad \cdots\cdots (3\text{-}11)$$

The following circuit equations are acquired from Fig. 3-11:

$$\begin{cases} V_{noise1}(\omega) = \frac{I_{noise1}(\omega)}{j\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_prop}(\omega) \\ V_{noise2}(\omega) = \frac{I_{noise2}(\omega)}{j\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_prop}(\omega) \\ V_{noise3}(\omega) = -\frac{I_{noise3}(\omega)}{jm\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_prop}(\omega) \\ V_{LISN\_prop}(\omega) = -R_{LISN} I_{LISN\_prop}(\omega) \end{cases} \quad \cdots\cdots (3\text{-}12)$$

Here, the functions $I_{noise3}(\omega)$, $I_{LISN\_prop}(\omega)$, $V_{noise3}(\omega)$, and $V_{LISN\_prop}(\omega)$ are obtained as the results of the Fourier transformation applied to $i_{noise3}(t)$, $i_{LISN\_prop}(t)$, $v_{noise3}(t)$ and $v_{LISN\_prop}(t)$. From (3-4) and (3-10), $V_{noise3}(\omega)$ is expressed as follows.

$$V_{noise3}(\omega) = -n(V_{noise1}(\omega) + V_{noise2}(\omega)) = -nV_{noise}(\omega) \quad \cdots\cdots (3\text{-}13)$$

, where m is the capacitance ratio of C'_a to C_a and $m = C'_a / C_a$. From (3-11), (3-12), and (3-13), the relationship between $V_{noise3}(\omega)$ and $V_{LISN\_prop}(\omega)$ is expressed as follows:

$$V_{LISN\_prop}(\omega) = \frac{j\omega C_a C_{LISN} R_{LISN}(mn-1) V_{noise}(\omega)}{C_{LISN} + C_a(2+m)(1+j\omega C_{LISN} R_{LISN})} \quad \cdots\cdots (3\text{-}14)$$

From (3-6) and (3-14), the CM noise terminal voltage ratio between the proposed and conventional circuits is expressed as follows:

$$\frac{V_{\mathrm{LISN\_prop}}(\omega)}{V_{\mathrm{LISN\_conv}}(\omega)} = \frac{(1-mn)\left(C_{\mathrm{LISN}}+2C_{\mathrm{a}}(1+j\omega C_{\mathrm{LISN}}R_{\mathrm{LISN}})\right)}{C_{\mathrm{LISN}}+C_{\mathrm{a}}(2+m)(1+j\omega C_{\mathrm{LISN}}R_{\mathrm{LISN}})} \quad \text{(3-15)}$$

$V_{\mathrm{LISN\_prop}}(\omega)$ / $V_{\mathrm{LISN\_conv}}(\omega)$ indicates the change in CM noise between the proposed and conventional circuits, and $G_{\mathrm{noise12}}(\omega)$ in the following equation is introduced to evaluate the CM noise change in dB:

$$G_{\mathrm{noise12}}(\omega) = 20\log_{10}\left|\frac{V_{\mathrm{LISN\_prop}}(\omega)}{V_{\mathrm{LISN\_conv}}(\omega)}\right| \quad \text{(3-16)}$$

$G_{\mathrm{noise12}}(\omega)$ is negative when the CM noise in the proposed circuit decreases and positive when the CM noise in the proposed circuit increases. In Fig. 3-13, $G_{\mathrm{noise12}}(\omega)$ is indicated in the contour graph in which the vertical axis indicates the capacitance ratio m and the horizontal axis indicates the turns ratio n. From (3-15) and (3-16) and Fig. 3-13, it can be observed that the CM noise terminal voltage is 0 V when $mn = 0$. However, the CM noise reduction effect weakens as mn

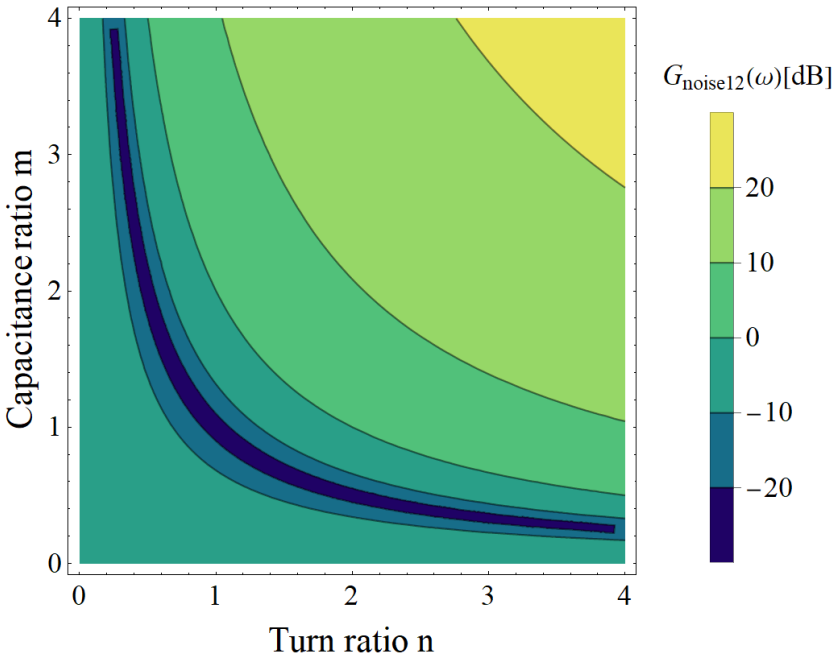


Fig. 3-13. Dependence of $G_{\mathrm{noise12}}(\omega)$ on n and m in (3-16).

departs from 1. However, when $mn > 2$, the CM noise in the proposed circuit increases. Therefore, the auxiliary winding and capacitor C'_a should be designed to achieve $mn = 1$ to maximize the CM noise reduction effect.

3.4. CM Noise Analysis Considering the Leakage Inductance of Auxiliary Winding

3.4.1. Leakage Inductance of Auxiliary Winding

In the previous section, the coupling coefficient between the auxiliary winding and the main windings was assumed to be 1 to simplify the problem for understanding the mechanism of CM noise reduction and clarifying the design guidelines. However, the coupling coefficient in the actual application is less than 1. In addition, parasitic components greatly influence the noise analysis in a broad bandwidth. Consequently, leakage inductance is considered. Therefore, a more practical CM noise analysis considering the frequency characteristics is conducted by considering the leakage inductance of the auxiliary winding. However, the parasitic capacitance and resistance of the auxiliary winding and parasitic inductance and resistance of the capacitance C'_a are assumed to be sufficiently small and ignored.

3.4.2. CM Noise Equivalent Circuit Considering the Leakage Inductance L_{lk3}

The leakage inductance of magnetic coupling between the auxiliary winding and L_{lk}s observed from the auxiliary winding side is defined as L_{lk3}. The CM noise equivalent circuit L_{lk} added to the circuit in Fig. 3-11 is shown in Fig. 3-14. The auxiliary winding consists of ideal transformers and L_{lk3}, and the CM noise terminal voltage in Fig. 3-14 is $v_{LISN\_prop\_lk}(t)$. The function obtained from the Fourier transformation applied to $v_{LISN\_prop\_lk}(t)$ is $V_{LISN\_prop\_lk}(\omega)$. The following circuit equations are obtained from Fig. 3-14:

$$\begin{cases} V_{noise1}(\omega) = \frac{I_{noise1}(\omega)}{j\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_prop}(\omega) \\ V_{noise2}(\omega) = \frac{I_{noise2}(\omega)}{j\omega C_a} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_prop}(\omega) \\ V_{noise3}(\omega) = -\left(\frac{1}{jm\omega C_a} + j\omega L_{lk3}\right) I_{noise3}(\omega) + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN\_prop}(\omega) \\ V_{LISN\_prop\_lk}(\omega) = -R_{LISN} I_{LISN\_prop}(\omega) \end{cases} \quad \cdots\cdots\cdots\cdots\cdots (3\text{-}17)$$

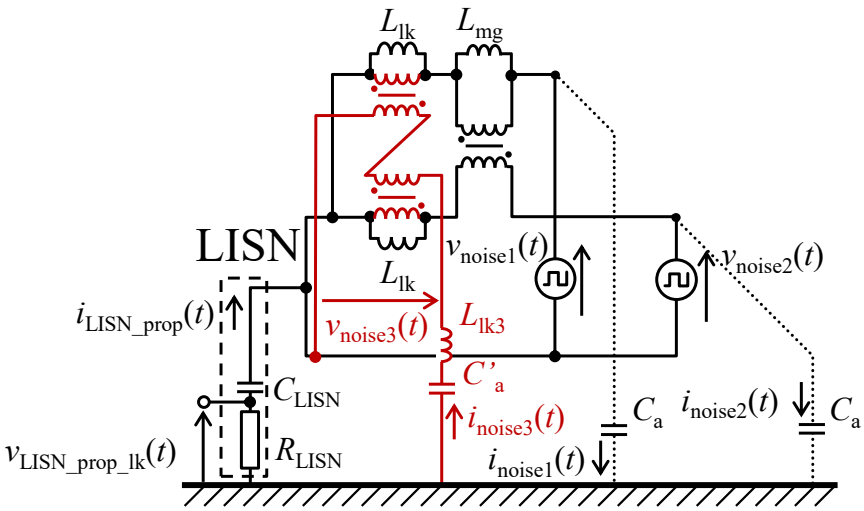


Fig. 3-14. CM noise equivalent circuit of proposed circuit with L_{lk3}.

From (3-11), (3-13), and (3-17), CM noise terminal voltage $V_{LISN\_prop\_lk}(\omega)$ is expressed as follows:

$$V_{LISN\_prop\_lk}(\omega) = \frac{j\omega C_a C_{LISN} R_{LISN}(mn - 1 + m\omega^2 L_{lk3} C_a) V_{noise}(\omega)}{mC_a(1 + j\omega C_{LISN} R_{LISN}) + (1 - m\omega^2 L_{lk3} C_a)(C_{LISN} + 2C_a(1 + j\omega C_{LISN} R_{LISN}))} \quad \cdots\cdots (3\text{-}18)$$

In addition, the ratio of the CM noise terminal voltage in the proposed circuit to that in the conventional circuit is expressed as follows when L_{lk3} is considered:

$$\frac{V_{LISN\_prop\_lk}(\omega)}{V_{LISN\_conv}(\omega)} = \frac{(1 - mn - m\omega^2 L_{lk3} C_a)(C_{LISN} + 2C_a(1 + j\omega C_{LISN} R_{LISN}))}{mC_a(1 + j\omega C_{LISN} R_{LISN}) + (1 - m\omega^2 L_{lk3} C_a)(C_{LISN} + 2C_a(1 + j\omega C_{LISN} R_{LISN}))} \quad \cdots\cdots (3\text{-}19)$$

Furthermore, (3-19) includes L_{lk3}, and L_{lk3} influences the CM noise reduction effect of the proposed circuit. Therefore, $G_{noise13}(\omega)$ is defined similarly to (3-15) for evaluation as follows:

$$G_{noise13}(\omega) = 20\log_{10}\left|\frac{V_{LISN\_prop\_lk}(\omega)}{V_{LISN\_conv}(\omega)}\right| \quad \cdots\cdots (3\text{-}20)$$

The CM noise reduction effect is evaluated with $G_{noise13}(\omega)$ when L_{lk3} is considered.

3.4.3. Design of *n* Considering the Leakage Inductance L_{lk3}

As explained in the previous section, L_{lk3} influences the CM noise reduction effect of the proposed circuit. In this section, the value of n that maximizes the CM noise reduction effect of the proposed circuit is investigated when L_{lk3} is considered. The frequency characteristics of $G_{noise13}(\omega)$ calculated with various values of n are shown in Fig. 3-15. The coupling coefficient of

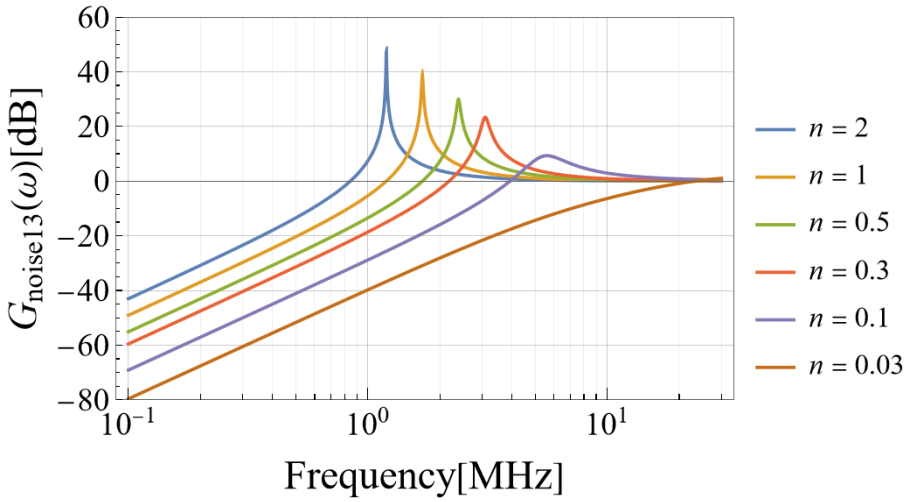


Fig. 3-15. Calculated $G_{noise13}(\omega)$ with various values of n.

the auxiliary winding is defined as k_3 when the graphs in Fig. 3-15 are derived. The number of turns of the main windings and the coupling coefficient k_3 is assumed to be constant. Subsequently, the value of L_{lk3} is proportional to (1 - k_3) and to the number of turns of the auxiliary winding. Therefore, L_{lk3} is defined as follows in the calculation:

$$L_{lk3} = (1 - k_3)n^2 l_3 \quad \cdots\cdots (3\text{-}21)$$

, where l_3 is the coefficient decided by the structure of the auxiliary winding; in this case, l_3 is the self-inductance of the auxiliary winding when n = 1. In addition, the value of C'_a is set to achieve mn = 1 following the design guidelines discussed in Section 3.3.2. The parameters used for the calculation are shown in Table 3-1.

Table 3-1. Circuit parameter for calculation.

Definition	Symbol	Value
Parasitic capacitance	C_a [F]	4.22×10^{-11}
Capacitance of LISN	C_{LISN}[F]	2.00×10^{-7}
Resistance of LISN	R_{LISN}[Ω]	2.50×10^{1}
Coupling coefficient	k_3	3.00×10^{-1}
Aux. inductance coefficient	l_3[H]	3.00×10^{-4}

As shown in Fig. 3-15, $G_{noise13}(\omega)$ is negative when the CM noise decreases and positive when the CM noise increases in the proposed circuit. The frequency characteristics of $G_{noise13}(\omega)$ differ when the values of n differ. The canceling current path, including L_{lk3}, is shown in Fig. 3-16 to understand the influence of the turns ratio n on the CM noise. In Fig. 3-16, C_{LISN} is ignored because $C_{LISN} >> C'_a$. In the loop, the reversed phase voltage source $v_{noise3}(t)$, L_{lk3}, C'_a, and R_{LISN} exist in series. The impedance of the canceling current path $Z_{cancel}(\omega)$ is expressed as follows:

$$Z_{cancel}(\omega) = R_{LISN} + j\omega L_{lk3} + \frac{1}{j\omega C'_a} \quad \cdots\cdots (3\text{-}22)$$

From (3-15), the CM noise is canceled when L_{lk3} is ignorable. Therefore, CM noise decreases in the proposed circuit when $j\omega L_{lk3} << 1 / j\omega C'_a$. However, L_{lk3} and C'_a are connected in series in the canceling current loop. Therefore, $Z_{cancel}(\omega)$ can be too small because of the series resonance between L_{lk3} and C'_a at the resonant frequency $\omega_r = \sqrt{1/L_{lk3}C'_a}$. Hence, excessive canceling current can increase the CM noise in the proposed circuit.

However, the CM noise in the proposed circuit does not increase when $G_{noise13}(\omega_r) \leq 0$ at $\omega_r = \sqrt{1/L_{lk3}C'_a}$. From (3-19), the condition in which $G_{noise13}(\omega_r) \leq 0$ at $\omega_r = \sqrt{1/L_{lk3}C'_a}$, when

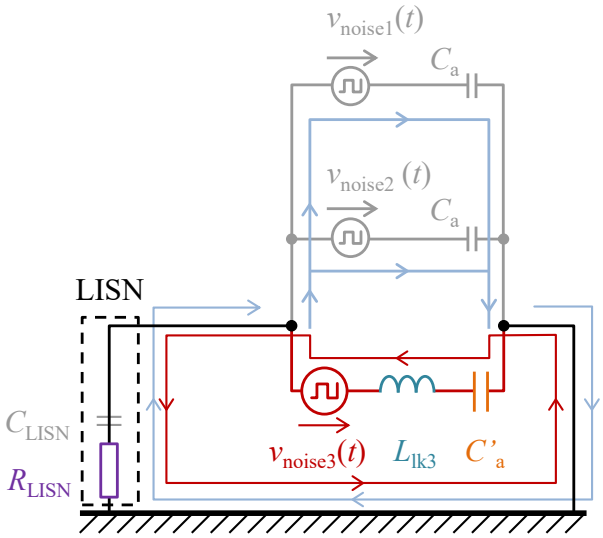


Fig. 3-16. Canceling current path including L_{lk3}.

$mn = 1$ is expressed as follows:

$$\left|\frac{C_{\mathrm{LISN}} + 2C_{\mathrm{a}}(1 + j\omega_{\mathrm{r}}C_{\mathrm{LISN}}R_{\mathrm{LISN}})}{mC_{\mathrm{a}}(1 + j\omega_{\mathrm{r}}C_{\mathrm{LISN}}R_{\mathrm{LISN}})}\right| \leq 1 \quad \cdots\cdots (3\text{-}23)$$

When $\omega_{\mathrm{r}} \gg 1/C_{\mathrm{LISN}}R_{\mathrm{LISN}}$, (3-23) is converted as follows:

$$\left|\frac{1 + 2j\omega_{\mathrm{r}}C_{\mathrm{a}}R_{\mathrm{LISN}}}{mj\omega_{\mathrm{r}}C_{\mathrm{a}}R_{\mathrm{LISN}}}\right| \leq 1 \quad \cdots\cdots (3\text{-}24)$$

The following relation always holds on the left-hand side of (3-24):

$$\left|\frac{1 + 2j\omega_{\mathrm{r}}C_{\mathrm{a}}R_{\mathrm{LISN}}}{mj\omega_{\mathrm{r}}C_{\mathrm{a}}R_{\mathrm{LISN}}}\right| > \frac{2}{m} \quad \cdots\cdots (3\text{-}25)$$

Therefore, at least, m should be larger than 2 to meet (3-24). When $1 << 2\omega_{\mathrm{r}}C_{\mathrm{LISN}}R_{\mathrm{LISN}}$ and $m > 2$, (3-24) is consistently met. However, the following equation should be satisfied to meet (3-24) when $1 >> 2\omega_{\mathrm{r}}C_{\mathrm{LISN}}R_{\mathrm{LISN}}$:

$$\left|\frac{1}{mj\omega_{\mathrm{r}}C_{\mathrm{a}}R_{\mathrm{LISN}}}\right| \leq 1 \quad \cdots\cdots (3\text{-}26)$$

Subsequently, (3-26) is converted as follows:

$$R_{\mathrm{LISN}} \geq \sqrt{\frac{L_{\mathrm{lk3}}}{C'_{\mathrm{a}}}} \quad \cdots\cdots (3\text{-}27)$$

Consequently, the CM noise in the proposed circuit does not increase when $m > 2$ and $R_{\mathrm{LISN}} \geq \sqrt{L_{\mathrm{lk3}}/C'_{\mathrm{a}}}$. Here, the resonant frequency ω_{r} should meet $\omega_{\mathrm{r}} \gg 1/C_{\mathrm{LISN}}R_{\mathrm{LISN}}$. For example, $1 / 2\pi C_{\mathrm{LISN}}R_{\mathrm{LISN}} = 31.8$ [kHz] based on the parameters listed in Table 3-1. To meet both the conditions of $m > 2$ and $R_{\mathrm{LISN}} \geq \sqrt{L_{\mathrm{lk3}}/C'_{\mathrm{a}}}$, n should be designed to be minimum.

The relationship between the frequency characteristics of CM noise and the impedance of the canceling current path is explained in detail below. The example frequency characteristics of $Z_{\mathrm{cancel}}(\omega)$ are shown in Fig. 3-17 (a) and (b). Considering that the CM noise decreases when $Z_{\mathrm{cancel}}(\omega) \approx 1 / j\omega C'_{\mathrm{a}}$, the frequency characteristic of $Z_{\mathrm{cancel}}(\omega)$ in Fig. 3-17 (a), in which $R_{\mathrm{LISN}} < \sqrt{L_{\mathrm{lk3}}/C'_{\mathrm{a}}}$, is divided into the following three frequency regions:

(i) This is the frequency band in which $Z_{\mathrm{cancel}}(\omega) \approx 1 / j\omega C'_{\mathrm{a}}$. The CM noise decreases in this

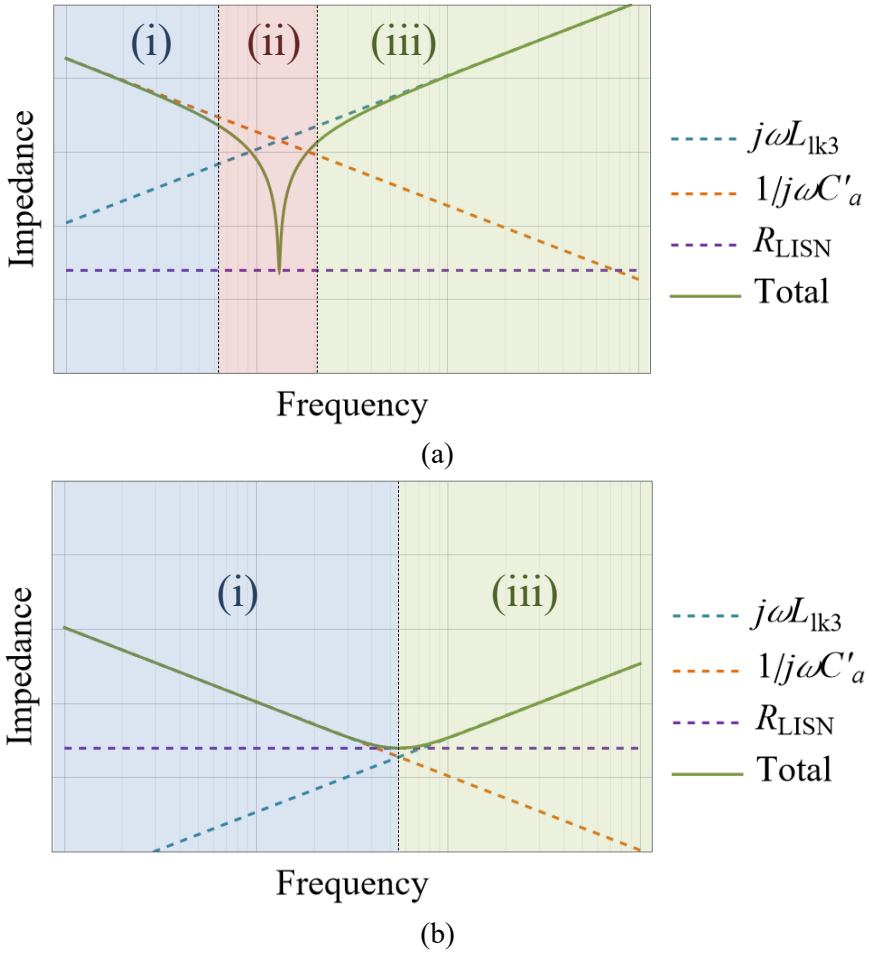


Fig. 3-17. Frequency characteristics of $Z_{cancel}(\omega)$ when (a) $R_{LISN} < \sqrt{L_{lk3}/C'_a}$ and (b) $R_{LISN} > \sqrt{L_{lk3}/C'_a}$.

frequency band because the capacitance C'_a is dominant in the noise propagation path.

(ii) This is the frequency band in which $Z_{cancel}(\omega)$ becomes extremely small because of the series resonance between L_{lk3} and C'_a. As a result, the excessive canceling current flows around the resonant frequency, and the CM noise increases because $|Z_{cancel}(\omega)| << |1 / j\omega C'_a|$.

(iii) This is the frequency band in which $Z_{cancel}(\omega) \approx j\omega L_{lk3}$. The phase of the canceling current is reversed from ideal because $Z_{cancel}(\omega) \approx j\omega L_{lk3}$; therefore, the CM noise increases. However, the amplitude of the canceling current is minimal because $|j\omega L_{lk3}| >> |1 / j\omega C'_a|$, and $Z_{cancel}(\omega)$ is significantly larger than the ideal impedance. Consequently, the CM noise increases

minimally and close to those values in the proposed and conventional circuits.

For example, $\sqrt{L_{lk3}/C'_a} = 789$ [Ω] when $n = 0.5$ from (3-21) and Table 3-1, whereas $R_{LISN} = 25$ Ω. Therefore, $R_{LISN} < \sqrt{L_{lk3}/C'_a}$ when $n = 0.5$. In Fig. 3-15, the CM noise is canceled at the frequency of less than 1 MHz but increases around 2.39 MHz, which is the resonant frequency of L_{lk3} and C'_a when $n = 0.5$. The CM noise undergoes minimal changes at a frequency of more than 4 MHz. These characteristics match the above explanations in (i) to (iii).

However, the CM noise in the proposed circuit does not increase when $R_{LISN} \geq \sqrt{L_{lk3}/C'_a}$, as in Fig. 3-17 (b), because $|Z_{cancel}(\omega)| \geq |1 / j\omega C'_a|$ at any frequency and $Z_{cancel}(\omega)$ does not meet the condition that $|Z_{cancel}(\omega)| < |1 / j\omega C'_a|$ at any frequency. For example, $\sqrt{L_{lk3}/C'_a} = 11.6$[Ω] when n = 0.03 from (3-21) and Table 3-1. Therefore, $R_{LISN} \geq \sqrt{L_{lk3}/C'_a}$ when $n = 0.03$. In Fig. 3-15, the CM noise is canceled at a frequency of less than 10 MHz and undergoes minimal changes at a frequency of more than 10 MHz when $n = 0.03$. By contrast, the CM noise does not increase around 9.76 MHz, which is the resonant frequency of L_{lk3} and C'_a. These characteristics only match the above explanations in (i) and (iii).

Consequently, the CM noise does not decrease in the frequency region (iii) and increases in the frequency region (ii) when L_{lk3} is considered. However, the minimum n value minimizes the increase in CM noise in the frequency region (ii). In addition, based on Fig. 3-15 and the above explanation in (i) to (iii), the frequency region (i), in which the CM noise in the proposed circuit decreases, is limited by the resonant frequency ω_r. Therefore, the CM noise reduction effect is improved when ω_r is increased. Thus, the minimum n value maximizes the CM noise reduction effect in the frequency region (i).

3.4.4. Influence of the *mn* Error on CM Noise

In Section 3.3, the design guidelines for the auxiliary winding and the capacitance C'_a meeting $mn = 1$ are established. However, implementing the proposed circuit with high accuracy

of mn is difficult because of errors such as the manufacturing error of C'_a. Therefore, the influence of error in mn on the CM noise reduction effect is discussed in this section. The error in mn is defined as e_{mn}, which is expressed as follows:

$$e_{mn} = mn - 1 \quad \cdots\cdots (3\text{-}28)$$

The frequency characteristics of $G_{noise13}(\omega)$ with various values of e_{mn} are shown in Fig. 3-18, where n = 0.03 and L_{lk3} is calculated from (3-21) and Table 3-1. In Fig. 3-18, $G_{noise13}(\omega)$ is 40 dB/dec under 0 dB when $e_{mn} = 0$. However, $G_{noise13}(\omega)$ has an asymptote $G_{noise13}(\omega) = 20\log_{10}|e_{mn}|$ that becomes the lower limit when $e_{mn} > 0$. This asymptote is acquired from the following approximation derived from (3-19) when ω is sufficiently small:

$$\left|\frac{V_{LISN\_prop\_lk}(\omega)}{V_{LISN\_conv}(\omega)}\right| \approx \left| e_{mn} + m\omega^2 L_{lk3} C_a \right| \quad \cdots\cdots (3\text{-}29)$$

However, in the case where $e_{mn} < 0$, $G_{noise13}(\omega)$ has a local minimum when ω meets $e_{mn} = -m\omega^2 L_{lk3} C'_a$ from (3-29). When $e_{mn} < 0$, $G_{noise13}(\omega)$ also has an asymptote $G_{noise13}(\omega) = 20\log_{10}|e_{mn}|$.

Consequently, the CM noise decreases on a larger scale at a lower frequency when mn = 1; however, practically $G_{noise13}(\omega)$ has a lower limit depending on e_{mn} when e_{mn} is considered.

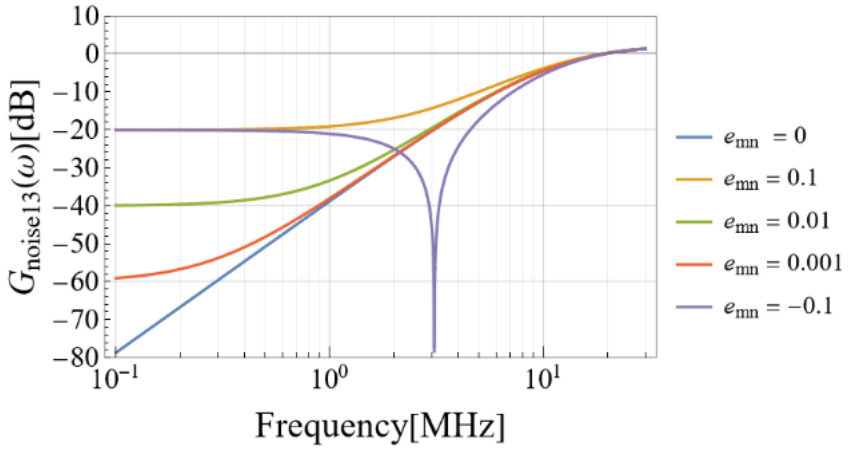


Fig. 3-18. Calculated $G_{noise13}(\omega)$ with e_{mn}.

3.5. CM Noise Cancelling Effect in the Measurement

Herein, the experimental circuits were designed and implemented based on the discussion in the previous sections. The proposed circuit's CM noise reduction effect was investigated using the measurements.

3.5.1. Experimental Setting

The experimental parameters are presented in Table 3-2.

Table 3-2. Circuit parameters for calculation and experiment.

Definition	Symbol	Value
Input voltage	V_{in} [V]	200
Output voltage	V_o [V]	300
Input power	P_{in} [W]	1.00×10^{3}
Switching frequency	F_{sw} [Hz]	1.00×10^{5}
Leakage inductance of main windings	L_{lk} [H]	1.48×10^{-4}
Magnetizing inductance	L_{mg} [H]	8.60×10^{-5}
Parasitic capacitance	C_a [F]	4.22×10^{-11}

Although the number of turns of the auxiliary winding should be minimized, as explained in Section 3.4.3, the CM noise reduction effect was compared between two numbers of turns of the auxiliary winding: 15 turns and 1 turn. The number of turns of the main windings was 30 in the conventional and proposed circuits. The circuit parameters dependent on the number of turns of the auxiliary winding are presented in Table 3-3. The turns ratio n was calculated from the main

Table 3-3. Circuit parameters for different values of n.

Definition	15 turns	1 turn
Number of main windings turns	30.0	
n	5.00×10^{-1}	3.33×10^{-2}
L_{lk3}[H]	4.91×10^{-5}	4.57×10^{-7}
C'_a [F]	9.02×10^{-11}	1.39×10^{-9}
Resonant frequency of L_{lk3} & C'_a[Hz]	2.39×10^{6}	6.34×10^{6}
m	2.13×10^{0}	3.29×10^{1}
mn	1.07×10^{0}	1.10×10^{0}
e_{mn}	6.87×10^{-2}	9.79×10^{-2}
$\sqrt{L_{lk3}/C'_a}$ [Ω]	7.38×10^{2}	1.81×10^{1}

and auxiliary windings. Once n is acquired, C'_a is designed to meet $mn = 1$, as explained in Section 3.3. The mn values calculated in Table 3-3 had errors but were suppressed to 7% and 10% in the 15-turn winding and 1-turn winding, respectively. Whether the CM noise increases in the proposed circuit can be predicted from the value of $\sqrt{L_{lk3}/C'_a}$ and (3-27). The target frequency band of CM noise reduction was set to be under 1 MHz, that is, the 10th harmonics of the switching frequency F_{sw} = 100 kHz. The details of the measurement equipment are presented in Table 3-4. The measured CM noise was evaluated by comparing the CM noise in the proposed and conventional circuits.

Table 3-4. Measurement equipment.

Instrument	Part number	Manufacturer
LISN	NNBM 8124	SCHWARZBECK
CM/DM switch	CMDM 8700	SCHWARZBECK
Spectrum analyzer	RSA306B	Tektronix

3.5.2. Implementation of the Coupled Inductor with Auxiliary Winding

The auxiliary winding generates the reversed-phase noise voltage source by the magnetic coupling with the leakage inductance of the main winding L_{lk}, as shown in Fig. 3-8. The magnetic structure shown in Fig. 3-15 was employed in the implementation. The flux corresponding to the magnetizing inductance is canceled in the auxiliary winding loop, and only the flux corresponding to the leakage inductance appears to cross the auxiliary winding. As a result, the auxiliary winding ideally generates $V_{noise3}(\omega)$ in (3-13). As shown in Fig. 3-19, the auxiliary winding was not wound around the center leg but around the core's outer legs to include the flux that leaks into the air. The same magnetic core with high permeability was utilized for the coupled inductor in the conventional and proposed circuits to maintain the conversion performance. The core was made of PC40, an Mn-Zn ferrite used for high power applications with a low loss at high frequency

manufactured by TDK, and the shape is EE type EC70×69×16.

The results of the implemented coupled inductor are presented in Table 3-5. The auxiliary winding and the capacitor C'_a were added to the inductor in the proposed circuit. However, the additional components increased the weight of the inductor only by 5.86%. Therefore, the power density of the proposed circuit is rarely degraded in the proposed circuit.

3.5.3. CM Noise Reduction Effect of Auxiliary Winding

The experimental circuit and the experimental environment are shown in Fig. 3-20 and Fig.

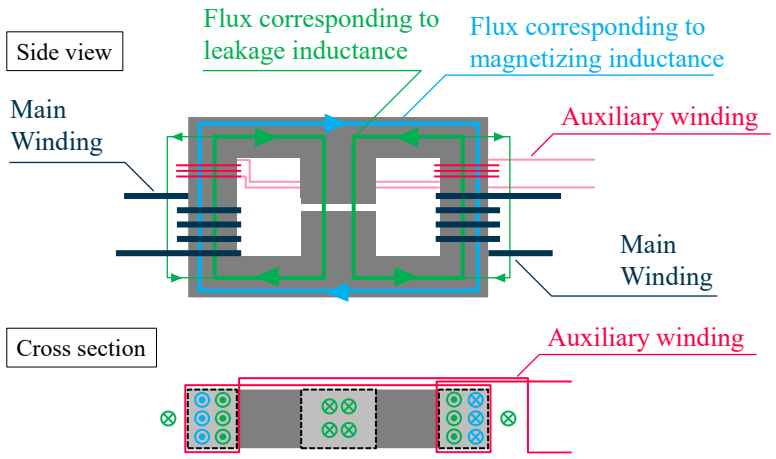
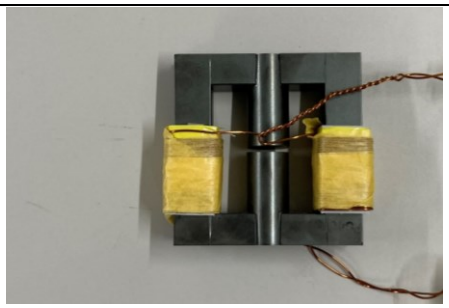
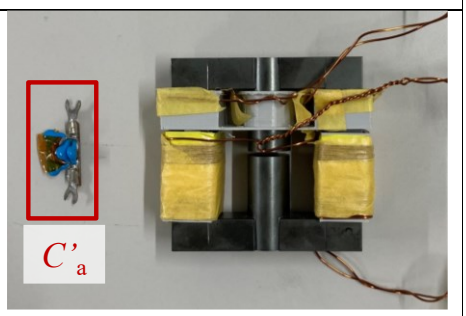


Fig. 3-19. Magnetic structure of the coupled inductor with auxiliary winding.

Table 3-5. Calculated result of $V_{noise3}(\omega)$ referring to Table 3-3.

	Conventional	Proposed
Components	Coupled inductor	Coupled inductor + Aux. winding + C'_a
Photograph		
Weight	290 g	307 g (+5.86 %, 17 g)

3-21. The measurement results of the CM noise spectra in the conventional circuit, the proposed circuit with the 15-turn auxiliary winding, and the proposed circuit with the 1-turn auxiliary winding are shown in Fig. 3-22 (a), (b), and (c), respectively. All the spectra shown in Fig. 3-22

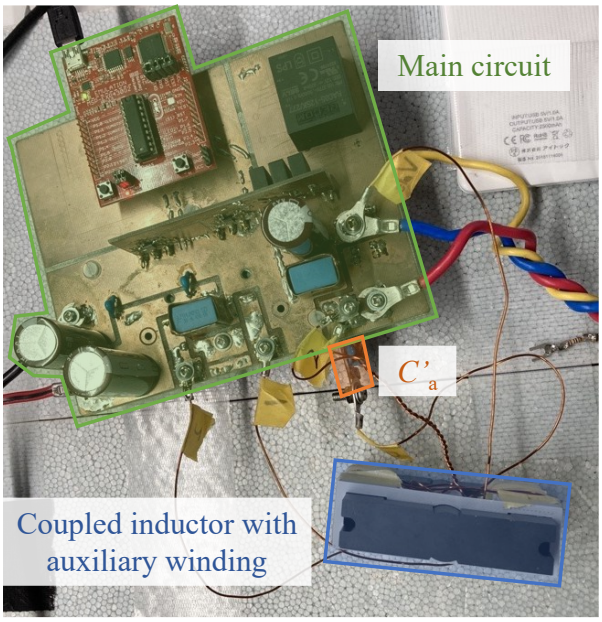


Fig. 3-20. Experimental circuit.

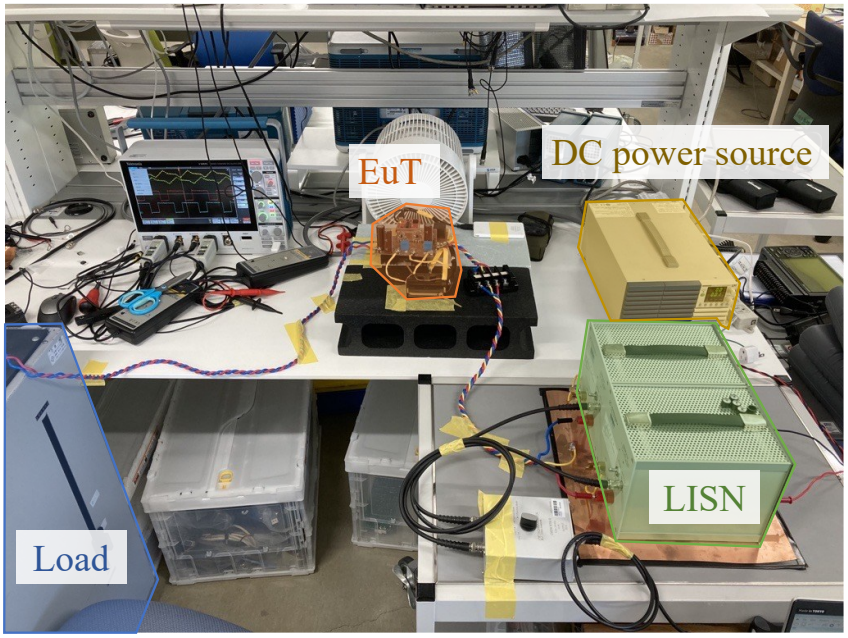


Fig. 3-21. Experimental environment.

are compared in Fig. 3-23. The even harmonics elements of F_{sw} dominated because the noise source of the two-phase interleaved converter appeared to have a switching frequency of $2F_{sw}$. In addition, the calculated results of $G_{noise13}(\omega)$ referring to Table 3-3 are shown in Fig. 3-24.

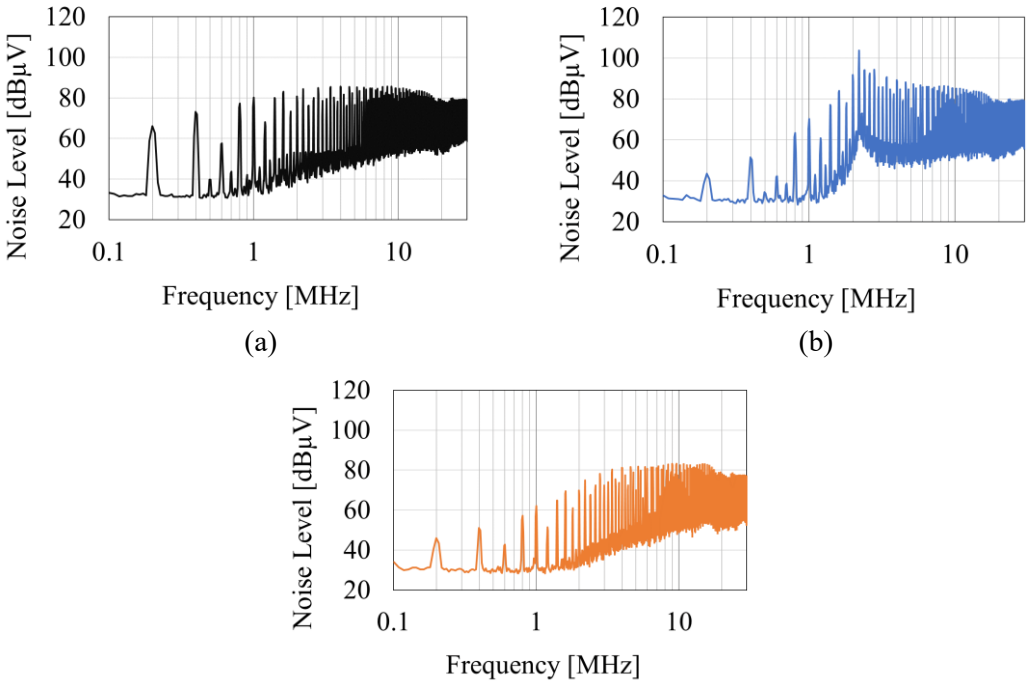


Fig. 3-22.Experimental CM noise spectra in (a) conventional circuit, (b) proposed circuit with 15 turns auxiliary winding, and (c) proposed circuit with 1 turn auxiliary winding.

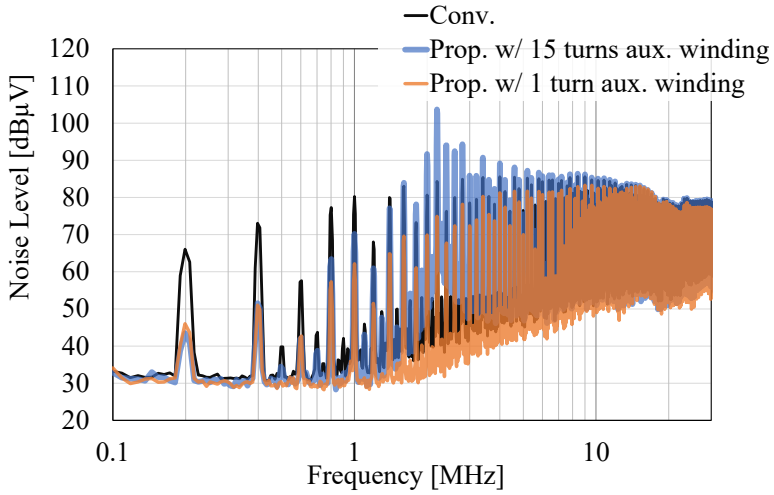


Fig. 3-23. Comparison of experimental CM noise spectra.

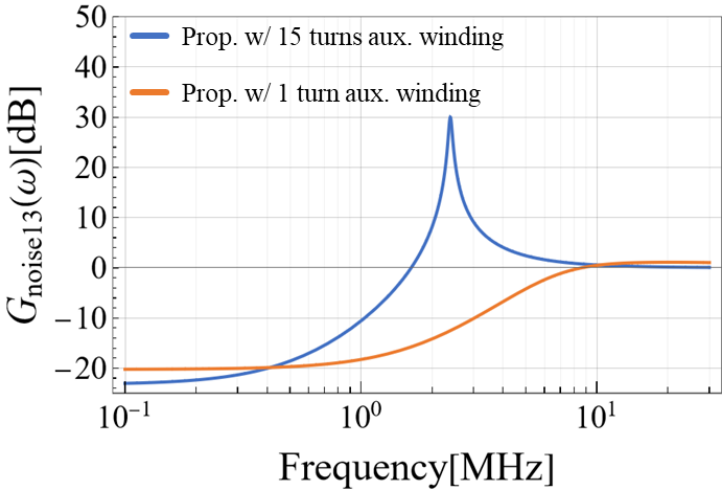


Fig. 3-24. Calculated result of $G_{noise3}(\omega)$ referring to Table 3-3.

As shown in Fig. 3-23, the CM noise decreased the most at 200 kHz in both the proposed circuits. The CM noise decreased by 22.6 dB with the 15-turn auxiliary winding and by 20.1 dB with the 1-turn auxiliary winding. In addition, based on the values of e_{mn} in Table 3-3, $G_{noise13}(\omega)$ shown in Fig. 3-24 had a lower limit of -23.3 dB with the 15-turn auxiliary winding and a lower limit of -20.2 dB with the 1-turn auxiliary winding. Therefore, the experimental and calculation results had less than a 3.10% error regarding the maximum amount of CM noise reduction.

From the values of $\sqrt{L_{lk3}/C'_a}$ presented in Table 3-3, the 15-turn auxiliary winding met $R_{LISN} < \sqrt{L_{lk3}/C'_a}$, and the CM noise increased with the 15-turn auxiliary winding at 2.39 MHz, which is the resonant frequency of L_{lk3} and C'_a, both in Fig. 3-23 and Fig. 3-24. Here, the amount of noise increase was 19 dB in Fig. 3-23; however, the increase was 30 dB in Fig. 3-24. This difference was because the parasitic resistance of the auxiliary winding is not considered in the calculation. By contrast, the 1-turn auxiliary winding met $R_{LISN} \geq \sqrt{L_{lk3}/C'_a}$, and the CM noise did not increase at 6.34 MHz, which is the resonant frequency of L_{lk3} and C'_a, both in Fig. 3-23 and Fig. 3-24.

Moreover, the CM noises in the proposed circuits with the 15-turn winding and 1-turn

windings showed little change over 10 MHz, both in Fig. 3-23 and Fig. 3-24.

Consequently, it was verified that the CM noise under 1 MHz is decreased with the auxiliary winding. By contrast, as discussed in the previous sections, the CM noise reduction effect is restricted depending on L_{lk3}, C'_a, or e_{mn}. In addition, the unnecessary increase in the CM noise due to resonance can be suppressed by designing $\sqrt{L_{lk3}/C'_a}$ as small as possible.

3.6. Discussion

3.6.1. Expanding the Phase Number of the Interleaved DC–DC Converter with Auxiliary Winding

The previous sections discussed the two-phase interleaved DC–DC converter. Based on this discussion, the extension of the phase number is further discussed in this section.

Herein, the N_p-phase interleaved DC–DC converter with the phase number N_p is discussed. However, only the ideal situation is mathematically analyzed in this section, and the analysis with the leakage inductance of the auxiliary winding or experimental verification is not conducted in this dissertation. The simplified CM noise equivalent circuit of a conventional N_p-phase interleaved DC–DC converter is shown in Fig. 3-18, which is the extended version of Fig. 3-5. The conventional circuit includes the noise source $V_{noise1}(\omega)$, $V_{noise2}(\omega)$, …, and $V_{noise}{}_{Np}(\omega)$, and each phase has the CM capacitance C_a. The CM capacitances act as CM noise propagation paths.

The simplified CM noise equivalent circuit of the proposed circuit with N_p phases is shown in Fig. 3-26. In the proposed circuit, an auxiliary winding and a capacitor C'_a are added to cancel the CM noise, similar to that of the proposed circuit with two phases discussed in the previous sections. The voltage applied to the auxiliary winding $V_{noise(Np+1)}(\omega)$ is expressed as follows:

$$V_{noise(Np+1)}(\omega) = -nV_{noise}(\omega) \quad \cdots\cdots (3\text{-}30)$$

, where $V_{noise}(\omega)$ is expressed as follows:

$$V_{noise}(\omega) = \sum_{k=1}^{N_p} V_{noise}{}_k(\omega) \quad \cdots\cdots (3\text{-}31)$$

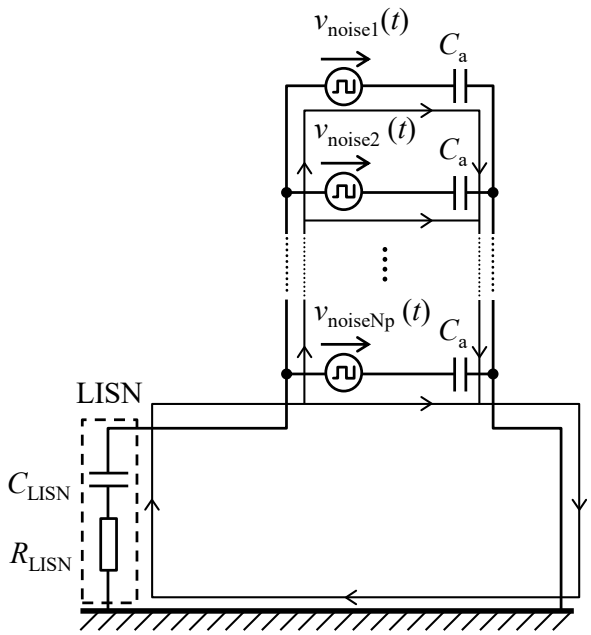


Fig. 3-25. Simplified CM noise equivalent circuit of the conventional circuit with N_p-phases

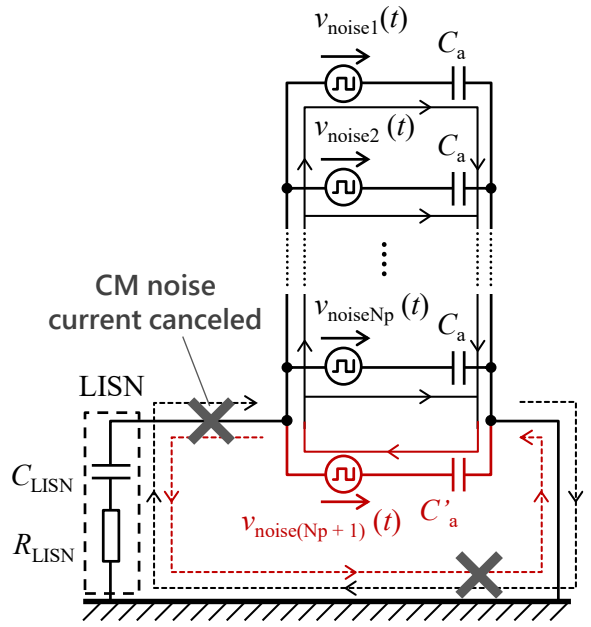


Fig. 3-26. Simplified CM noise equivalent circuit of the proposed circuit with N_p-phases

Here, the CM noise terminal voltage in the conventional circuit $V_{LISN\_conv}(\omega)$ and that in the proposed circuit $V_{LISN\_prop}(\omega)$ are expressed as follows with N_p phases:

$$V_{LISN\_conv}(\omega) = \frac{-j\omega C_a C_{LISN} R_{LISN} V_{noise}(\omega)}{C_{LISN} + N_p C_a (1 + j\omega C_{LISN} R_{LISN})} \quad \text{(3-32)}$$

$$V_{\mathrm{LISN\_prop}}(\omega)=\frac{j\omega C_{\mathrm{a}}C_{\mathrm{LISN}}R_{\mathrm{LISN}}(mn-1)V_{\mathrm{noise}}(\omega)}{C_{\mathrm{LISN}}+C_{\mathrm{a}}(N_{\mathrm{p}}+m)(1+j\omega C_{\mathrm{LISN}}R_{\mathrm{LISN}})} \quad (3\text{-}33)$$

From (3-32) and (3-33), the ratio of CM noise between the proposed circuit and the conventional circuit is expressed as follows:

$$\frac{V_{\mathrm{LISN\_prop}}(\omega)}{V_{\mathrm{LISN\_conv}}(\omega)}=\frac{(1-mn)\left(C_{\mathrm{LISN}}+N_{\mathrm{p}}C_{\mathrm{a}}(1+j\omega C_{\mathrm{LISN}}R_{\mathrm{LISN}})\right)}{C_{\mathrm{LISN}}+C_{\mathrm{a}}(N_{\mathrm{p}}+m)(1+j\omega C_{\mathrm{LISN}}R_{\mathrm{LISN}})} \quad (3\text{-}34)$$

From (3-34), the CM noise in the proposed circuit is canceled when $mn = 1$. Consequently, the CM noise in the N_{p}-phase interleaved DC–DC converter with any N_{p} more than three is canceled with the auxiliary winding, and C'_{a} is designed to meet $mn = 1$ similar to that in the two-phase interleaved DC–DC converter discussed in the previous sections.

3.6.2. Auxiliary Winding Applied to Other Circuit Configurations

The multi-phase boost DC–DC converter is discussed in the previous sections, and the auxiliary winding applied to other circuit configurations is considered in this section.

The two-phase interleaved buck DC–DC converter with an auxiliary winding and the CM noise equivalent circuit is shown in Fig. 3-27 (a) and (b), respectively. The buck converter and the boost converter have a symmetrical structure. Therefore, the CM noise equivalent circuits are identical, and the auxiliary winding can cancel the noise.

The two-phase interleaved power factor correction (PFC) circuit with an auxiliary winding is shown in Fig. 3-28 (a). The right pair of the MOSFETs switches in the grid frequency, which is a considerably lower frequency than that of other switches. Therefore, the right pair of the MOSFETs are ignored in the CM noise equivalent circuit shown in Fig. 3-28 (b). Consequently, the CM capacitance of the switching node is connected parallel with the LISN in Fig. 3-28 (b). Therefore, Fig. 3-28 (b) has an equivalent circuit that only adds a capacitor parallel to the LISN to the equivalent circuit in Fig. 3-12. Therefore, the auxiliary winding can still cancel the CM noise in the PFC circuit.

As shown in Fig. 3-27 and Fig. 3-28, the CM noise reduction method with auxiliary winding can be expanded to other circuit configurations compared with the multi-phase interleaved boost DC–DC converter.

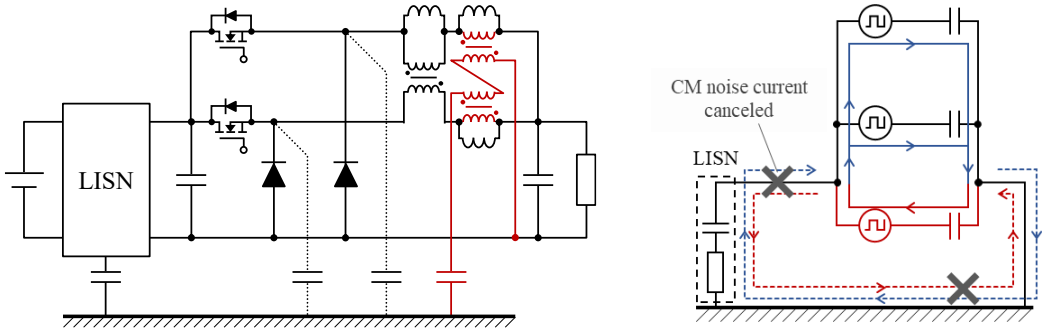


Fig. 3-27. two-phase interleaved buck DC-DC converter with an auxiliary winding in (a) circuit diagram and (b) CM noise equivalent circuit.

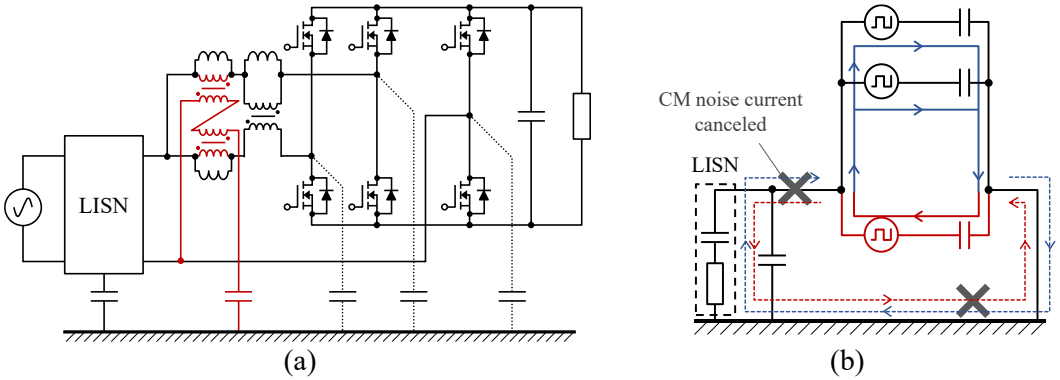


Fig. 3-28. two-phase interleaved PFC converter in (a) circuit diagram and (b) CM noise equivalent circuit.

3.7. Conclusion

In this chapter, the multi-phase circuit configuration with an auxiliary winding was proposed to reduce the CM noise. First, the conventional and proposed circuit configurations were mathematically analyzed, and the CM noise reduction mechanism was explained. Next, the design guideline of the auxiliary winding that $mn = 1$ was indicated. Furthermore, the CM noise reduction mechanism was analyzed in a more practical condition. As a result of the analysis, the number of turns in the auxiliary winding was minimized to suppress the increase in noise from resonance.

Finally, the CM noise reduction effect was investigated in the simulation and experiment. In addition, the degradation of the power density of the experimental circuit with the auxiliary winding and C'_a were verified to be minor. The expansibility of the proposed circuit configuration's phase number to more than 3 as well as the applications of the auxiliary winding to other circuit configurations was discussed. The characteristics of the CM noise reduction with auxiliary winding are summarized in Table 3-6.

In conclusion, the proposed circuit configuration was verified to reduce the CM noise to lower than 1 MHz in a multi-phase DC–DC converter with arbitrary phase numbers and with a slight change in the converter's power density.

Table 3-6. Characteristics of proposed CM noise reduction methods.

	Strong points	Weak points
CHAPTER 3 Auxiliary winding	- Small increase in volume & weight - Available for any number of phases	- CM noise reduction frequency band is limited by leakage inductance L_{lk3}

CHAPTER 4: CM NOISE REDUCTION WITH REVERSED CIRCUIT CONFIGURATION

4.1. Research Background

Switching devices are divided into two categories based on semiconductor chip structures: lateral and vertical. The vertical device has a high voltage rating and low on-resistance. Therefore, vertical devices are often employed in high power applications. The cross section of the semiconductor chips of vertical and lateral devices are shown in Fig. 4-1 (a) and (b)[98]-[101], respectively. The lateral device has the source, gate, and drain terminals on the top surface of the chip, whereas the vertical device has a drain terminal on the bottom surface and source and gate terminals on the top surface of the chip. Thus, the drain terminal is connected to the thermal pad when the chip is packaged. An implemented vertical device is shown in Fig. 4-2 (a) and (b). The parasitic capacitance to the ground, defined as CM capacitance in this dissertation, inevitably exists between the thermal pad and the heat sink because the thermal pad is placed close to the

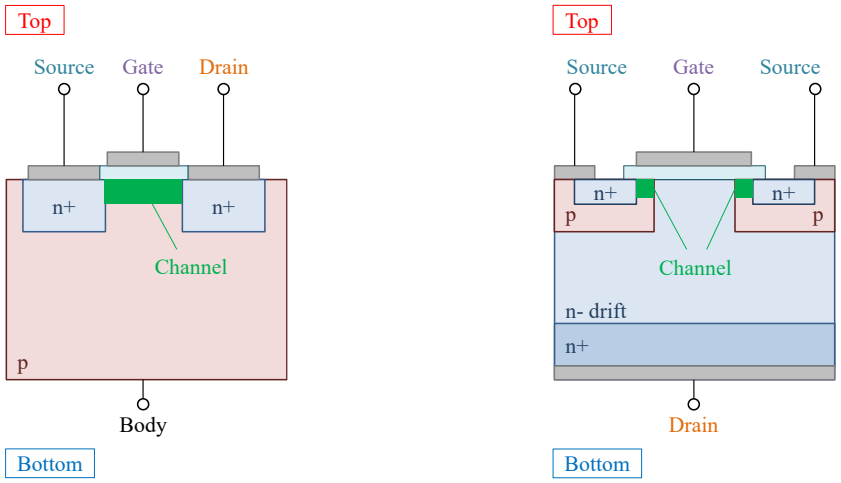


Fig. 4-1. Cross-section of semiconductor chip: (a) lateral MOSFET and (b) vertical MOSFET[98]-[101].

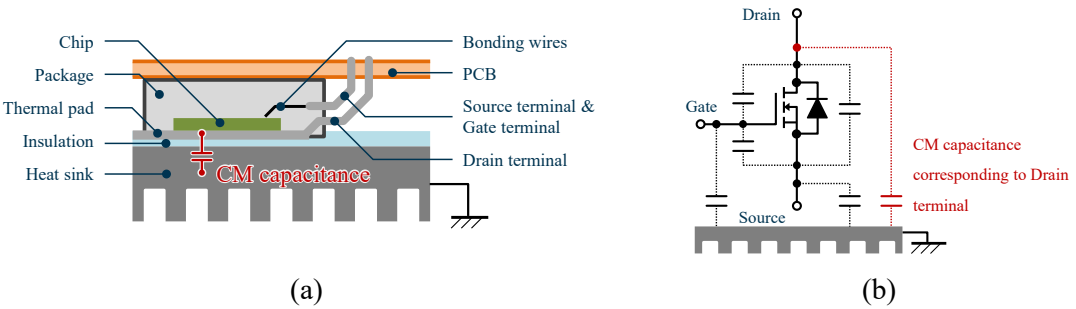


Fig. 4-2. Implemented vertical device in (a) cross-section and (b) circuit diagram.

heat sink for efficient heat dissipation. Therefore, the CM capacitance corresponding to the drain terminal dominates. As discussed in the previous section, the CM capacitance corresponding to the switching node becomes the primal CM noise propagation path. A large CM capacitance connected to the switching node results in a large CM noise current. Therefore, CM noise increases when the drain terminal of the vertical MOSFET is assigned to the switching node.

In this chapter, a circuit structure that implements a vertical MOSFET to decrease the CM capacitance in the CM noise propagation path is proposed to reduce the CM noise. The CM noise in the conventional and proposed circuits is analyzed and compared mathematically. Next, the experimental circuit implementation is discussed and compared. Finally, the results of the circuit simulation and experiment are indicated to verify the CM noise reduction effect.

4.2. Proposed Method

4.2.1. Conventional and Proposed Circuits

The conventional and proposed circuits are shown in Fig. 4-3 (a) and (b). A non-isolated boost converter is used as the investigation circuit. The CM capacitance in the conventional circuit is divided into C_{d_conv}, C_{s_conv}, C_{vin_conv}, and C_{vo_conv}. These CM capacitances correspond to each node in the boost converter, as shown in Fig. 4-3 (a). The CM noise propagates through the components of these CM capacitances. LISN is inserted between the input voltage source and the

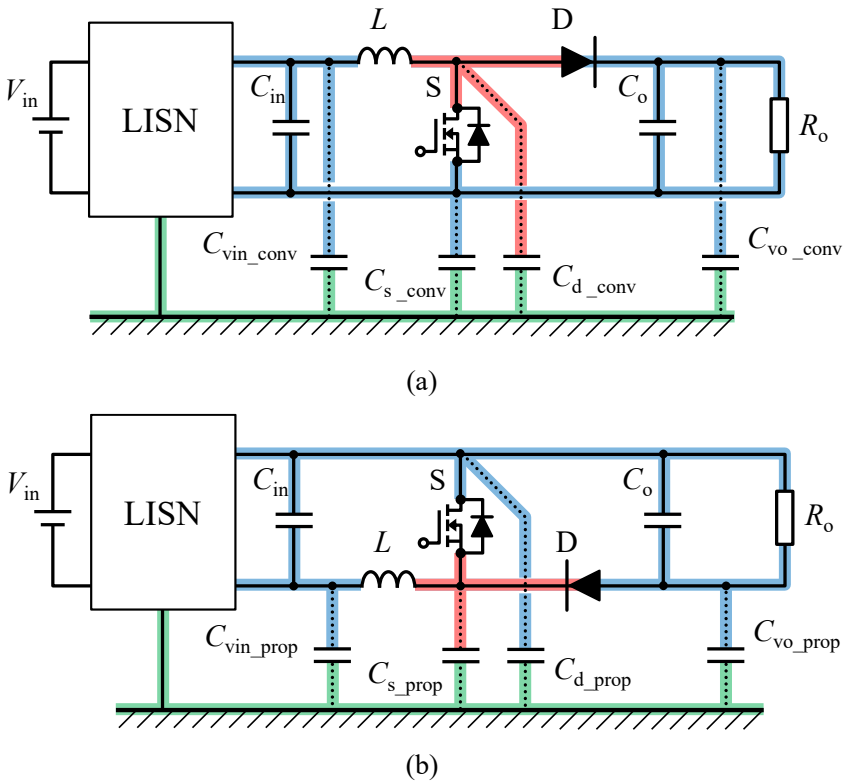


Fig. 4-3. (a) conventional circuit and (b) proposed circuit.

boost converter circuit for CM noise measurement. For clarification, the nodes are colored. In Fig. 4-3 (a), red indicates the switching node, blue indicates other DC nodes, and green indicates the ground. The CM capacitance C_{d_conv} exists between the switching node and the ground in Fig. 4-3 (a). Therefore, C_{d_conv} is charged and discharged when the switch S is turned off and on, which becomes the CM noise propagation path in the conventional circuit. Thus, the CM noise current decreases when C_{d_conv} becomes small.

By contrast, the proposed circuit shown in Fig. 4-3 (b) has a reversed version of the conventional circuit configuration. The inductor L and diode D move to the lower potential line, and the higher potential line is shorted between the input and the output terminals. The CM capacitance in the proposed circuit is divided into C_{d_prop}, C_{s_prop}, C_{vin_prop}, and C_{vo_prop}. These CM capacitances also correspond to each node in the proposed

circuit are colored in the same manner as in the conventional circuit. In Fig. 4-3 (b), the source terminal of the MOSFET S is the switching node. The CM capacitance C_{s_prop} exists between the switching node and the ground in Fig. 4-3 (a). Therefore, C_{s_prop} is charged and discharged when the switch S is turned on and off, thus becoming the CM noise propagation path in the proposed circuit structure. Thus, the CM noise current decreases when C_{s_prop} becomes small.

When a vertical MOSFET is utilized for the switch S in each circuit, it is assumed that each circuit has the same CM capacitance distribution, which is expressed as follows:

$$C_{d\_conv} = C_{d\_prop} > C_{s\_conv} = C_{s\_conv} \quad \text{(4-1)}$$

The behavior of noise current around a MOSFET in the conventional and proposed circuits is shown in Fig. 4-4 (a) and (b). The CM noise current flows through the CM capacitance corresponding to the switching node, such as C_{d_conv} and C_{s_prop}, because the voltage potential of the switching node fluctuates. A part of the noise current flows back to the DC line colored in blue through the other CM capacitances, and the remaining noise current that flows through the LISN is the CM noise current. In Fig. 4-4, the CM noise current in the conventional circuit is larger than that in the proposed circuit because the impedance of C_{d_conv} is smaller than C_{s_prop}. Therefore, the CM noise in the proposed circuit decreases, even though the noise sources and CM

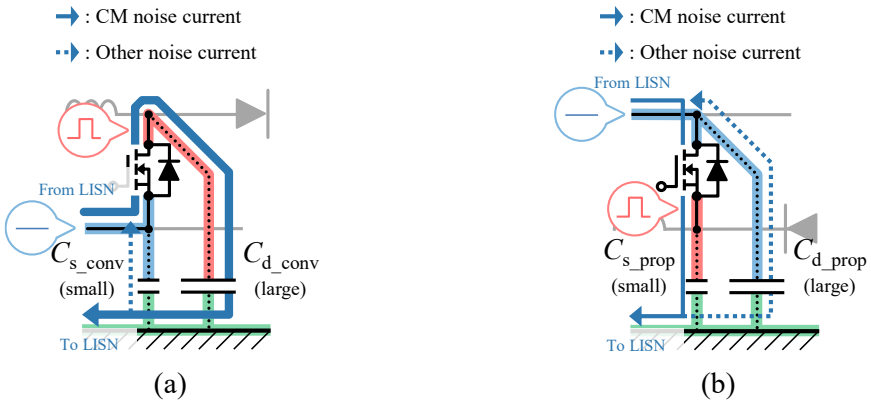


Fig. 4-4. Simplified behavior of (a) conventional circuit and (b) proposed circuit.

capacitance distributions are the same in the conventional and proposed circuits. Here, the conventional and proposed circuits have the same circuit components; thus, the proposed circuit configuration does not degrade the power density. The proposed method without additional circuit components is superior to the external filters in the power density perspective, as discussed in Chapter 1. In the following section, the CM noise reduction mechanism is mathematically analyzed.

4.2.2. CM Noise Analysis

In this section, the CM noise with the CM noise equivalent circuit is analyzed. First, the conventional and proposed circuits as a CM noise equivalent circuit are shown in Fig. 4-5 (a) and (b), respectively. When each circuit is transformed into a CM noise equivalent circuit, the input and output capacitances C_{in} and C_o are assumed to be short because the capacitances are sufficiently large. Similarly, the inductor L is assumed to be open because the inductance is sufficiently large. Next, C_{s_conv}, C_{vin_conv}, and C_{vo_conv}, which are the CM capacitances

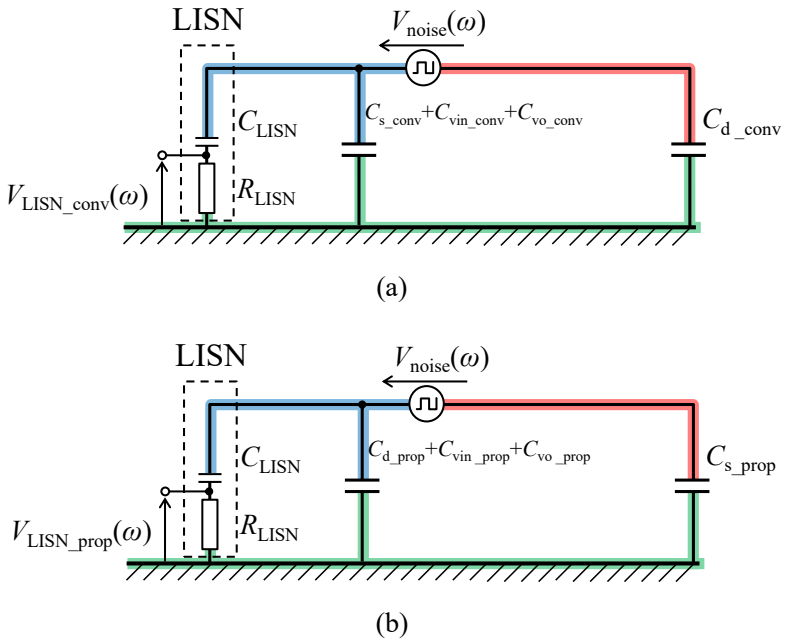


Fig. 4-5. CM noise equivalent circuit of (a) conventional circuit and (b) proposed circuit.

corresponding to the DC nodes, are combined in the conventional circuit. Likewise, C_{d_prop}, C_{vin_prop} and C_{vo_prop} are combined in the proposed circuit. A MOSFET and a diode in each circuit are substituted with the noise voltage source $V_{noise}(\omega)$, where ω indicates the noise angular frequency. LISN in the CM noise circuit consists of a capacitor C_{LISN} and a resistor R_{LISN}, as shown in Fig. 4-5 (a) and (b). The CM noise terminal voltage in the conventional circuit $V_{LISN\_conv}(\omega)$ is expressed as follows:

$$V_{LISN\_conv}(\omega) = \frac{j\omega C_{LISN} C_{d\_conv} R_{LISN} V_{noise}(\omega)}{(C_{all\_conv} + C_{LISN}) + j\omega C_{LISN} C_{all\_conv} R_{LISN}} \quad \cdots\cdots (4\text{-}2)$$

, where

$$C_{all\_conv} = C_{d\_conv} + C_{s\_conv} + C_{vin\_conv} + C_{vo\_conv} \quad \cdots\cdots (4\text{-}3)$$

Here, j indicates the imaginary unit. From (4-2), the CM noise in the conventional circuit depends strongly on the CM capacitance C_{d_conv} that corresponds to the switching node. The CM noise terminal voltage in the proposed circuit $V_{LISN\_prop}(\omega)$ is expressed as follows from Fig. 4-5 (b):

$$V_{LISN\_prop}(\omega) = \frac{j\omega C_{LISN} C_{s\_prop} R_{LISN} V_{noise}(\omega)}{(C_{all\_prop} + C_{LISN}) + j\omega C_{LISN} C_{all\_prop} R_{LISN}} \quad \cdots\cdots (4\text{-}4)$$

, where

$$C_{all\_prop} = C_{d\_prop} + C_{s\_prop} + C_{vin\_prop} + C_{vo\_prop} \quad \cdots\cdots (4\text{-}5)$$

From (4-4), it is found that the CM noise in the proposed circuit also strongly depends on the CM capacitance C_{d_conv} corresponding to the switching node, as in the conventional circuit. Therefore, based on (4-2) and (4-4), the CM noise terminal voltage ratio between the conventional and proposed circuits is expressed as follows:

$$\frac{V_{LISN\_prop}(\omega)}{V_{LISN\_conv}(\omega)} = \frac{C_{s\_prop}\{(C_{all\_conv} + C_{LISN}) + j\omega C_{LISN} C_{all\_conv} R_{LISN}\}}{C_{d\_conv}\{(C_{all\_prop} + C_{LISN}) + j\omega C_{LISN} C_{all\_prop} R_{LISN}\}} \quad \cdots\cdots (4\text{-}6)$$

When $C_{all\_conv} = C_{all\_prop}$, the above equation (4-6) is converted into:

$$\frac{V_{LISN\_prop}(\omega)}{V_{LISN\_conv}(\omega)} = \frac{C_{s\_prop}}{C_{d\_conv}} \quad \cdots\cdots (4\text{-}7)$$

Herein, the CM capacitances corresponding to the switching node C_{d_conv} and C_{s_prop} are assumed

to be minimized. In this case, C_{d_conv} is naturally larger than C_{s_prop} because of the inevitable part of the CM capacitance corresponding to the drain terminal, and the CM noise decreases in the proposed circuit from (4-7). The CM noise reduction effect is verified in the simulation and experiment sections.

4.3. Circuit Design and CM Capacitance

The CM noise reduction effect was mathematically verified in the previous section when $C_{d\_conv} > C_{s\_prop}$ and $C_{all\_conv} = C_{all\_prop}$. The experimental circuit should be carefully designed and implemented for comparison in the experiment. In this section, the experimental circuit's design procedure before the simulation and the experiment is explained.

4.3.1. Implementation of Circuit Components

A cross section of the experimental circuit is shown in Fig. 4-6, which explains the circuit implementation. Only the diode, MOSFET, PCB, and heat sink are indicated in Fig. 4-6 for simplification. The MOSFET is placed on the bottom surface of the PCB such that the thermal pad is faced toward the heat sink to dissipate the heat effectively. Therefore, the PCB is away from the heat sink by the thickness of the MOSFET package. Thus, the CM capacitance that originates from the MOSFET dominates the total CM capacitance, and the influence of the PCB on the CM capacitance is ignored in the circuit implementation shown in Fig. 4-6. In addition, the diode is mounted on the top surface to prevent the diode from affecting the CM capacitance. Furthermore, the heat sink, insulation sheet, MOSFET, and PCB are screwed together by the same torque in both circuits such that the CM capacitances corresponding to MOSFETs become the

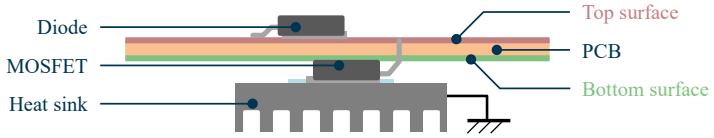


Fig. 4-6. Simplified cross-section of an experimental circuit.

same.

4.3.2. PCB Patterns

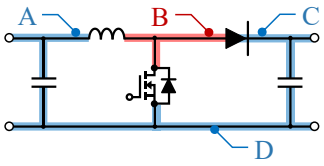
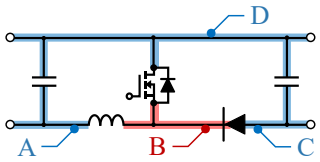
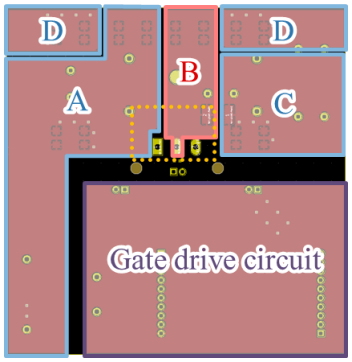
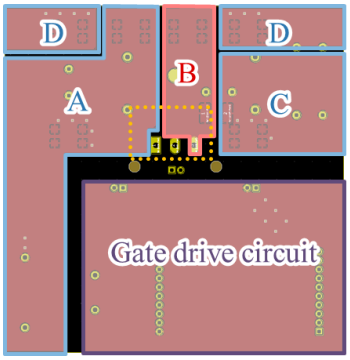
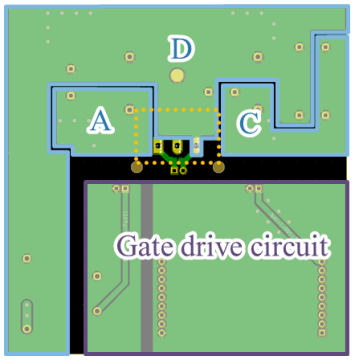
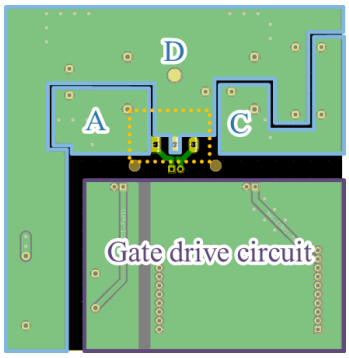
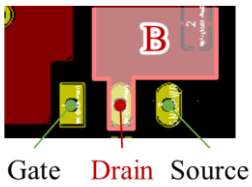
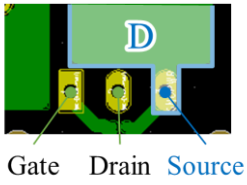
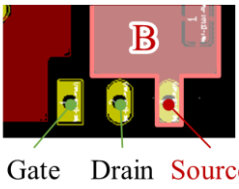
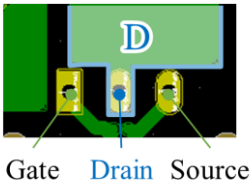
In the experimental circuits, the total CM capacitance C_{all_conv} and C_{all_prop} should have the same value for a precise comparison. Additionally, the CM capacitances corresponding to the switching nodes C_{d_conv} and C_{s_prop} should be minimized to reduce the CM noise as much as possible. In this section, the PCB patterns' design procedure to meet the abovementioned demands are explained. The circuit diagrams and PCB patterns on the top and bottom surfaces of the experimental circuits are presented in Table 4-1. Table 4-1 shows that each circuit is divided into four nodes: A, B, C, and D. Each of the top and bottom surfaces has a footprint for MOSFET in the yellow dotted square in each PCB. The enlarged circuit patterns around the MOSFETs are presented at the bottom of Table 4-1. Node B, colored in red, is a switching node, and CM capacitances corresponding to node B strongly influence the CM noise. As observed from Table 4-1, node B is connected to the drain terminal in the conventional circuit, whereas node B is connected to the source terminal in the proposed circuit. The PCB patterns assigned to node B are only on the top surfaces to eliminate the PCBs' influence, minimize the CM capacitances corresponding to the switching node, and achieve $C_{d\_conv} > C_{s\_prop}$. Additionally, both PCBs have the same size and shape to achieve $C_{all\_conv} = C_{all\_prop}$ for a precise comparison. In the following sections, the CM noise reduction effect of the proposed circuit is verified in the circuit simulation and experiment.

4.4. Simulation

4.4.1. Measurement and Extraction of CM Capacitance

The CM noise reduction effect of the proposed circuit was verified in the circuit simulation. Therefore, for circuit simulations, the distributed CM capacitances were modeled in the simulation. However, conducting separate measurements of each of the distributed CM

Table 4-1. Circuit diagrams and the PCB patterns of the experimental circuits.

	Conventional	Proposed
Circuit diagram		
Top surface		
Bottom surface		
Enlarged patterns around MOSFET	 	 

capacitances is difficult. Therefore, the total CM capacitances C_{all_conv} and C_{all_prop} were measured first. Next, each distributed CM capacitance was extracted through the finite element method

(FEM).

The circuit connections in the conventional and proposed circuits are shown in Fig. 4-7 and Fig. 4-8, respectively. All nodes were shorted in Fig. 4-6 (a) and Fig. 4-7 (a). Therefore, the capacitance between the shorted node and the ground is the total CM capacitance. The equivalent circuits of the measured circuits are shown in Fig. 4-7 (b) and Fig. 4-8 (b), and the measurement results are shown in Table 4-2. The measurement results of $C_{\text{all\_conv}}$ and $C_{\text{all\_prop}}$ showed a 6.90% error. These measurement results confirm the consistency of the extracted values of the CM capacitances in the FEM.

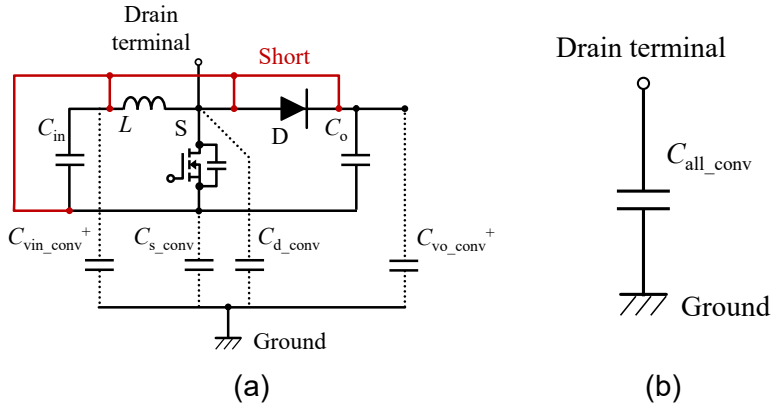


Fig. 4-7. Total CM capacitance in the conventional circuit (a) circuit connection for measurement and (b) equivalent circuit.

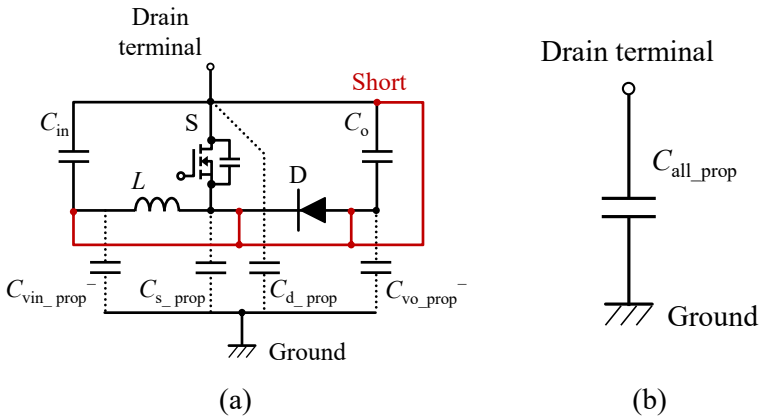


Fig. 4-8. Total CM capacitance in the proposed circuit (a) circuit connection for measurement

Table 4-2. Measurement results of the total CM capacitances.

C_{all_conv}	C_{all_prop}
90.4 pF	97.1 pF

Second, each of the distributed CM capacitances was extracted with the FEM. ANSYS Q3D was utilized for extracting the parasitic capacitance. The three-dimensional (3D) model created for the capacitance extraction is shown in Fig. 4-9. The model had a double-side PCB structure generated from the PCB design data. The size of PCB was 99.2 × 97.2 × 1.60 mm for the conventional and proposed circuits. The heat sink was substituted with the light gray box underneath the PCB. The MOSFET and the insulation sheet existed between the PCB and the heat sink. The thickness of the insulation sheet was adjusted such that the total extracted CM capacitances matched the measurement results because the sheet is flexible and the thickness changes, which is unmeasurable in the experimental circuit as the sheet is pressed. The extracted CM capacitance values of both the circuits are presented in Table 4-3 and Table 4-4. Both circuits had identical extracted total capacitances: $C_{all\_conv} = C_{all\_prop}$, and the error between the extracted

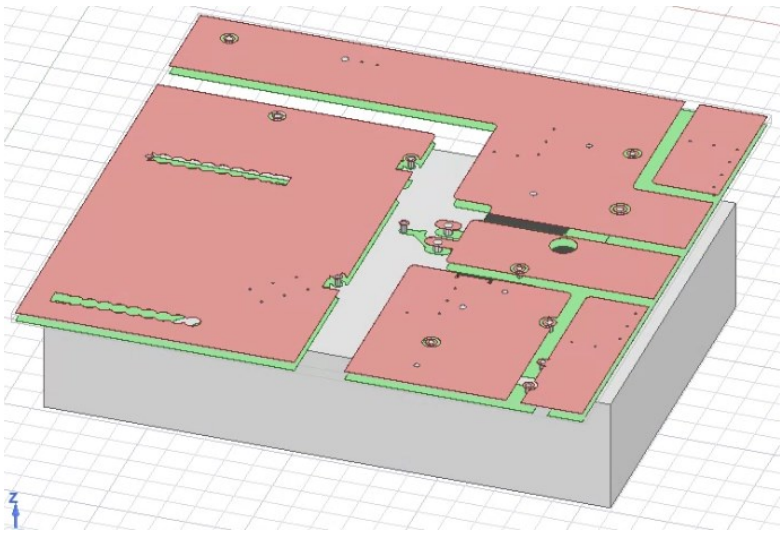


Fig. 4-9. 3D model of an experimental circuit in ANSYS Q3D for capacitance extraction.

Table 4-3. Extracted CM capacitances in the conventional circuit.

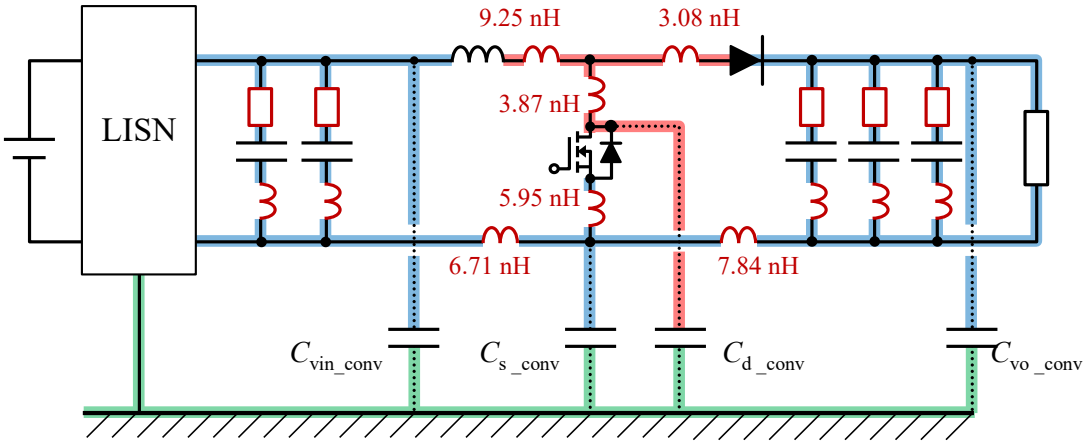
C_{all_conv}	C_{s_conv}	C_{vin_conv}	C_{vo_conv}	C_{d_conv}
101 pF	5.61 pF	2.39 pF	1.74 pF	91.1 pF

Table 4-4. Extracted CM capacitances in the proposed circuit.

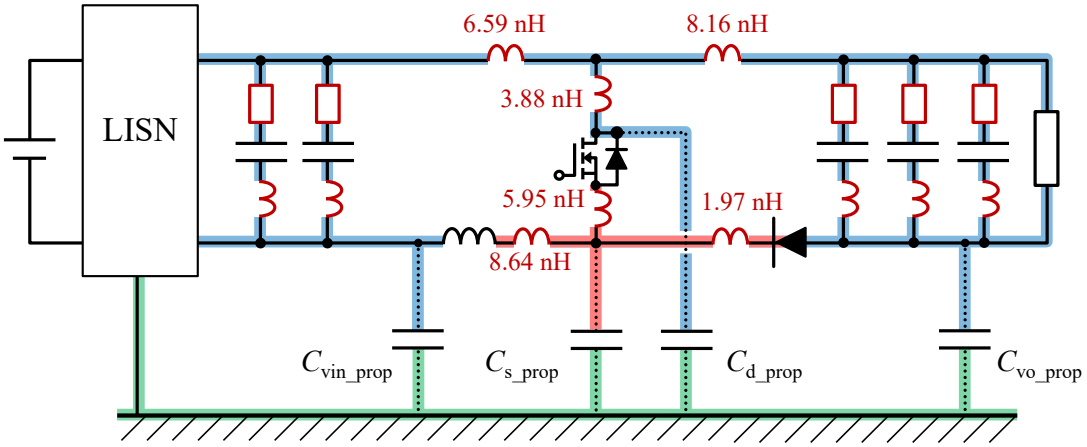
C_{all_prop}	C_{s_prop}	C_{vin_prop}	C_{vo_prop}	C_{d_prop}
101pF	0.771 pF	2.37 pF	1.73 pF	96.0 pF

and measured values of the total CM capacitance was less than 10.5%. Therefore, the extracted values of the CM capacitance were consistent with the measure values. The CM capacitances corresponding to the drain terminals dominated the total CM capacitance in each circuit. In addition, the extracted values met the condition $C_{d\_conv} > C_{s\_prop}$. Thus, the capacitance extraction results met the expected conditions for CM noise reduction.

In addition, the parasitic inductances were modeled in the circuit simulation to precisely analyze the CM noise in a broad bandwidth. The 3D model shown in Fig. 4-9 was also utilized to extract the parasitic inductances. Fig. 4-10 (a) and (b) show the extracted parasitic inductances. Although these parasitic inductances were extracted from the 3D models, the equivalent series inductance (ESL) and the equivalent series resistance (ESR) of the input and output capacitances were not extracted from the 3D models because the circuit components were not on the 3D models of PCB. Therefore, the ESLs and ESRs of the capacitances were measured before the input and output capacitances were implemented on the PCB. Each of the input and output capacitances consists of several capacitors. The input capacitance consists of an electrolytic capacitor and a film capacitor, whereas the output capacitor consists of two electrolytic capacitors and a film capacitor. The ESLs and ESRs of these two types of capacitors are presented in Table 4-5. These extracted and measured parasitic elements were used in the circuit simulation, discussed in the subsequent section.



(a)



(b)

Fig. 4-10. Extracted parasitic inductance from the 3D model of experimental circuits: (a) the conventional circuit and (b) the proposed circuit.

Table 4-5. Measured ESLs and ESRs of the electrolytic capacitor and film capacitor for the input and output capacitor.

	Capacitance [uF]	ESL [nH]	ESR [mΩ]	Part number	Manufacturer
Electrolytic capacitor	127	15.3	140	EKXJ451ELL151M M50S	NIPPON CHEMI-CON
Film capacitor	0.965	10.5	21.8	B32522N6105K000	EPCOS

4.4.2. Circuit Simulation

The circuit simulator PLECS was used for the circuit simulation. The circuit parameters for the circuit simulation and the experiment are presented in Table 4-6. The noise voltage sources $V_{noise}(\omega)$ in Fig. 4-5 (a) and (b) correspond to the drain-source voltage of the MOSFETs shown in Fig. 4-3 (a) and (b). The MOSFETs in the circuit simulation were ideal, and the CM capacitances corresponding to nodes refer to the extraction results. Additional 155 pF capacitance from the parasitic capacitance of the input cable between the LISN and the PCB was added to each CM capacitance corresponding to the input terminals C_{s_conv}, C_{vin_conv}, C_{d_prop}, and C_{vin_prop} in the circuit simulation. The CM noise was evaluated by comparing the CM noise of conventional and proposed circuits in the circuit simulation and experiment. The simulation results are shown in Fig. 4-11 (a), (b), and (c). As shown in Fig. 4-11 (a), the CM noise terminal voltage in the proposed circuit was more than 40 dB below that in the conventional circuit, which ranged from 100 kHz to 30 MHz. The amount of CM noise reduction is independent of the frequency when the parasitic inductance is not considered, as shown in (4-7) and Fig. 4-11 (a). As shown in Fig. 4-11 (c), the CM noise in the conventional circuit changed by less than 1 dB from 100 kHz to 30 MHz, even if the parasitic inductances are considered. However, the CM noise in the proposed circuit changed by more than 10 dB at 30 MHz when the parasitic capacitance was considered. Thus, the amount of CM noise reduction decreases in high frequency such as 30 MHz because the CM noise in the proposed circuit increases when the parasitic inductances are considered, which differs from the mathematical analysis results described in Section 4.2.2.

Based on the results shown in Fig. 4-11, it was found that the proposed circuit with a smaller CM capacitance corresponding to the switching node decreases the CM noise. However, the amount of CM noise reduction may change depending on the frequency because of parasitic inductances.

Table 4-6. The circuit parameter for simulation and experiment.

Parameter	Value
Input voltage	50 V
Output voltage	75 V
Input power	62.5 W
Switching frequency	100 kHz
Duty ratio	0.333
R_{LISN}	25.0 Ω
C_{LISN}	0.200 μF

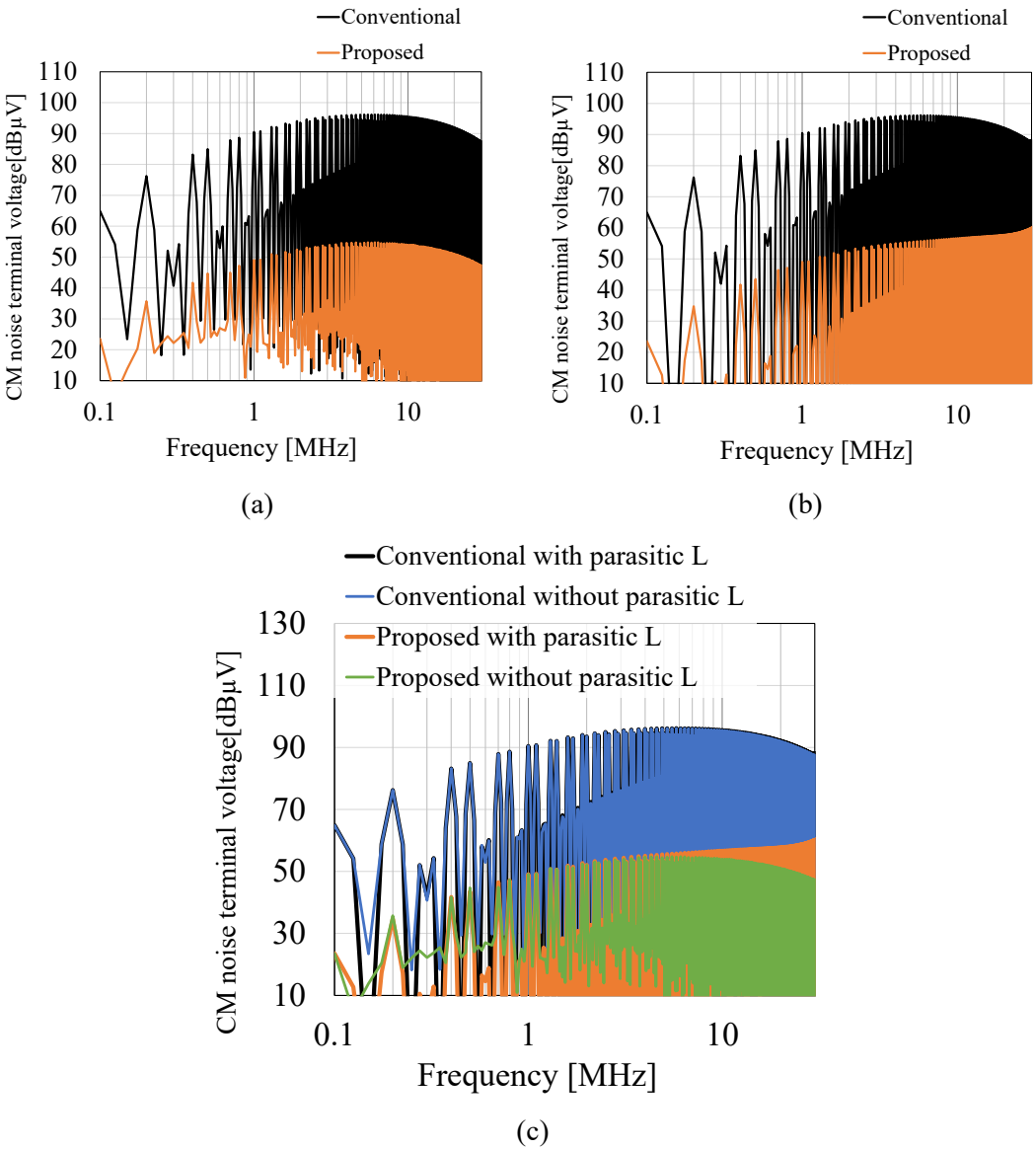


Fig. 4-11. Simulation results (a) without parasitic inductances, (b) with parasitic inductances, and (c) both compared.

4.5. Experiment

The two circuits were also compared in the experiment. The measurement equipment parameters used in the experiment is presented in Table 4-7. Fig. 4-12 and Fig. 4-13 show the experimental circuits and environment, and the experimental results are shown in Fig. 4-14. The CM/DM switch CMDM 8700 B, which extracts the CM element from the noise terminal voltage,

Table 4-7. The measurement equipment.

Instrument	Part number	Manufacturer
LISN	NNBM 8124	SCHWARZBECK
CM/DM switch	CMDM 8700 B	SCHWARZBECK
Spectrum analyzer	RSA306B	Tektronix

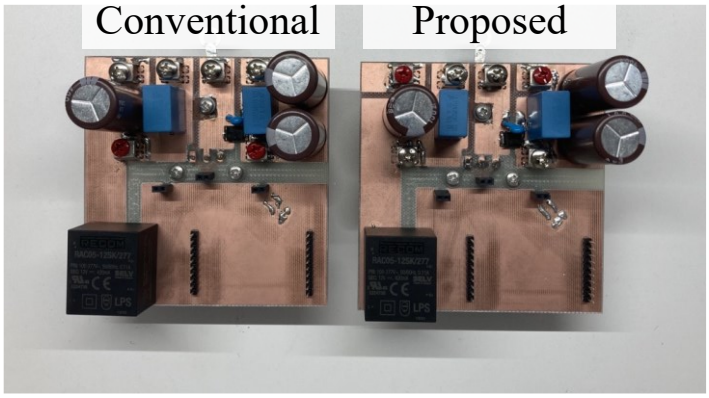


Fig. 4-12. Experimental circuits.

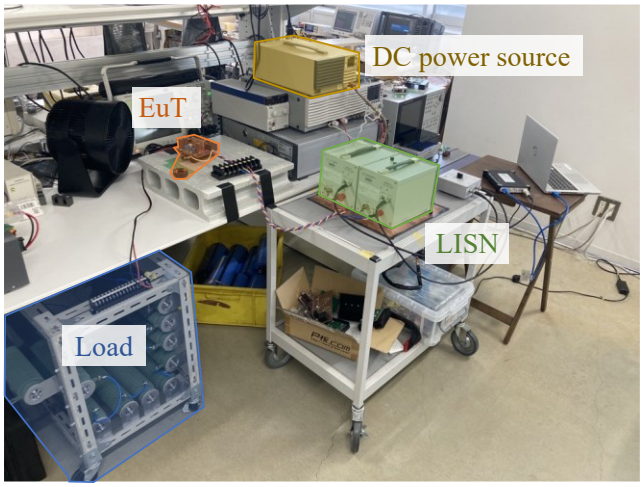


Fig. 4-13. Experimental environment.

attenuates the output signal by 20 dB ± 3 dB in the measurement frequency. Thus, the measurement result shown in Fig. 4-14 was corrected based on the attenuation of the result by the CMDM 8700. As shown in Fig. 4-14, the proposed circuit also decreased the CM noise in the experiment. The CM noise in the proposed circuit decreased by approximately 20 dB in a broad bandwidth, whereas the noise decreased by 26 dB at the maximum. The experimental results verified that the proposed circuit decreases the CM noise.

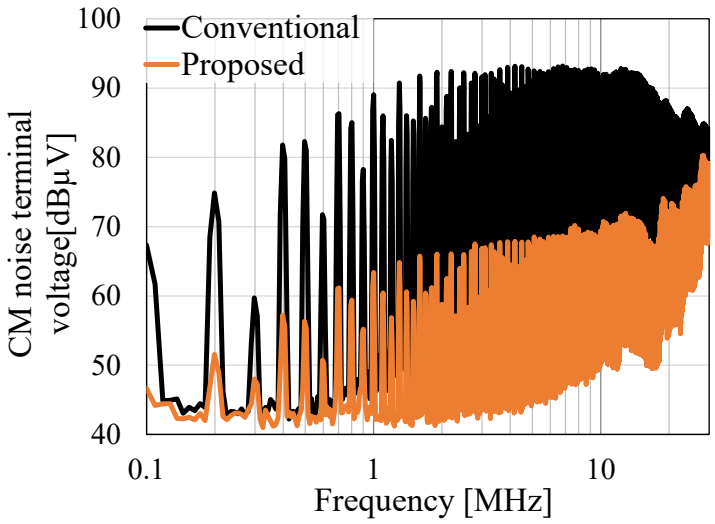


Fig. 4-14. Experimental results.

The simulation and experimental results are compared in Fig. 4-15 (a) and (b). The difference among the envelopes of conventional circuits was within 5 dB, ranging from 100 kHz to 30 MHz in Fig. 4-15 (a). However, the difference in envelopes between the simulation and experimental results of the proposed circuit was approximately 15 dB, ranging from 200 kHz to 7 MHz, and the difference increased in the frequency band higher than 7 MHz, even though the parasitic inductances were considered in the simulation shown in Fig. 4-15 (b). The causes of these differences between the CM noise terminal voltages in the simulation and experiment were

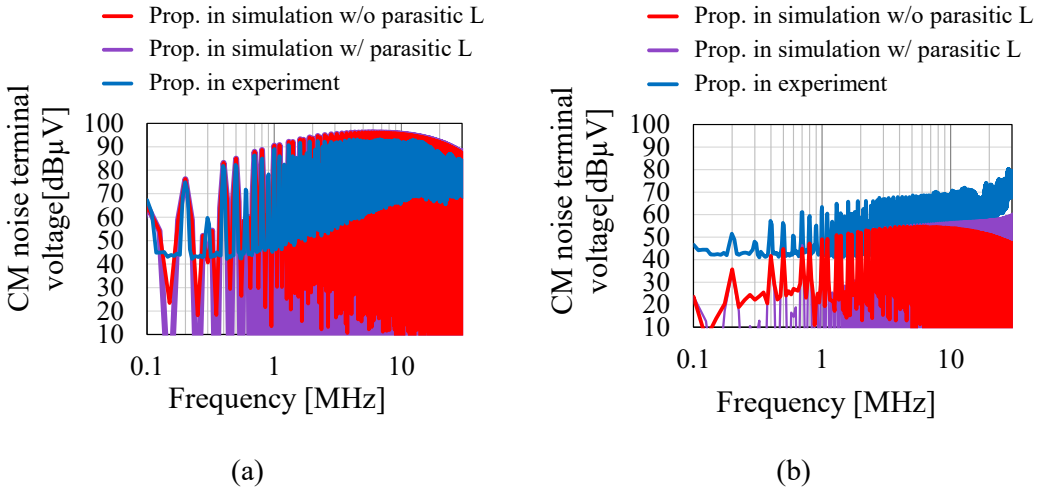


Fig. 4-15. Comparison of simulation and experimental results: (a) conventional and (b) proposed.

not identified but discussed as follows:

The spectra of the drain-source voltage of S are compared in Fig. 4-16. The drain-source voltage becomes a noise voltage source in conventional and proposed circuits. Thus, the spectra of noise voltage sources are compared first to investigate the influence of the noise source on the difference in CM noise. In the simulation, the drain-source voltages had identical spectra, whereas, in the experiment, the spectra of drain-source voltages in the conventional and proposed circuits differed within 2 dB.

By contrast, the difference between the simulation and experiment was approximately 5 dB at a frequency higher than 6 MHz, as shown in Fig. 4-16. This difference in noise voltage sources shown in Fig. 4-16 is close to the difference in the CM noise of conventional circuits shown in Fig. 4-15 (a). Therefore, the difference in the CM noise of conventional circuits originates from the difference in the noise sources. However, the difference in the CM noise in the proposed circuit in Fig. 4-15 (b) is significantly larger than that in the noise sources. Thus, the difference in CM noise between the simulation and experiment of the proposed circuit is

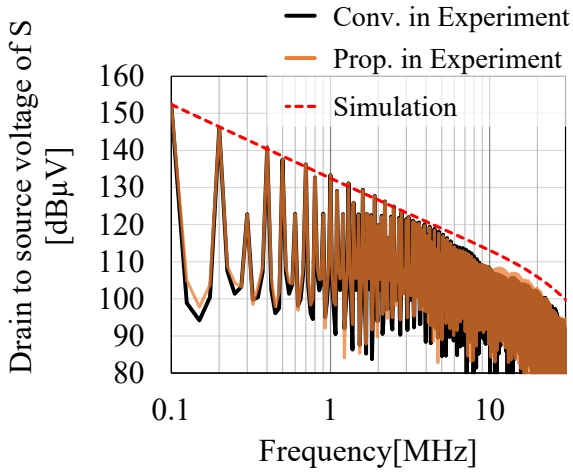


Fig. 4-16. Spectra of drain-source voltage of S in simulation and experiment.

considered to originate not from the noise sources but from the noise propagation paths.

To consider the causes of the difference in the CM noise between the simulation and the experiment, the envelopes of the CM noise terminal voltages of the proposed circuit are shown in Fig. 4-17. Each envelope is divided into two frequency regions: less than 7 MHz and more than

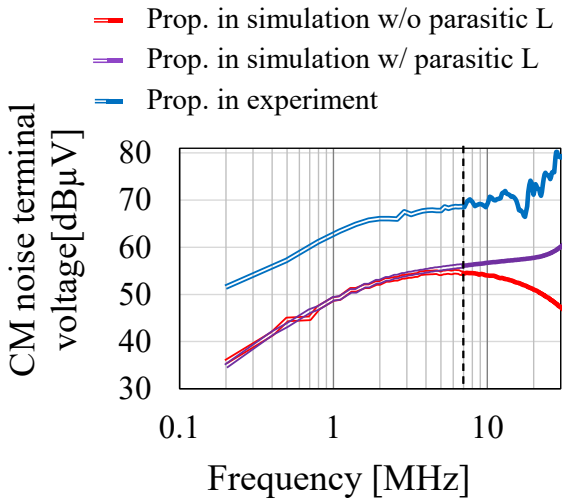


Fig. 4-17. The envelopes of the CM noise of proposed circuit in the simulation and experiment.

7 MHz. The envelopes of less than 7 MHz are drawn in double lines. First, C_{s_prop} was dominating in the propagation path of less than 7 MHz in each case because the influence of the parasitic inductance is ignored at lower frequencies. Thus, C_{s_prop} decides the amplitude of the CM noise. However, the amplitude of the CM noise was 20 dB larger than that in the experiment. Therefore, the experimental circuit had a larger C_{s_prop} than the simulation. Consequently, it is considered that the extracted C_{s_prop} is not accurate or additional CM capacitances exist but are not considered in the simulation.

Next, the envelopes of more than 7 MHz are drawn in single lines. The simulation result without considering the parasitic inductance decreased, whereas the simulation result by considering the parasitic inductance and the experimental result increased as the frequency increased. Thus, the parasitic capacitances are considered to increase the CM noise at higher frequencies. The CM noise in the conventional circuit should have also increased if the resonance, including C_{d_conv} or C_{s_prop} and parasitic inductances, amplifies the CM noise. However, the parasitic inductances did not increase the CM noise in the conventional circuit, as shown in Fig. 4-15 (a). Therefore, the increasing CM noise at a frequency of more than 7 MHz was supposed to be a superposition rather than an amplification. The increasing noise may have another propagation path such as a mixed-mode noise path, through which the noise propagates via interactions between the CM and DM noise. Consequently, the increasing noise at a frequency of more than 7MHz in the proposed circuit was considered to be superposed noise from another propagation path such as mixed-mode noise. Therefore, the C_{s_prop} error and the influence of the parasitic inductances on the CM noise must be investigated in future studies.

4.6. Discussion

The reversed circuit configuration was verified to reduce the CM noise in the simulation and experiment. Several conditions were set to precisely compare the CM noise. In this section,

the conditions where the reversed circuit configuration is adequate are discussed.

4.6.1. MOSFET Structure

The reversed circuit configuration decreases the CM noise by avoiding assigning the switching node to the terminal whose corresponding CM capacitance is large. The switching node was assigned to the source terminal in the proposed circuit because the drain terminal is connected to the thermal pad and has a large corresponding CM capacitance in the vertical MOSFET.

In other words, if the source terminal is connected to the thermal pad instead of the drain terminal, the CM capacitance corresponding to the switching node of the conventional circuit is already minimized. In this condition, the reversed circuit configuration will increase the CM noise. Additionally, even though the drain terminal has a large corresponding CM capacitance, the source terminal of a MOSFET acts as the switching node in a non-isolated buck DC–DC converter. The non-isolated buck DC–DC converter is shown in Fig. 4-18 (a). In the reversed circuit configuration of the buck converter, shown in Fig. 4-18 (b), the drain terminal of the MOSFET is assigned to the switching node. Therefore, in the case of the buck converter, the reversed circuit configuration is expected to increase the CM noise.

Consequently, the CM noise reduction effect of the reversed circuit configuration depends on the MOSFET structure and the circuit structure.

4.6.2. CM Capacitance Corresponding to the Diode

In the implementation process, the diodes in the experimental circuits were implemented on the top surface of the PCB to avoid the CM capacitance corresponding to the diodes. However, a diode is also typically placed on a heat sink for practical use for efficient performance. Therefore, a diode influences the CM capacitance. However, unlike a MOSFET chip, a diode chip has one terminal on each surface. Thus, there is a slight technical difficulty in changing the terminal

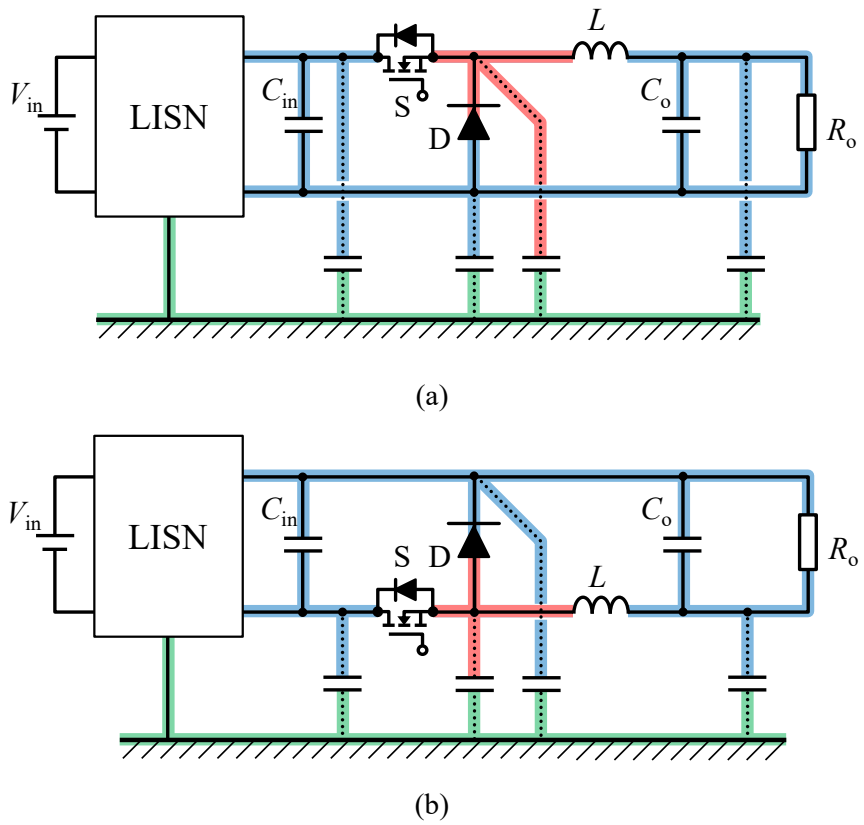


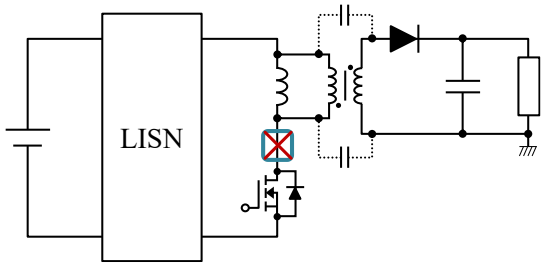
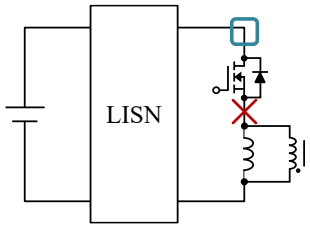
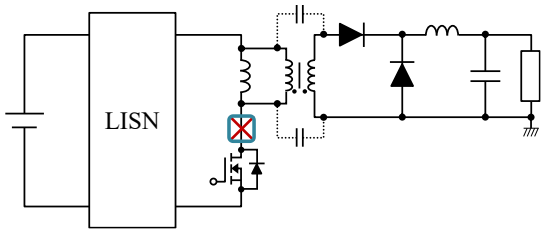
Fig. 4-18. Non-isolated buck DC-DC converter in (a) conventional circuit configuration and (b) reversed circuit configuration.

connected to the thermal pad. Therefore, the terminal connected to the thermal pad is supposed to be selectable. The CM capacitance corresponding to the switching node can be minimized, even though the diode influences the CM capacitance.

4.6.3. Reversed Circuit Configuration in Other Circuit Configurations

The non-isolated boost DC–DC converter is discussed in the previous sections. Here, the versatility of the reversed circuit configuration in other circuit configurations is discussed. The forward converter and the flyback converter are shown in Table 4-8. In the circuit diagrams, a blue square indicates a terminal connected to a thermal pad, and a red cross indicates a switching node. The primary side of each converter is reversed to separate the thermal pad and the switching

Table 4-8. Isolated buck DC-DC converters with reversed circuit configurations.

	Conventional	Reversed circuit configuration (Primary side)
Forward converter		
Flyback converter		

▢: Thermal pad, ✕: Switching node

node and to reduce the CM capacitance. However, as shown in conventional circuits, the interwinding capacitances exist between the primary and secondary sides of the circuits and, typically, the secondary sides are not isolated from the ground in low output voltage applications. Therefore, the interwinding capacitances also act as a CM noise propagation path. Thus, the interwinding capacitance of the transformer should be decreased to decrease the CM noise.

4.7. Conclusion

In this chapter, the reversed circuit configuration for CM noise reduction was proposed. First, the CM noise in the conventional and proposed circuits was analyzed, and the CM noise reduction mechanism was mathematically explained. Second, the circuit implementation procedure for proper experimental verification was explained. The circuit simulation and experiment were conducted, and the CM noise reduction effect of the reversed circuit configuration was verified. Finally, the detailed conditions in which the reversed circuit

configuration effectively reduces CM noise were discussed. In addition, reversed circuit configurations for configurations other than non-isolated DC–DC converters were discussed. The characteristics of CM noise reduction with the reversed circuit configuration are summarized in Table 4-9.

In conclusion, the ability of the proposed circuit configuration to reduce the CM noise in a non-isolated boost DC–DC converter without changing the circuit components and increasing the volume and weight was verified.

Table 4-9. Characteristics of proposed CM noise reduction methods.

	Strong points	Weak points
CHAPTER 4 Reversed configuration	- No increase in volume & weight - No change in circuit components	- Not for MOSFETs with thermal pad connected to source terminals. - Thermal pads of diodes are required to be selectable

CHAPTER 5: CM NOISE REDUCTION WITH THERMAL PAD ASSIGNMENT

5.1. Research Background

As discussed in the previous chapter, the CM capacitance corresponding to the switching node becomes a primal CM noise propagation path. Therefore, the reversed circuit configuration decreases the CM noise by changing the switching node but does not change the CM capacitance distribution. Therefore, in this chapter, a CM noise reduction method that changes the CM capacitance distribution to decrease the CM capacitance corresponding to the switching node is discussed.

5.2. Parasitic Capacitance and CM noise

5.2.1. Circuit Structure

In this chapter, the investigation was conducted in a non-isolated bidirectional DC–DC converter configuration shown in Fig. 5-1. The input voltage source is V_{in}, the input capacitance is C_{in}, the power inductor is L, the output capacitor is C_o, and the resistive load is R_o. The upper and lower arm switching devices are S_1 and S_2, respectively. LISN is inserted into the input side of the DC–DC converter to measure the CM noise. The DC–DC converter is isolated from the

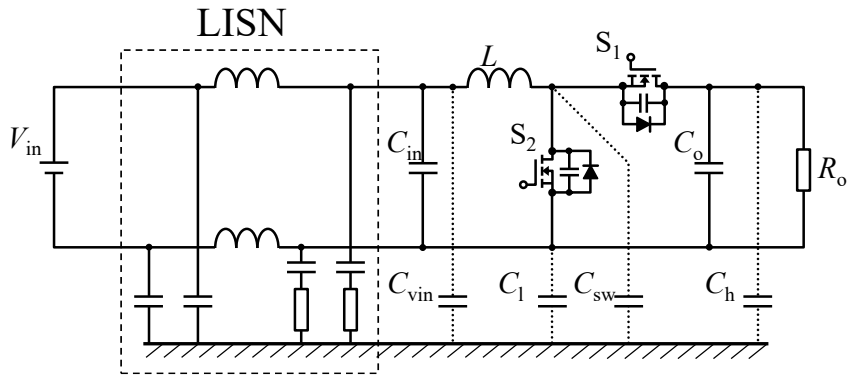


Fig. 5-1. Non-isolated bidirectional DC-DC converter.

ground, as shown in Fig. 5-1.

The CM capacitances are distributed in the overall circuit. In the circuit diagram, distributed CM capacitances are illustrated as CM capacitances distributed to each node in the DC–DC converter. Therefore, the CM capacitance is distributed in four capacitances corresponding to each node: C_{vin}, C_h, C_{sw}, and C_l. C_{vin} corresponds to one of the input terminals with a high voltage potential; C_h corresponds to the high voltage DC node of the half-bridge, which consists of S_1 and S_2; C_{sw} corresponds to the switching node; and C_l corresponds to a low voltage DC node of the half-bridge, respectively. The four CM capacitances strongly depend on the structure of the PCB patterns, the ground plane, and the switching devices. The package structure of the switching devices and PCB patterns around the switching device influence the C_h, C_{sw}, and C_l because these capacitances are connected to the switching devices.

5.2.2. CM Noise Analysis

The relationship between the CM noise and the distribution of CM capacitances is mathematically analyzed. The CM noise equivalent circuit for analysis is derived from the investigation circuit shown in Fig. 5-1. The CM noise equivalent circuit of the investigation circuit is shown in Fig. 5-2. As in the procedure to convert the circuit structure, the input capacitance C_{in} and output capacitance C_o are sufficiently large and assumed to be short. The inductor L, however, is sufficiently large and assumed to be open. The noise voltage source $V_{noise}(\omega)$, a function of

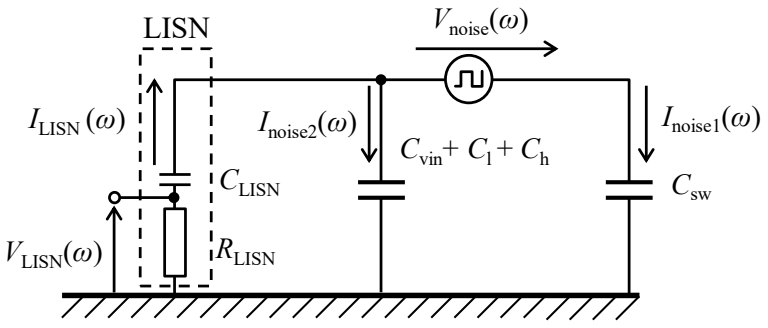


Fig. 5-2. CM noise equivalent circuit of the investigation circuit.

noise angular frequency ω, represents MOSFETs S_1 and S_2. The series connection of the resistance R_{LISN} and the capacitance C_{LISN} represents the simplified structure of LISN. The capacitances C_{vin}, C_h, and C_{sw} are connected in parallel, whereas C_l is connected to $V_{noise}(\omega)$ in series. The CM noise terminal voltage is $V_{LISN}(\omega)$. The current that flows through C_l is $I_{noise1}(\omega)$, whereas the total current propagates through C_{vin}, C_h, and C_{sw} is $I_{noise2}(\omega)$. The current that flows through the LISN is $I_{LISN}(\omega)$. The following circuit equations are acquired from Fig. 5-2:

$$\begin{cases} V_{noise}(\omega) = \frac{I_{noise1}(\omega)}{j\omega C_{sw}} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN}(\omega) \\ 0 = \frac{I_{noise2}(\omega)}{j\omega(C_{vin} + C_h + C_l)} + \left(\frac{1}{j\omega C_{LISN}} + R_{LISN}\right) I_{LISN}(\omega) \\ V_{LISN}(\omega) = -R_{LISN} I_{LISN}(\omega) \\ I_{LISN}(\omega) = I_{noise1}(\omega) + I_{noise2}(\omega) \end{cases} \quad \cdots\cdots (5\text{-}1)$$

From (5-1), $V_{LISN}(\omega)$ in the following equation is derived:

$$V_{LISN}(\omega) = -\frac{j\omega C_{LISN} R_{LISN} V_{noise}(\omega)}{\left(1 + \frac{C_{LISN}}{C_{all}}\right) + j\omega C_{LISN} R_{LISN}} \frac{C_{sw}}{C_{all}} \quad \cdots\cdots (5\text{-}2)$$

, where C_{all} in the following equation is the total of the distributed CM capacitance:

$$C_{all} = C_{vin} + C_h + C_{sw} + C_l \quad \cdots\cdots (5\text{-}3)$$

For analyzing the influence of the CM capacitance on CM noise, two non-isolated DC–DC converters are hypothesized to exist for comparison: circuits A and B. The CM noise terminal voltage in each circuit is expressed as follows:

$$\begin{cases} V_{LISN\_A}(\omega) = -\frac{j\omega C_{LISN} R_{LISN} V_{noise}(\omega)}{\left(1 + \frac{C_{LISN}}{C_{all}}\right) + j\omega C_{LISN} R_{LISN}} \frac{C_{sw\_A}}{C_{all}} \\ V_{LISN\_B}(\omega) = -\frac{j\omega C_{LISN} R_{LISN} V_{noise}(\omega)}{\left(1 + \frac{C_{LISN}}{C_{all}}\right) + j\omega C_{LISN} R_{LISN}} \frac{C_{sw\_B}}{C_{all}} \end{cases} \quad \cdots\cdots (5\text{-}4)$$

Here, the CM noise terminal voltage is $V_{LISN\_A}(\omega)$ in circuit A, whereas it is $V_{LISN\_B}(\omega)$ in circuit B. Circuit A is assumed to have the CM capacitance C_{sw_A} that corresponds to the switching node instead of C_{sw}, whereas the circuit B is assumed to have C_{sw_B} instead of C_{sw}. The total CM capacitance C_{all} and the noise voltage source $V_{noise}(\omega)$ are assumed to be the same in circuits A and B. From (5-4), the ratio of $V_{LISN\_A}(\omega)$ to $V_{LISN\_B}(\omega)$ is expressed as follows:

$$\frac{V_{\mathrm{LISN\_A}}(\omega)}{V_{\mathrm{LISN\_B}}(\omega)} = \frac{C_{\mathrm{sw\_A}}}{C_{\mathrm{sw\_B}}} \quad (5\text{-}5)$$

From (5-5), it is found that the CM noise voltage $V_{\mathrm{LISN}}(\omega)$ depends on C_{sw} and changes even if the noise voltage source $V_{\mathrm{noise}}(\omega)$ and the total CM capacitance C_{all} are constant. Therefore, the CM noise strongly depends on the distribution of the CM capacitances. This dependency of CM noise on the distribution of the CM capacitance has not been investigated experimentally in the previous research. Thus, the influence of the distribution of CM capacitances on CM noise is investigated in the subsequent sections.

5.3. Investigation Method

Previous sections showed that the distribution of CM capacitances significantly influences the CM noise terminal voltage. The noise voltage source $V_{\mathrm{noise}}(\omega)$ and the total CM capacitance C_{all} should be set to be constant to simplify the comparison. Based on this condition, the CM noise should be compared with different combinations of values of C_{vin}, C_{h}, C_{sw}, and C_{l} to investigate the influence of the distributed CM capacitance on CM noise. Herein, the switching devices for investigation and the implementation procedure for the experimental circuit are discussed before conducting investigations in the simulation and measurement.

5.3.1. Devices for Investigation

In the investigation, two switching devices are used for S_1 and S_2 to achieve the desired CM capacitance distribution: TP65H070LDG and TP65H070LSG. These devices are cascode-type GaNFET manufactured by Transphorm, each consisting of a low-voltage silicon MOSFET for gate drive and a high-voltage GaN HEMT. These devices have the same characteristics, including the voltage rating, current rating, parasitic capacitance, rise time, and fall time, but differ in footprint. The footprint on the bottom surface of TP65H070LDG and TP65H070LSG are shown in Fig. 5-3 (a) and (b), respectively. One large thermal pad and two small pads exist on the bottom surface of each switching device. Each thermal pad has the same area, whereas the area

Fig. 5-3. Bottom views of (a) TP65H070LDG and (b) TP65H070LSG.

of each pair of small pads slightly differs.

Furthermore, these two devices are different in terms of terminal assignment. The thermal pad and drain terminal are connected, whereas the other two small pads are connected to the source and gate terminals in TP65H070LDG, shown in Fig. 5-3 (a). By contrast, the thermal pad and source terminal are connected, whereas the other two small pads are connected to the drain and gate terminals in TP65H070LSG, shown in Fig. 5-3 (b). Therefore, the CM capacitance distribution corresponding to the switching device differs between these two devices because of differently assigned terminals, even though these devices have the same characteristics electrically and thermally, and the noise voltage source $V_{\mathrm{noise}}(\omega)$ remains the same. Here, TP65H070LDG and TP65H070LSG have the same package size. Thus, the total volume and weight of the circuits are the same, even though each circuit has a different combination of switching devices.

The cross section of a device on the PCB is shown in Fig. 5-4, which was to analyze the CM capacitance. Double-sided PCBs are used for implementation. A MOSFET was placed on the top surface of the PCB, whereas the insulation sheet and the heat sink were placed on the bottom surface for heat dissipation. The thermal pattern on the bottom surface of the PCB and MOSFET and the thermal pattern is connected electronically and thermally through the thermal vias for

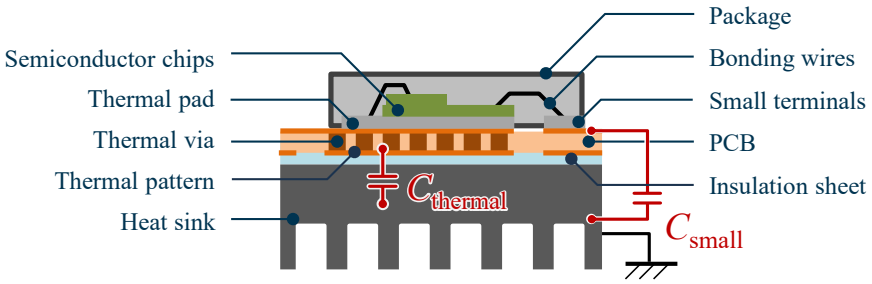


Fig. 5-4. Cross-section of a switching device, a PCB, an insulation sheet, and a heat sink combined.

efficient thermal dissipation. The thermal patterns should be designed to be sufficiently large on the bottom surface and placed close to the heat sink. The heat sink is connected to the ground. Thus, the terminal assigned to the thermal pad necessarily has a large CM capacitance. In this chapter, this CM capacitance corresponding to the thermal pad is defined as $C_{thermal}$.

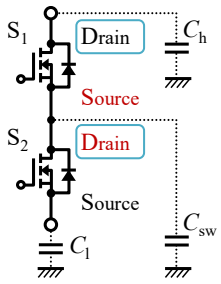
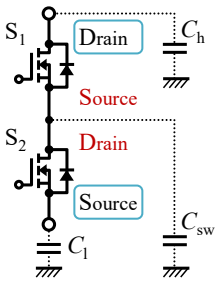
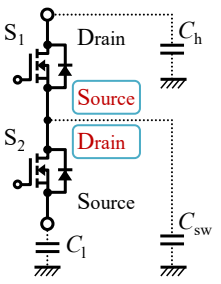
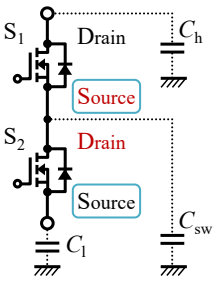
The two small pads other than the thermal pad have a negligible influence on heat dissipation. Thus, the thermal patterns on the bottom surface of the PCB are not necessarily connected to these small pads. Therefore, the PCB pattern design can minimize the CM capacitance corresponding to these two small pads. In this chapter, this CM capacitance is defined as C_{small}. Consequently, the CM capacitance $C_{thermal}$ naturally becomes much larger than C_{small} when C_{small} is minimized to decrease the CM noise. Here, the CM capacitance corresponding to the gate pad, a pad at the left bottom corner in Fig. 5-3 (a) and (b), is considered to be sufficiently small and ignored to simplify the analysis. The other CM capacitance except $C_{thermal}$s and C_{small}s is defined as C_{other}, which is assumed to be included in C_{vin}, C_h, or C_l in Fig. 5-1 and strongly depends on the PCB design other than the thermal pattern. $C_{thermal}$ and C_{small} are also indicated in Fig. 5-4. $C_{thermal}$s, C_{small}s, and C_{other} change depending on the circuit patterns and are distributed to C_{vin}, C_h, C_{sw}, and C_l. The relationships between the different CM capacitances are expressed as follows:

$$C_{all} = C_{vin} + C_h + C_{sw} + C_l = 2C_{thermal} + 2C_{small} + C_{other} \quad \cdots\cdots (5\text{-}6)$$

As explained in the previous sections, the distribution of the CM capacitance, especially C_{sw}, is essential when discussing the CM noise. Therefore, in this section, the relationship between the CM capacitance and the combinations of the switching devices implemented is discussed. There are two types of MOSFETs to be implemented: TP65H070LDG and TP65H070LSG, and an investigation circuit needs two switching devices S_1 and S_2. Thus, four combinations of FETs are possible. Four circuit diagrams of the half-bridge with all combinations of switching devices are presented in Table 5-1. A thermal pad is indicated by a blue square, and a terminal connected to the switching node is indicated by red letters.

Additionally, the distribution of the CM capacitance in each case is presented in Table 5-1 as well. $C_{vin} + C_h + C_l$ includes C_{other} in each case. $C_{thermal}$ is designed the same so that heat is dissipated equally in each case. Neither of the thermal pads in S_1 and S_2 is connected to the

Table 5-1. Parasitic capacitance and combinations of FETs.

		Case 1	Case 2	Case 3	Case 4
Circuit diagram of half-bridge					
Thermal pad	S_1	Drain	Drain	Source	Source
	S_2	Drain	Source	Drain	Source
C_{sw}		$C_{thermal} + C_{small}$	$2C_{small}$	$2C_{thermal}$	$C_{thermal} + C_{small}$
$C_{vin} + C_h + C_l$		$C_{thermal} + C_{small} + C_{other}$	$2C_{thermal} + C_{other}$	$2C_{small} + C_{other}$	$C_{thermal} + C_{small} + C_{other}$
C_{all}		$2C_{thermal} + 2C_{small} + C_{other}$			

*□: a thermal pad

switching node in case 2, shown in Table 5-1. Thus, C_{sw} omits $C_{thermal}$ and becomes the smallest among all cases.

However, the switching node and both thermal pads are connected in case 3. Therefore, C_{sw} becomes the largest among all cases. Furthermore, one thermal pad is connected, and the other is not connected to the switching node in cases 1 and 4. Thus C_{sw} becomes the same in cases 1 and 4. The implementation method to achieve the above-explained conditions in all cases of device combinations is discussed in the next section.

5.3.2. Circuit Implementation

The distribution of CM capacitances should be carefully designed to compare the CM noise properly. In this section, the circuit implementation procedures are explained.

The cross section of an experimental circuit is illustrated in Fig. 5-5. The MOSFETs S_1 and S_2 are mounted on the top surface of the PCB. Thus, thermal vias are necessary to dissipate the heat generated in S_1 and S_2 through the thermal pattern and heat sink. Therefore, the thermal patterns on the bottom surface of the PCB are designed to have equal areas for equal heat dissipation, resulting in equal $C_{thermal}$. The bottom surface designs of the PCBs for all cases are illustrated in Fig. 5-6 (a) to (d). All bottom surfaces shown in Fig. 5-6 are the same in form and size. The size of each PCB is 81.6 × 70.9 × 1.60 mm. Each bottom surface consists of three patterns, and two of these patterns are thermal patterns that are connected to the thermal pads of S_1 and S_2, as shown in Fig. 5-6. The thermal pattern is designed to have the same area such that

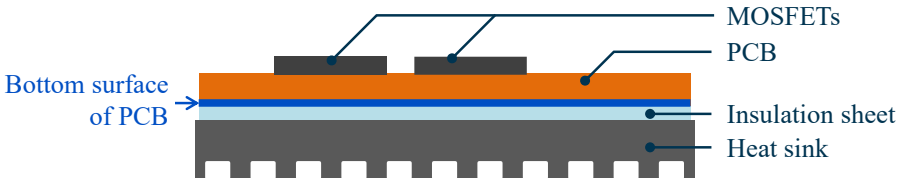


Fig. 5-5. Cross-section of an experimental circuit.

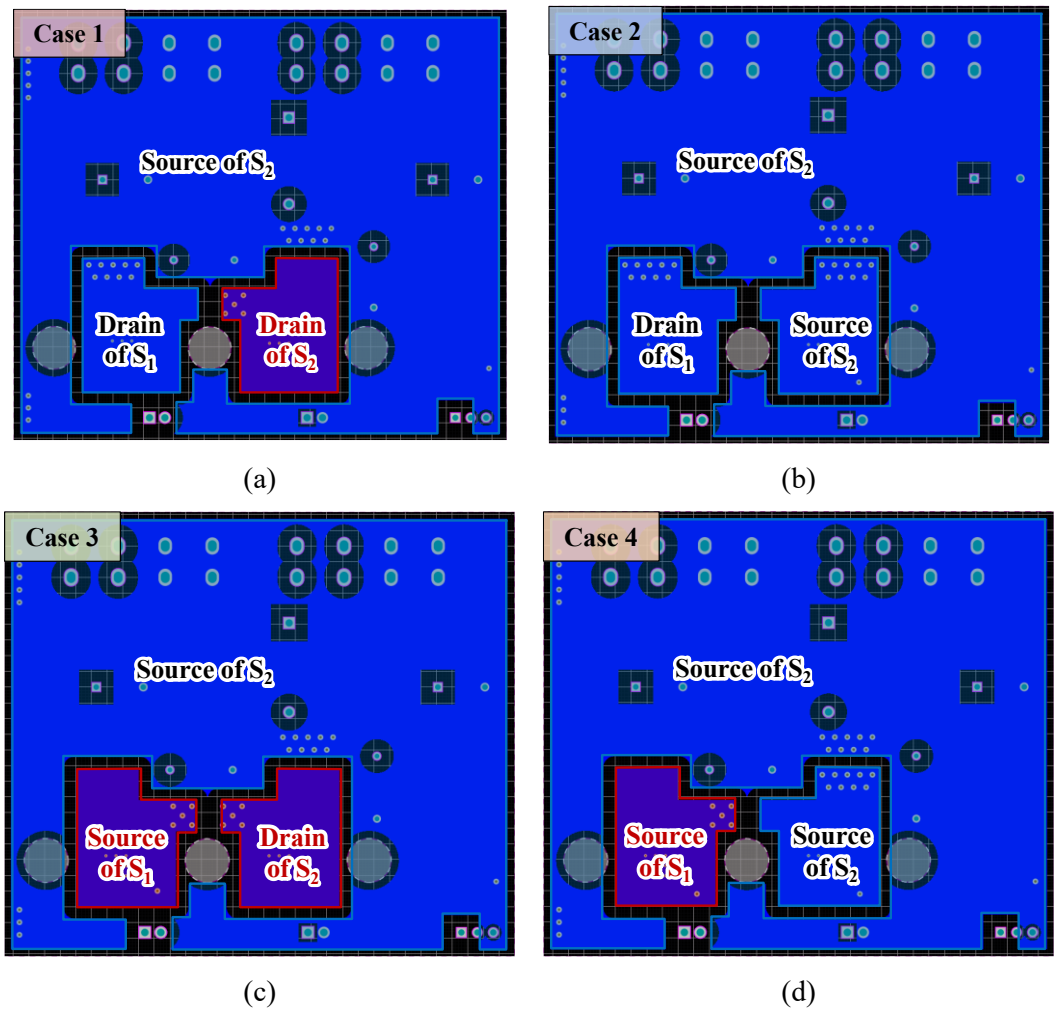


Fig. 5-6. Bottom circuit patterns of experimental circuits with different device combinations: (a) case 1, (b) case 2, (c) case 3, and (d) case 4.

S_1 and S_2 achieve equal heat dissipation. In Fig. 5-6, the red line indicates a thermal pattern on the bottom surface connected to the switching node. The PCB pattern, other than the thermal patterns that occupy a large part of the bottom surface, is connected to the source terminal of S_2. This pattern corresponds to C_l, which is dominant in C_{all} of each experimental circuit. In Fig. 5-6 (b), none of the thermal patterns and the switching node are connected. In Fig. 5-6 (c), both thermal patterns and the switching node are connected. In Fig. 5-6 (a) and (d), only one thermal pad is connected to the switching node. These structures are indicated in Table 5-1. Therefore, the

PCB design implements the circuit structure that achieves the conditions for appropriate comparison discussed in Table 5-1. With these PCB circuits, the changes in CM noise should depend only on C_{sw} because the bottom PCB patterns were designed to have the same form and size, and C_{all} should remain the same among all experimental circuits.

A PCB, an insulation sheet, and a heat sink were screwed together in the assembling process of an experimental circuit. Polycarbonate screws were utilized to fix the components instead of metal screws to avoid additional EMI through the metal screws. An experimental circuit is shown in Fig. 5-7. This circuit needed three screws to fix the components. The torque driver tightened these screws to equalize the torque on all screws in the experimental circuit. Here, because FETs have the same electric characteristics that result in the same $V_{noise}(\omega)$ and C_{all} is the same among experimental circuits, the CM noise results in the simulation described below and differences in the measurement depend only on the distribution of the CM capacitances.

5.4. Simulation

In this section, the CM noise terminal voltage was simulated with each combination of switching devices and compared. Before the circuit simulation, FEM simulation was conducted

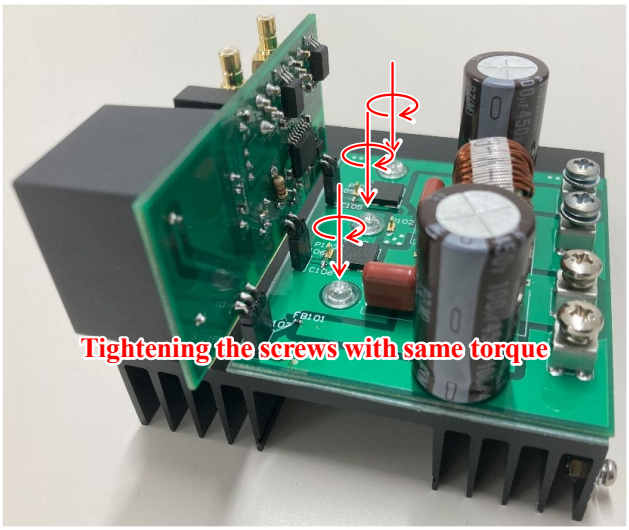


Fig. 5-7. Polycarbonate screws in an experimental circuit.

to extract the CM capacitances distributed in each experimental circuit.

5.4.1. CM capacitance extraction

The CM capacitances in the circuit simulation were set to the values that reflect the actual circuit's CM capacitances. However, although C_{all} can be measured, C_{vin}, C_h, C_{sw}, and C_l are difficult to measure in the experimental circuit. Therefore, the 3D models, each consisting of a PCB, an insulation sheet, and a heat sink, were created in ANSYS Q3D to extract each CM capacitance distributed in the experimental circuits. The circuit elements were not included in the 3D model because all the circuit elements were placed on the top surface of a PCB, and the CM capacitances were supposed to depend strongly on the PCB, not the circuit elements. As an example, the 3D model of the circuit for case 1 created in ANSYS Q3D is shown in Fig. 5-8. The insulation sheet utilized for the experimental circuit was made of soft material, and the thickness is unknown when the PCB and heat sink pressed it. Therefore, the thickness of each insulation sheet was set such that the measurement results described later, and the extraction results of C_{all} show small errors. The extraction results of the CM capacitances are shown in Fig. 5-9. In Fig. 5-9, cases 1 and 4 showed relative values of C_{sw}, whereas case 3 showed a considerably larger $C_{sw,}$

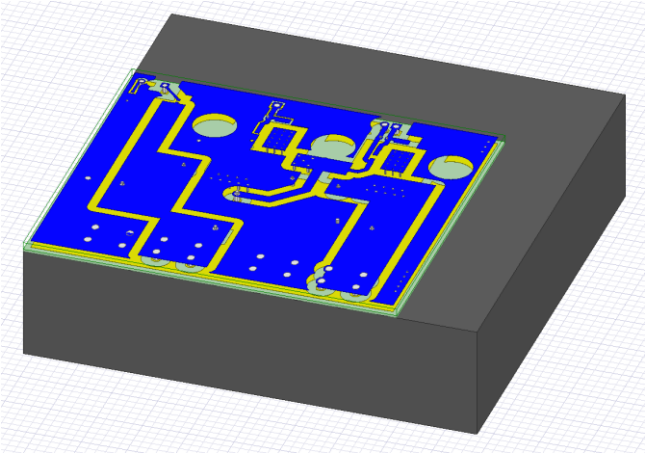


Fig. 5-8. 3D model of the experimental circuit for case 1.

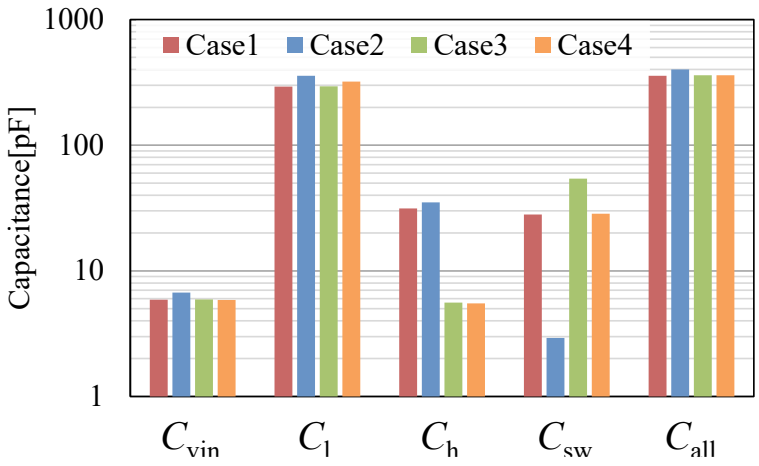


Fig. 5-9. CM capacitances extracted by ANSYS Q3D.

and case 2 showed a significantly smaller C_{sw}, as discussed in Table 5-1.

The total CM capacitance C_{all} had the error within 11% among all cases as designed. C_l was dominant in C_{all} in each case because the corresponding PCB pattern connected to the source terminal of S_2 occupied a large part of the bottom surface in each of the experimental circuits, as shown in Fig. 5-6. C_{all} was measured in the experimental circuits and compared with the extracted values to verify the consistency of the values extracted. The circuit connection for the measurement is shown in Fig. 5-10. In Fig. 5-10, all nodes in the experimental circuit were shorted to measure C_{all}. The capacitance between the shorted node terminal, indicated in red, and the ground is measured as C_{all}. The impedance analyzer E4990A manufactured by Keysight Technologies was utilized for capacitance measurements. The C_{all} values from the extraction and measurement are compared in Table 5-2. The errors in C_{all} were within 13.2% in all cases. These extracted CM capacitance values were employed in the circuit simulation described below.

5.4.2. CM noise analysis in Circuit Simulation

The CM noise terminal voltages in all cases in Table 5-1 were compared in the circuit simulation. The conditions for the investigation are presented in Table 5-3. The circuit simulation

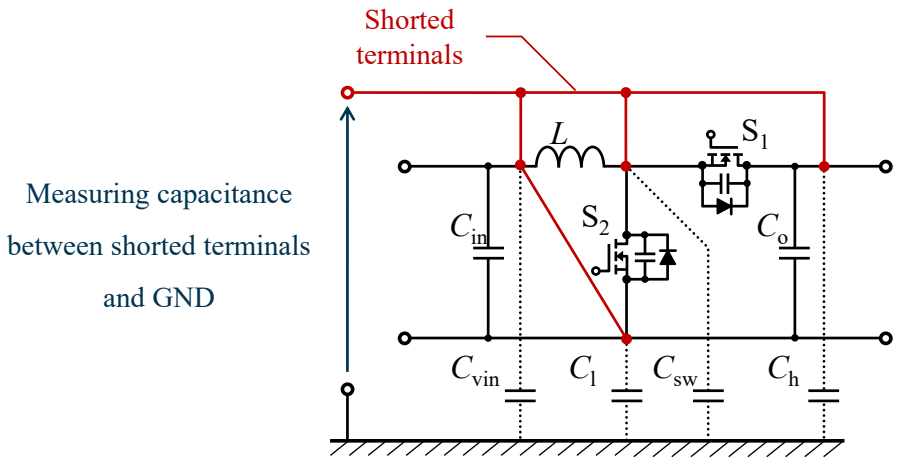


Fig. 5-10. Circuit connection to measure C_{all}.

Table 5-2. Comparison of total CM capacitance C_{all} in the simulation and measured.

		Case 1	Case 2	Case 3	Case 4
C_{all} [pF]	Simulation	358	401	360	360
	Measurement	397	355	394	396
	Error [%]	-9.8	13.2	-8.53	-9.11

Table 5-3. Parameters for investigation.

Parameter	Value
Input voltage	160 V
Output voltage	240 V
Input power	524 W
Switching frequency	100 kHz
Duty ratio	0.333
R_{LISN}	25 Ω
C_{LISN}	0.2 μF

was conducted in the circuit simulator PLECS. The drain-source voltage of an ideal MOSFET corresponded to $V_{noise}(\omega)$ among all cases in the circuit simulation. In the circuit simulation, the CM capacitance originating from the input cable between the PCB and LISN was considered and resulted in an additional 155 pF capacitance included in each of C_{vin} and C_l. The simulation results are shown in Fig. 5-11. As discussed in Sections 5.3.1 and 5.3.2, the CM noise terminal voltages

showed extremely close envelopes in cases 1 and 4.

By contrast, the envelope in case 3 was approximately 6 dB higher than those in cases 1 and 4, and the envelope in case 2 was approximately 20 dB lower than those in cases 1 and 4. The difference among the simulation results shown in Fig. 5-11 reflects the difference among C_{sw} shown in Fig. 5-9, whereas C_{all} and $V_{noise}(\omega)$ are shared among all cases. Thus, the simulation results indicated that the changes in the CM noise terminal voltage significantly depend on C_{sw}, even though C_{all} and $V_{noise}(\omega)$ do not change.

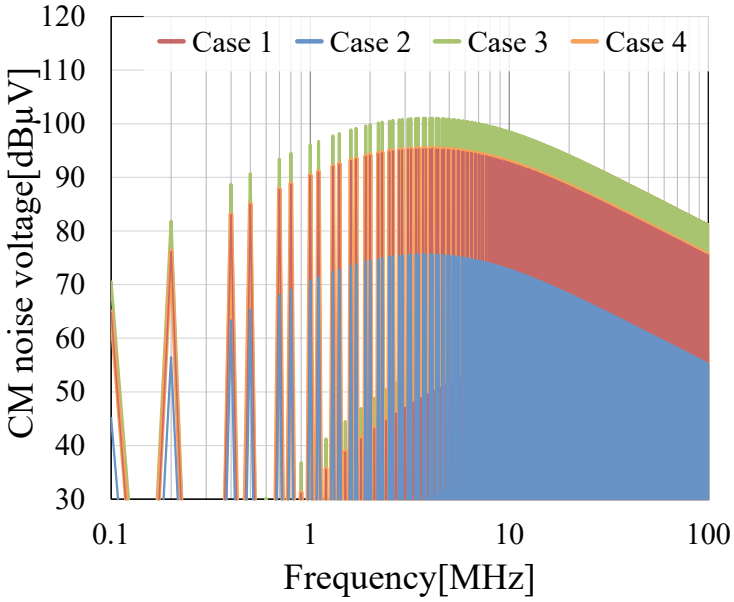


Fig. 5-11. CM noise terminal voltages in simulation.

5.5. Measurement

In this section, the CM noise terminal voltages were measured in the experimental circuit to evaluate the influence of C_{sw} on the CM noise in the experiment. The parameters in Table 5-3 were used in the measurement. The experimental circuits and environment are shown in Fig. 5-12 and Fig. 5-13, respectively. The measurement equipment is presented in Table 5-4. The

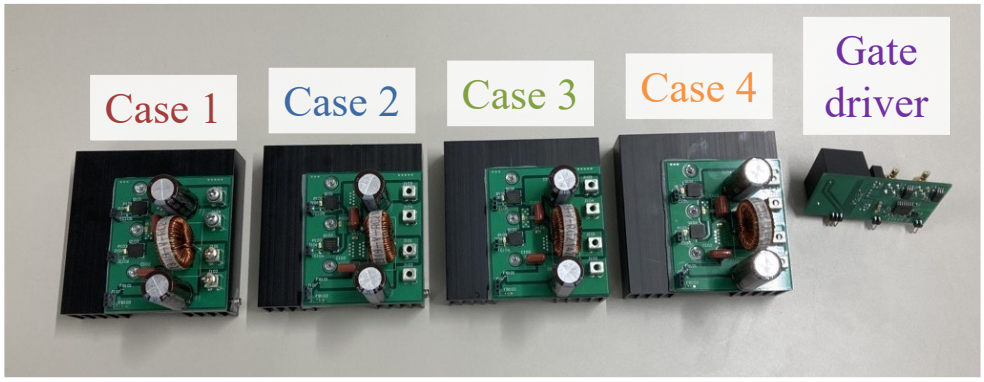


Fig. 5-12. Experimental circuits.

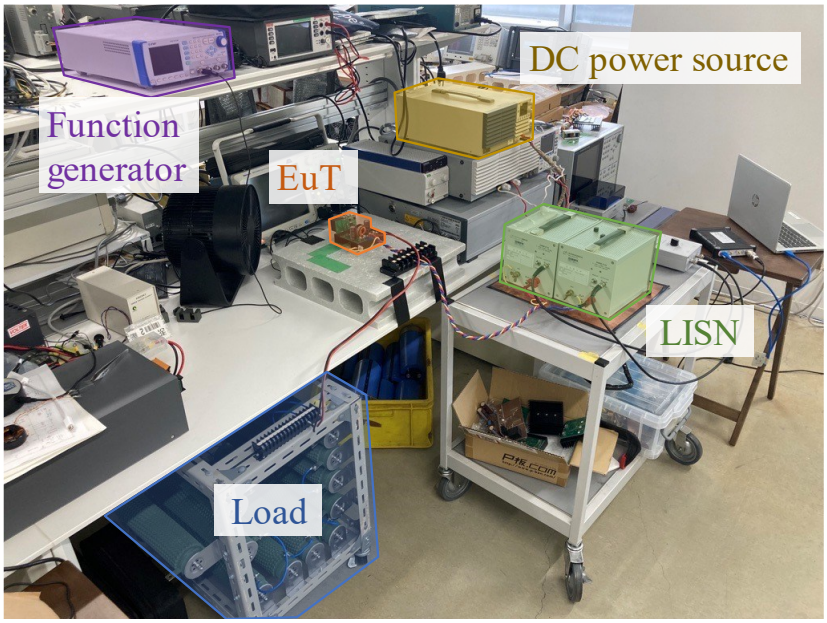


Fig. 5-13. Experimental environment.

measurement results are shown in Fig. 5-14 (a) to (d) and compared in Fig. 5-15. Here, the CM/DM switch CMDM 8700 B attenuated the input signal by 20 ± 3 dB when extracting the CM noise. Thus, the results shown in Fig. 5-14 and Fig. 5-15 were compensated based on the amount attenuated by CMDM 8700 B. In Fig. 5-15, case 3 showed the most significant CM noise terminal voltage, and case 2 showed the minimum CM terminal voltage.

By contrast, cases 1 and 4 showed the spectrum in the middle, similar to the simulation.

Table 5-4. Measurement equipment.

Instrument	Part number	Manufacturer
LISN	NNBM 8124	SCHWARZBECK
CM/DM switch	CMDM 8700 B	SCHWARZBECK
Spectrum analyzer	RSA306B	Tektronix

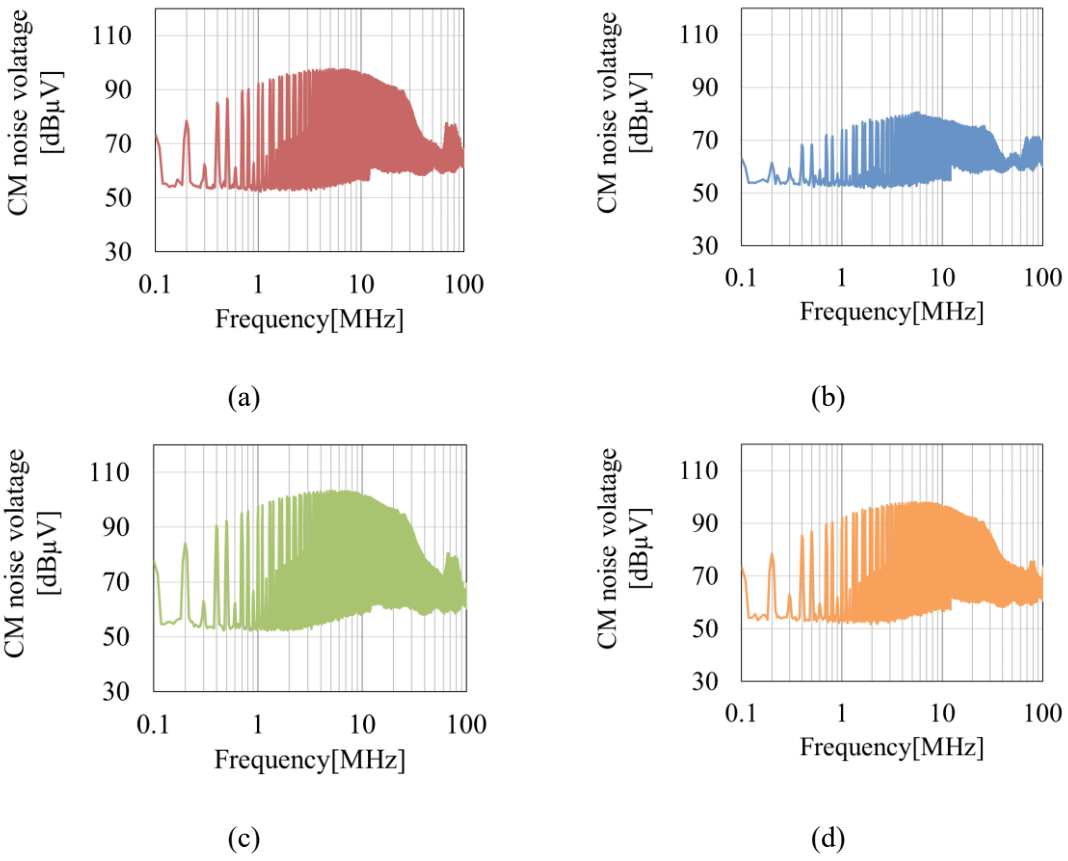


Fig. 5-14. Measured CM noise terminal voltages in (a) case 1, (b) case 2, (c) case 3, and (d) case 4.

There was a constant 20-dB difference between cases 2 and 3 at a frequency lower than 20 MHz. Cases 1 and 4 showed a noise level of 4 to 6 dB below that of case 3 at a frequency lower than 20 MHz. The relative difference in the CM noise terminal voltage among all the cases was similar

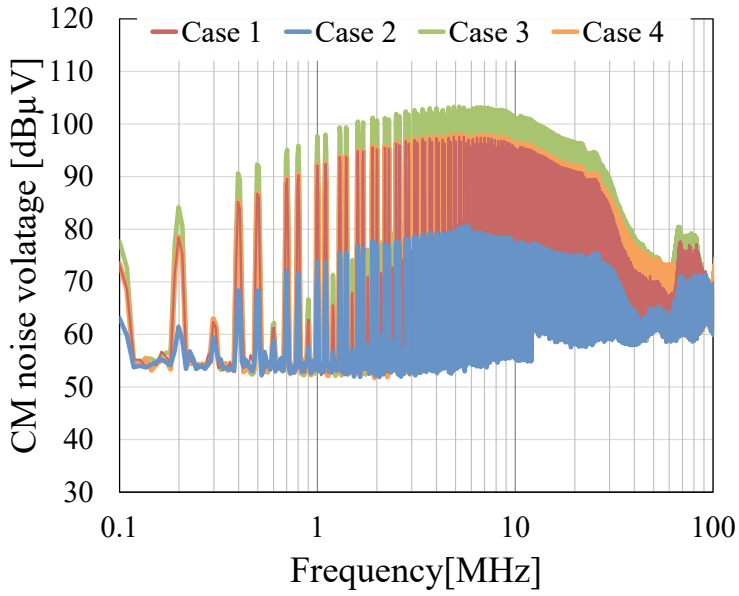


Fig. 5-15. Compared CM noise terminal voltages in measurement.

between the simulation and measurement results.

The envelope of the CM noise terminal voltage spectra in the measurement decreased more steeply than those in the simulation at a frequency higher than 30 MHz. The difference in the noise voltage source $V_{noise}(\omega)$ caused the difference in the CM noise terminal voltage at a high frequency between the simulation and measurement. The spectra of drain-source voltages in S_2 that acted as $V_{noise}(\omega)$ are shown in Fig. 5-16 (a), (b), (c), and (d). Additionally, all spectra are compared in Fig. 5-17. The spectra of drain-source voltages also decreased more steeply at a frequency higher than 30 MHz in measurement than those in simulation. Thus, the CM noise terminal voltage in the measurement decreased more steeply than that in the simulation because of the characteristics of the noise voltage source $V_{noise}(\omega)$ from (5-2) and Fig. 5-17. Consequently, the measurement results showed that the changes in the CM noise significantly depend on C_{sw} as shown in the simulation results.

Additionally, switching performance was evaluated in the experimental circuits. The efficiency of each experimental circuit is presented in Table 5-5. The waveforms of the drain-

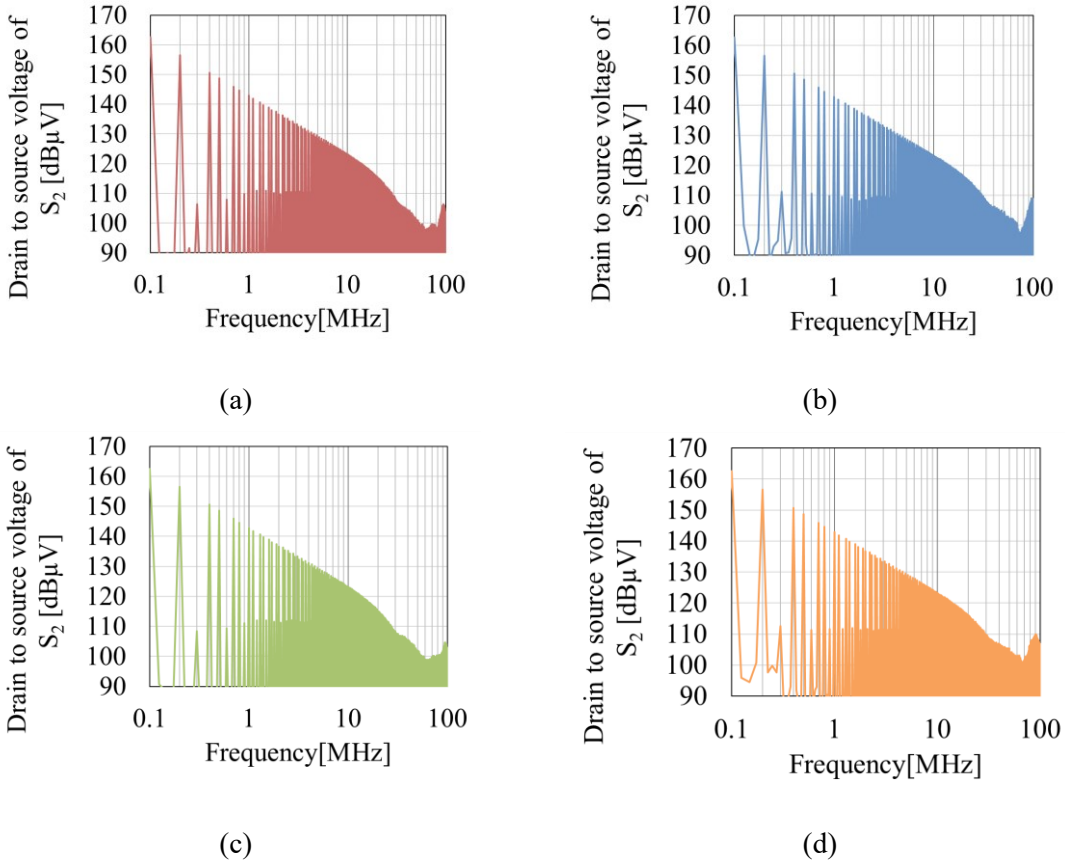


Fig. 5-16. Measured spectra of drain-source voltage of S_2 in (a) case 1, (b) case 2, (c) case 3, and (d) case 4.

source voltages are shown in Fig. 5-18. The conversion efficiency of each experimental circuit showed a small error in Table 5-5, and the drain-source voltage waveforms shown in Fig. 5-18 had similar *dv*/*dt* characteristics in all cases. The resonance in each waveform at turn-on and turn-off differed in amplitude, but the resonance was not supposed to significantly influence the efficiency. The resonant frequencies ranging from 80 MHz to 100 MHz appear as peaks in the spectra in Fig. 5-17. From Table 5-5 and Fig. 5-18, it was found that the efficiency is sufficiently close among the experimental circuits, and the efficiency is verified not to influence the CM noise terminal in the measurement.

5.6. Discussion

5.6.1. Other Implementation Methods to Decrease C_{sw}

In the previous sections, a specific combination of switching devices was found to decrease C_{sw}, which is the CM capacitance corresponding to the switching node, and to decrease the CM

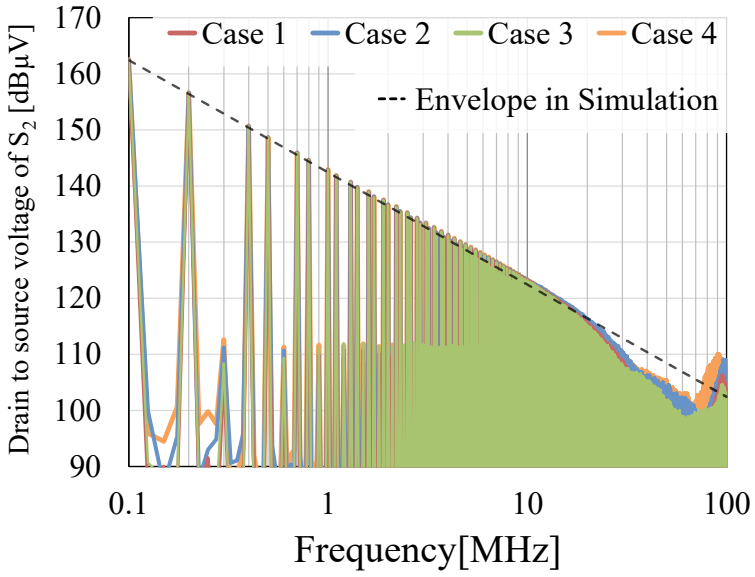


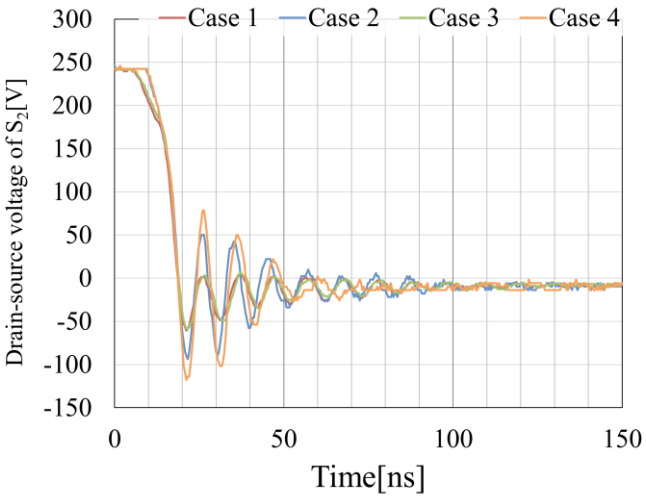
Fig. 5-17. Compared spectra in Fig. 5-16.

Table 5-5. Efficiency of experimental circuits.

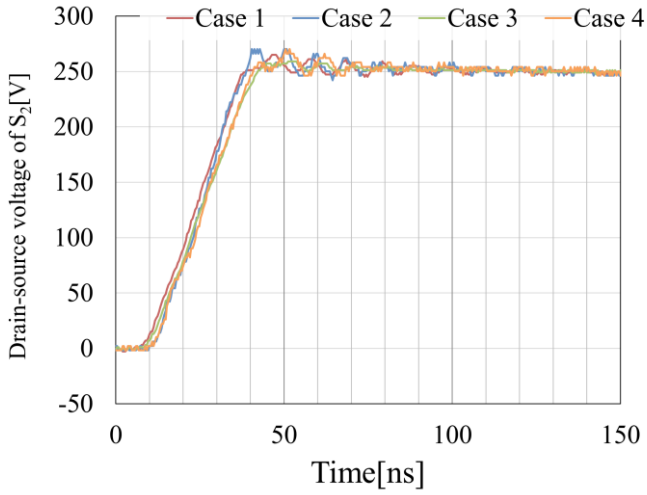
	Case 1	Case 2	Case 3	Case 4
Efficiency [%]	97.8	97.8	97.9	97.9

noise. Consequently, the distribution of CM capacitance significantly influences the CM noise. Therefore, in this section, the approaches to decrease the C_{sw} are discussed.

One method to design the CM capacitance is to utilize devices that employ selectable thermal pads, such as TP65H070LDG and TP65H070LSG, discussed in the previous sections. For example, GaN transistor GS66508P manufactured by GaN Systems Inc. has a floating thermal



(a)



(b)

Fig. 5-18. Drain-source voltage waveforms in S_2 at (a) turn-on and (b) turn-off.

pad initially insulated from the drain and source terminals. The bottom surface and the circuit symbol of GS66508P are shown in Fig. 5-19. The thermal pad is connected to the substrate internally but should be connected to the drain or source terminal externally. In [102], GS66508P was investigated in both operations with a thermal pad connected to the drain terminal and another thermal pad connected to the source terminal. Therefore, the CM noise should decrease when

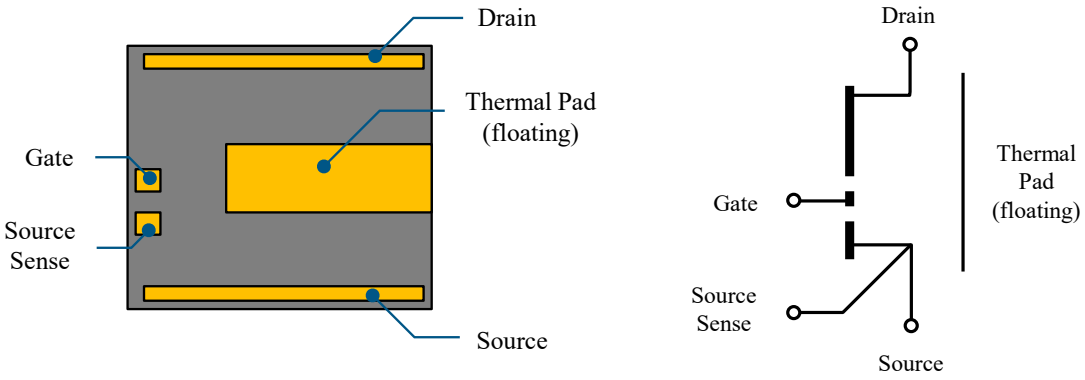


Fig. 5-19. GS66508P in (a) bottom surface of package and in (b) circuit symbol[102].

GS66508P is utilized with the appropriate connection of the thermal pad.

There is also a half-bridge module discussed in [103]. The module discussed in [103] is shown in Fig. 5-20. The module in Fig. 5-20 has a multi-layer structure, and the thermal pad was connected to the source terminal of the lower arm. Therefore, this module should reduce the CM noise as well.

Similarly, an IGBT half-bridge module structure to reduce the CM noise was proposed in [104]. The conventional and proposed modules are shown in Fig. 5-21. Each module consists of

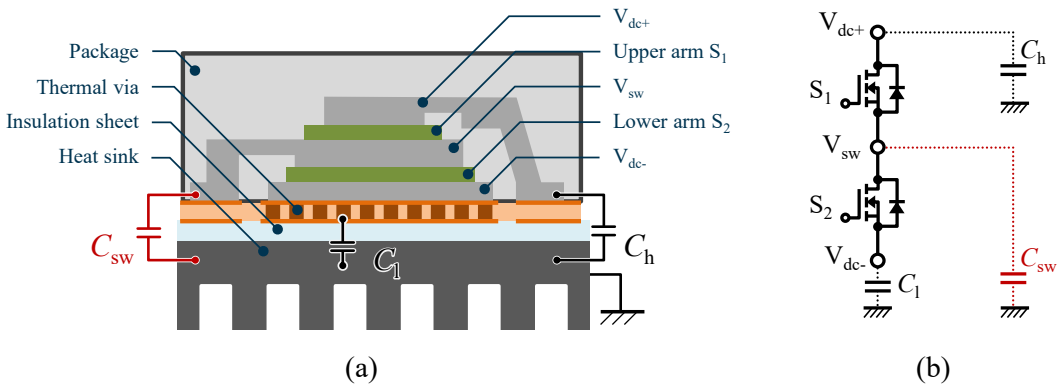


Fig. 5-20. Half-bridge module proposed in [103] in (a) cross section of the package and in (b) circuit diagram.

two IGBT chips. In the conventional module, each collector terminal faced toward the copper base. Therefore, there was an inevitable CM capacitance corresponding to the switching node because the lower arm's IGBT chip dissipates the heat from the collector terminal. However, the lower arm's IGBT chip was flipped in the proposed module structure. Thus, none of the emitter terminals of the upper arm and collector terminal of the lower arm faced toward the copper base to reduce the CM capacitance corresponding to the switching node. Consequently, this proposed module structure reduces the CM noise because of the reduced CM capacitance from the

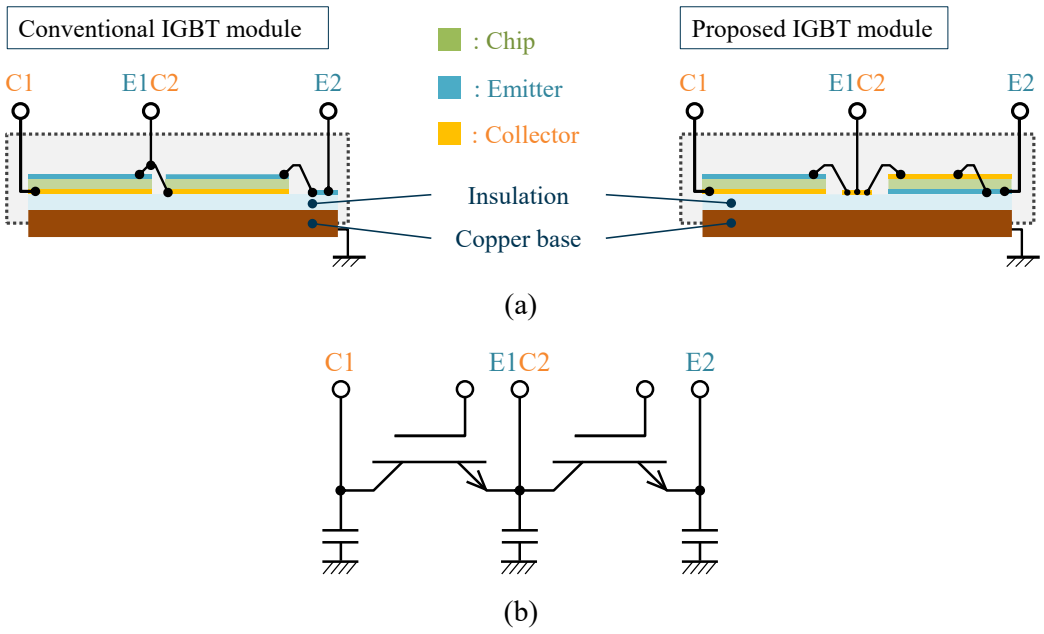


Fig. 5-21. The conventional and proposed IGBT modules in [104] in (a) cross sections of the modules and in (b) circuit diagram.

switching node.

5.6.2. CM Capacitance Reduction with Device Combinations in Other Circuit Configurations

The non-isolated boost DC–DC converter is discussed in the previous sections. Here, the

versatility of the CM capacitance reduction with device combinations in other circuit configurations is discussed.

The combination of devices with different thermal pads can reduce the CM noise in various circuit configurations as far as the noise current primally propagates the CM capacitance corresponding to the switching node. Several examples are shown in Fig. 5-22, and the half-bridge inverter is shown in Fig. 5-22 (a). The CM capacitance corresponding to the switching node in the half-bridge structure is reduced by the device combination not only in the non-isolated DC–DC converter but also in the half-bridge inverter, as presented in Table 5-1 and shown in Fig. 5-22 (a). Similarly, the device combination should reduce the CM capacitance in the full-bridge and 3-phase inverters. The LLC converter and DAB converter are shown in Fig. 5-22 (b) and (c), respectively. As explained in the previous chapters, the device combination reduces the CM capacitance corresponding to the switching node. Therefore, the device combination can decrease

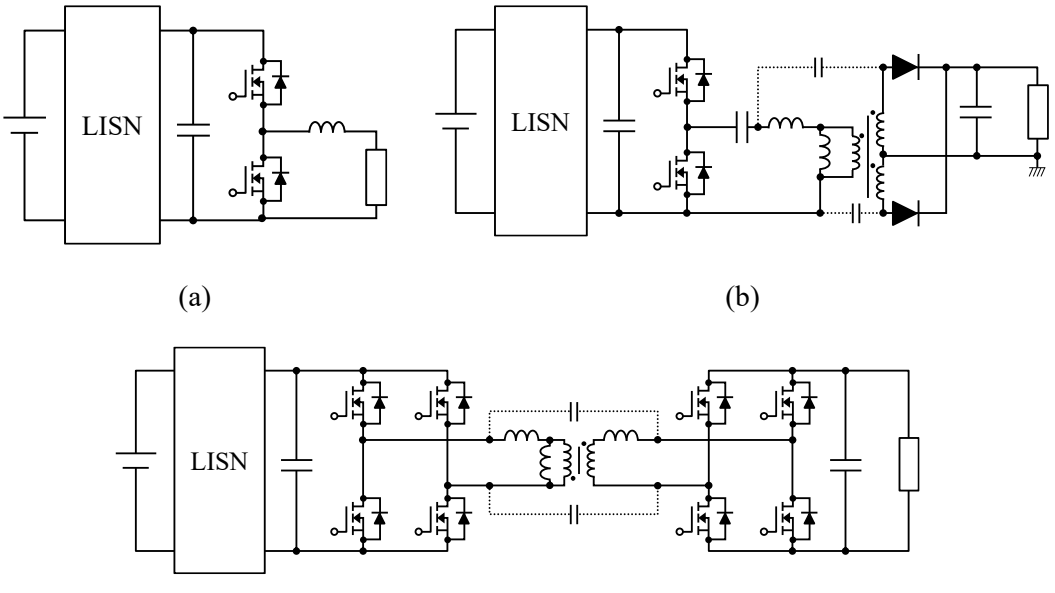


Fig. 5-22. Circuit configurations that the CM capacitance reduction is applied to: (a) half-bridge inverter, (b) LLC converter, and (c) DAB converter.

the CM noise in the circuits shown in Fig. 5-22 (b) and (c) as well. However, the interwinding capacitance of the transformer in Fig. 5-22 (b) and (c) can also act as the CM noise propagation path when the secondary side is grounded, as in the forward and flyback converters discussed in Section 4.6.3. Therefore, the interwinding capacitance should also be minimized to reduce the CM noise by the device combination.

5.7. Conclusion

In this chapter, the effect of modified thermal pads on CM noise was investigated. First, the CM noise in the investigation circuit was analyzed mathematically. Second, the switching devices and the implementation method for investigation were explained. The CM noise with different switching device combinations was compared in the simulation and experiment. The simulation and experimental results showed that the CM noise becomes minimum when the thermal pads avoid connecting to the switching node. Other implementation methods to decrease the CM noise corresponding to the switching node were discussed. In addition, other circuit configurations that can reduce the CM capacitance corresponding to the switching node were discussed. The characteristics of the CM noise reduction with thermal pad assignment are summarized in Table 5-6.

In conclusion, the CM noise reduction method with thermal pad assignment enormously decreases the CM noise in a non-isolated DC–DC converter without changing the circuit configuration and increasing the volume and weight.

Table 5-6. Characteristics of proposed CM noise reduction methods.

	Strong points	Weak points
CHAPTER 5 Thermal pad assignment	- No increase in volume & weight - No change in circuit configuration	- Switching devices with selectable thermal pads are necessary

CHAPTER 6: CONCLUSION

6.1. Summary

Owing to the rising global concerns for energy and environmental issues and an exponential increase in global data traffic, the demand for SMPSs has recently increased to manage electric power in electrified transportation, renewable energy generation, and data centers; in particular, non-isolated DC–DC converters are commonly used for these applications. Therefore, there has been an increase in the use of WBG devices in SMPSs to fulfill the power density requirement. However, a high *dv*/*dt* ratio and high-frequency operation, the characteristics of WBG devices, increase the EMI in SMPSs. Thus, countermeasures are required to reduce the switching noise. However, noise reduction methods such as external filters increase the volume and weight of SMPSs and degrade the power density. Therefore, this dissertation aimed to propose CM noise reduction methods for non-isolated DC–DC converters without increasing their volume and weight.

In Chapter 3, a CM noise reduction method for a multi-phase interleaved DC–DC converter with a coupled inductor by auxiliary winding was proposed. The design guidelines considering the leakage inductance of the auxiliary winding were indicated, and the number of turns in the auxiliary winding was recommended to be as small as possible to suppress the increase in CM noise and expand the bandwidth in which the CM noise reduction is effective. In addition, the influence of the design error on the CM noise reduction effect was discussed. Lastly, the CM noise reduction effect was verified in the experiment.

In Chapter 4, a reversed circuit configuration was proposed to reduce the CM noise by assigning a small CM capacitance to the CM noise propagation path. First, the proposed circuit configuration was analyzed mathematically, and the CM noise reduction mechanism was explained. Next, the implementation method of the experimental circuits to investigate the CM

noise reduction effect was discussed. Finally, the CM noise reduction effect was verified in the circuit simulation and experiment.

In Chapter 5, a combination of thermal pad connections to reduce the CM capacitance in the propagation path and reduce the CM noise was discussed. First, the investigation circuit was mathematically analyzed, and the influence of thermal pads on the distribution of the CM capacitance and CM noise was discussed. Next, the implementation method of the experimental circuits to investigate the CM noise reduction effect was explained. Finally, the circuit simulation and experiment were performed to verify the CM noise reduction effect of the thermal pad connection.

The characteristics of the proposed methods are summarized in Table 6-1. As summarized above, this dissertation offers in-depth discussions on CM noise reduction methods to achieve high-power-density SMPSs with WBG devices from multiple aspects. The ability of each proposed method to reduce the CM noise with a minor or no increase in the volume and weight of the circuit was verified. In addition, each proposed method applies to circuit configurations

Table 6-1 Characteristics of proposed CM noise reduction methods.

	Strong points	Weak points
CHAPTER 3 Auxiliary winding	- Small increase in volume & weight - Available for any number of phases	- CM noise reduction frequency band is limited by leakage inductance L_{lk3}
CHAPTER 4 Reversed configuration	- No increase in volume & weight - No change in circuit components	- Not for MOSFETs with thermal pad connected to source terminals - Thermal pads of diodes are required to be selectable
CHAPTER 5 Thermal pad assignment	- No increase in volume & weight - No change in circuit configuration	- Switching devices with selectable thermal pads are necessary

other than a non-isolated DC–DC converter, as discussed in each chapter. Therefore, this dissertation contributes to the CM noise reduction in other circuit structures.

6.2. Future Prospects

In the future, the CM noise reduction method with auxiliary winding will be investigated with different magnetic materials. Mn–Zn ferrite is utilized because of its high permeability; however, the effective frequency is limited. By contrast, dust cores have low permeability but are effective at higher frequencies. Therefore, the influence of magnetic materials on the CM noise reduction effect will be investigated. In particular, the magnetic coupling of auxiliary winding will be focused because the CM noise reduction effect at a frequency higher than 1 MHz is limited owing to leakage inductance.

The influence of parasitic inductances in the reversed circuit configuration will also be investigated because parasitic inductances affect the high-frequency characteristics of CM noise higher than 7 MHz. To understand CM and DM noise behavior simultaneously, the circuit will be analyzed without simplification such as the CM noise equivalent circuit. In addition, the influence on control and sensing will be investigated because the reversed circuit configuration does not have common ground and circuit control or sensing can be difficult without common ground.

Future studies focusing on other circuit configurations than the non-isolated DC–DC converter discussed in Chapters 3, 4, and 5 are needed. The behavior of the CM noise will be analyzed in detail. The auxiliary winding structure and reversed circuit configuration will be modified to fit in other circuit structures. The CM noise reduction effect will eventually be investigated in experimental conditions.

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