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主　論　文　の　要　旨

論文題目　**Reduction in Mg Ion Implantation Damage and GaN Direct Growth on SiC Substrate for Vertical Power Device Applications**
(縦型パワーデバイス応用のためのMgイオン注入ダメージの低減及びSiC基板へのGaN直接成長に関する研究)

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論　文　内　容　の　要　旨

To apply GaN to high-power device applications in future, GaN-based power devices must have higher current density with a higher breakdown voltage. Vertical device structures have the advantage of a wide vertical channel, which is expected to realize high current density and a high breakdown voltage. By moving the lateral channel from the near surface region to the device bulk, vertical structure devices are also expected to have a low current collapse effect. In this thesis, I investigated several techniques that are important for the realization of GaN-based vertical structure devices.

First, magnesium ion implantation was investigated as a means of realizing p-type GaN. It is still challenging to implant magnesium ions into GaN, because the annealing temperature (calculated to be around 1400-1500 ℃) is much higher than the decomposition temperature of GaN (around 900 ℃). Also, the high thermal activation

energy of magnesium (about 200 meV) and the resulting low activation efficiency (below 1% at room temperature) make a high-dose of magnesium ions necessary to realize a high hole concentration. Increasing the ion dose also increases the ion implantation damage. Many researchers have attempted to optimize the material and thickness of the cap layer to protect the GaN sample surface from losing nitrogen atoms. They have also attempted to optimize the high-temperature post annealing process to further protect the cap layer during this process. My approach has focused on decreasing the ion implantation damage. I proposed a pre-sputter technique and proved its effectiveness for reducing of Mg ion implantation damage on the basis of simulation and experimental results. By simulation, it was shown that the implantation damage could be reduced by about 95% with the use of a 100 nm pre-sputter layer. In the case of low-dose implantation, p-type GaN formation was observed in samples implanted with magnesium ions at both a high temperature and room temperature by photoluminescence and capacitance-voltage measurements. The sample subjected to high-temperature implantation had an activation rate almost one order higher than that of the sample implanted at room temperature. Details are given in Chapter 2.

Secondly, I studied the direct growth of GaN direct growth on a c-plane SiC substrate. In the case of GaN-based power devices with a lateral structure, the breakdown voltage is increased by increasing the distance between the gate and drain electrodes. When using a vertical device structure, the breakdown voltage is increased by increasing the layer thickness of the vertical drift region. Thus, a small device size is expected, which will also result in thermal concentration in the device structure. Thus, it is necessary to use a substrate with high thermal conductivity to resolve this problem. SiC substrates are advantageous owing to their high thermal conductivity. Thus, my research has

focused on developing an epitaxy technique for GaN/SiC vertical structure devices. Owing to the poor surface wetting of gallium, the direct growth of GaN on SiC results in the formation of three-dimensional islands under optimized GaN growth conditions on a sapphire substrate. Thus, GaN is usually grown on SiC via a high-temperature 100-nm-thick AlN intermediate layer. The high-resistance interlayer makes it impossible to fabricate vertical structure devices. My approach is to directly grow GaN on SiC. By employing a pre-flow of trimethylaluminum before GaN growth, an ultrathin AlGaN interlayer was formed. This interlayer provides a simple method improving the poor surface wetting of gallium and the possibility of fabricating vertical structure devices. I realized a direct growth of 1.2-μm thick crack-free GaN layer on both 6H and 4H SiC bulk substrates. The reason for the realization of crack-free GaN was analyzed. The ultrathin interlayer was found to have the effect of releasing the strain generated by the lattice and thermal mismatch between GaN and SiC so that crack-free GaN was realized. This is explained in detail in Chapter 3.

Finally, the direct growth of GaN on a nonpolar SiC substrate was investigated. I realized the nearly direct growth of GaN on both a-plane and m-plane SiC substrates for the first time in the world. This approach involves the growth of GaN on the wall of c-plane trench-patterned SiC substrates. In the case of a trench-patterned c-plane SiC substrate, the walls are a-plane and m-plane SiC. The trench-patterned SiC substrate is a future approach to reducing the impact of the impact of the GaN/SiC band offset. The interface of nonpolar GaN/SiC was also analyzed. The thickness of the interlayer formed by the pre-flow process was found to be around 2-3 nm. To observe the performances of GaN/SiC vertical devices, c-plane GaN/SiC samples were used to fabricate GaN/SiC vertical Schottky barrier diodes. The fabricated Schottky barrier

diodes were compared with GaN/AlN/SiC and GaN/GaN vertical Schottky barrier diodes. The GaN/SiC structure exhibited a significant decrease in series resistance after the TMAl-treatment compared with the GaN/AlN/SiC structure. Almost the same forward I-V performance as the GaN/GaN structure was realized by optimizing the pre-flow process time. Details are discussed in Chapter 4. Finally, it is expected that our proposed techniques will contribute to future GaN-based vertical power devices.