Reduction in Mg Ion Implantation Damage and GaN Direct Growth on SiC Substrate for Vertical Power Device Applications

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縦型パワーデバイス応用のためのMgイオン注入ダメージの低減及びSiC基板へのGaN直接成長に関する研究

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ABSTRACT OF THE THESIS

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To apply Gallium nitride (GaN) to high-power devices in the future, current densities and breakdown voltages must be increased. Vertical device structures possess the advantage of having wide vertical channels, which is expected to realize high current density and high breakdown voltage. By moving the lateral channel from the near-surface region to the bulk of the device, vertical structure devices are also expected to have a low current collapse effect. In this thesis, I investigated several techniques that are important for the realization of GaN-based vertical structure devices.

First, magnesium-ion implantation was investigated as a means of realizing p-type GaN. It is still challenging to implant magnesium ions into GaN because the annealing temperature (calculated to be around 1400°C–1500°C) is much higher than the decomposition temperature of GaN (around 900°C). In addition, the high thermal activation energy of magnesium (about 200 meV) and the resulting low activation efficiency (below 1% at room temperature) make a high-dose of magnesium ions necessary to realize a high hole concentration. Increasing the ion dose also increases the ion implantation damage. Many researchers have attempted to optimize the material and thickness of the cap layer to protect the GaN sample surface from losing nitrogen atoms. Researchers have also attempted to optimize the high-temperature

post-annealing process to further protect the cap layer. My approach focused on decreasing the ion implantation damage. I proposed a pre-sputter technique and demonstrated its effectiveness for reducing Mg-ion implantation damage using both simulations and experiments. The simulation results showed that the implantation damage could be reduced by about 95% with the use of a 100-nm pre-sputter layer. In the case of low-dose implantation, p-type GaN formation was observed by photoluminescence and capacitance-voltage measurements in samples implanted with magnesium ions at both high temperature and at room temperature. The activation rate of the sample subjected to high-temperature implantation was almost one order of magnitude higher than that of the sample implanted at room temperature. Details are given in Chapter 2.

Second, I studied the direct growth of GaN on c-plane SiC substrates. In the case of GaN-based power devices with lateral structures, the breakdown voltage is increased by increasing the distance between the gate and drain electrodes. When using a vertical device structure, the breakdown voltage is increased by increasing the layer thickness of the vertical drift region. Thus, a small device size is expected, which will result in thermal concentration in the device structure. Thus, it is necessary to use a substrate with a high thermal conductivity to resolve this problem. SiC substrates are advantageous due to their high thermal conductivity. Thus, my research focused on developing an epitaxy technique for GaN/SiC vertical structure devices. Due to the poor surface wetting of gallium, the direct growth of GaN on SiC results in the formation of three-dimensional islands under optimized GaN growth conditions on sapphire substrates. Thus, GaN is usually grown on SiC via a high-temperature 100-nm-thick AlN intermediate layer. This high-resistance interlayer makes it impossible to fabricate vertical structure devices. My approach was to directly grow

GaN on SiC. By employing a preflow of trimethylaluminum before GaN growth, an ultrathin AlGaN interlayer was formed. This interlayer improves the poor surface wetting of gallium in a simple fashion, making it possible to fabricate vertical structure devices. I realized the direct growth of 1.2-μm-thick crack-free GaN layers on both 6H and 4H SiC bulk substrates. The reason for the formation of these crack-free GaN layers was investigated. The ultrathin interlayer was found to have the effect of releasing the strain generated by the lattice and thermal mismatch between GaN and SiC, resulting in crack-free GaN. This is explained in detail in Chapter 3.

Finally, the direct growth of GaN on a nonpolar SiC substrate was investigated. For the first time, I realized the nearly direct growth of GaN on both a-plane and m-plane SiC substrates. My approach involved the growth of GaN on the walls of c-plane trench-patterned SiC substrates. In the case of a trench-patterned c-plane SiC substrate, the walls were a-plane and m-plane SiC. The trench-patterned SiC substrate represents a new approach to reducing the effect of the GaN/SiC band offset. The interface of nonpolar GaN/SiC was also analyzed. The thickness of the interlayer formed by the preflow process was found to be around 2-3 nm. To observe the performances of GaN/SiC vertical devices, c-plane GaN/SiC samples were used to fabricate GaN/SiC vertical Schottky barrier diodes. The fabricated Schottky barrier diodes were compared with GaN/AlN/SiC and GaN/GaN vertical Schottky barrier diodes. compared with the GaN/AlN/SiC structure, the GaN/SiC structure exhibited a significant decrease in series resistance after the TMAl-treatment. The forward I-V performance was almost the same as that of the GaN/GaN structure after the preflow process time was optimized. Details are discussed in Chapter 4. The techniques proposed in this theses are expected to contribute to future GaN-based vertical power devices.

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1. Preface

1.1 Introduction

Nowadays, energy problems are becoming more and more serious, generating a need for tremendous progress in both science and industry technology. Gallium nitride (GaN) is receiving considerable attention due to its optical device applications (e.g., the use of GaN-based light emitting diodes (LEDs) was found to decrease energy usage related to lighting by about 61% in Japan[1]) and its power device applications (e.g., the use of GaN-based transistors decreased energy loss of an inverter and converter system by about 60%[2]). Akasaki, Amano, and Nakamura were awarded the 2014 Nobel Prize in Physics for their contributions to making GaN an energy-efficient and environmentally friendly light source. GaN-based devices have already developed, commercialized, and applied in optical devices. In the future, GaN-based devices are expected to be applied in more fields as power devices to save energy. This thesis focuses on applying GaN to power devices.

GaN was first synthesized by Johnson et al. in 1932[3] and again by Juze and Hahn in 1938[4] by passing ammonia over hot gallium. Until the discovery of low-temperature nucleation buffer layers by Amano et al. in 1986[5], the crystal quality of GaN was too poor for the fabrication of light-emitting devices. The synthesis of p-type GaN by Amano et al.[6] began a device revolution. Since then, GaN has been widely applied to LEDs, laser diodes (LDs), and high-electron-mobility transistors (HEMTs). As a direct bandgap semiconductor material, GaN/InGaN hetero-structures can have high internal quantum efficiency. With GaN/InGaN blue LEDs and phosphors, white LEDs can be easily fabricated. GaN/InGaN LEDs have long lifetimes with low power dissipation.

LED lighting is expected to save a quarter of the 300 TWh light power used in Japan by 2020. To further improve the lighting performances of LEDs, the dislocation density within GaN should be decreased to improve the internal quantum efficiency of the device. Using epitaxial lateral overgrowth, the dislocation density in hetero-epitaxial GaN was decreased from 10^8–10^{10} to 10^5–10^6 cm^{-2}. It also greatly improved the reliability of GaN-based LDs and pushed GaN-based LDs into commercialization. With the development of GaN-bulk growth technique, future GaN-based LDs could have easy device process with small device size. On the other hand, two-dimensional electron gas (2DEG) is generated by piezoelectric polarization fields in the GaN/AlGaN hetero-epitaxial growth technique. High-mobility 2DEG is used as the HEMT's channel. HEMTs have attracted attention due to their radio frequency switching speeds and low on-resistances under high-temperature (HT) operation. Currently, GaN-based power devices are applied in middle-power applications. Future GaN-based power devices are expected to be used in high-power applications. The details are described in the next section.

Table 1.1. Properties of semiconductors[7)]

	GaN	4H-SiC	Si	GaAs
Bandgap at RT［eV］	3.39	3.26	1.1	1.4
Relative permittivity	9.0	10	11.8	12.8
Electric field strength［10^6 V/cm］	3.3	2.0	0.3	0.4
Electron mobility［cm^2/Vs］	1500 (2DEG)	720^a,650^c	1350	8500
Saturation velocity of electron［10^7 cm/s］	2.5	2.0	1.0	2.0
Thermal conductivity［W/cm・K］	1.3	4.5	1.5	0.5

1.2 GaN-based Power Devices and Applications

As GaN is a wide-bandgap semiconductor material, GaN-based power devices are expected to be third-generation electrical devices after Si-based first-generation and GaAs-based second-generation electrical devices. Si-based electrical devices are widely applied due to the near-perfect epitaxial growth technique of Si. GaAs-based electrical devices are mainly applied for high-frequency applications because of the high electron mobility of GaAs. As semiconductor technology has developed, Si-based power devices have approached a performance plateau due to the limitations of the properties of silicon. Further improving the performances of Si-based power device also presents challenges for the cooling systems. Future power devices are expected to operate at HT with high breakdown voltage and low on-resistance performances.

GaN-based electrical devices are expected due to the excellent material properties of GaN. The properties of GaN and several other semiconductor materials are shown in Table 1.1.[7] GaN has a wide bandgap, large breakdown field, high electron mobility, and high saturation velocity of electrons. Thus, GaN-based power devices are expected to have the following advantageous characteristics:

(1) Due to the wide bandgap of GaN, GaN-based power devices should be able to operate at HT, decreasing the cooling requirements, and also have radiation hard operation;

(2) Due to the large critical electric field of GaN, GaN-based power devices should have high breakdown voltage and low on-resistance; and

(3) Due to the high mobility and high saturation velocity of GaN, GaN-based power devices should operate at high frequency with reduced size of passives.

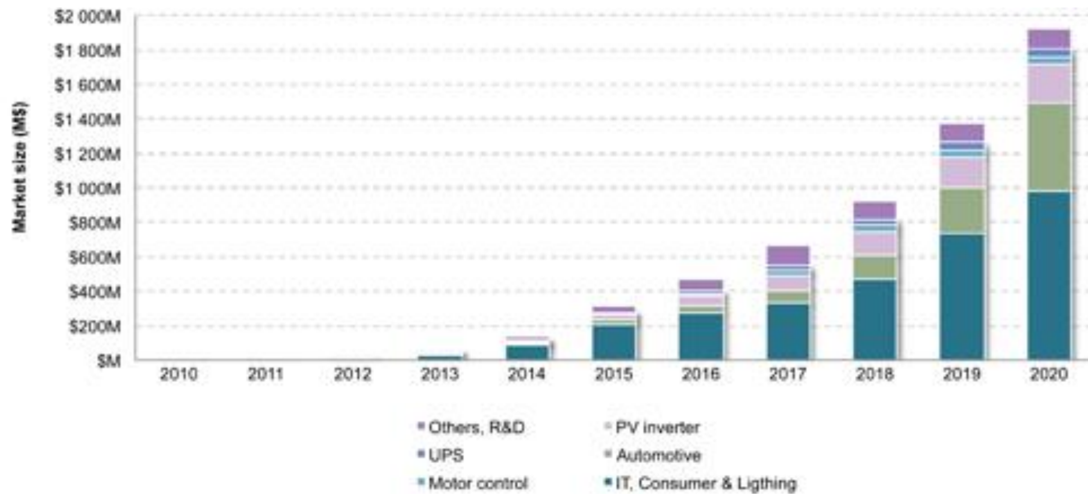


Fig. 1.1. Analysis of the world-wide market for GaN-based devices.[8)]

Thus, GaN-based electrical devices are currently attracting considerable interest. GaN-based power devices are widely studied in many countries. Due to their abovementioned merits, GaN-based power devices are expected to contribute to increase in popularity. The radio frequency and low switching energy loss performances are expected to improve the energy transfer efficiencies of invertor and convertor systems. The high-temperature operation is expected to release the automotive cooling system request. The high breakdown voltage performance is expected to drive power applications without the use of a voltage transformer to realize miniaturization. These applications are expected to enlarge the market for GaN-based power devices in the near future. Figure 1.1 presents an analysis of the current and expected market for GaN-based devices conducted by Yole development in France[8)]. The market for GaN-based power devices is expected to keep increasing and exceed 1 billion U. S. dollars by 2020. The analysis also shows that GaN has many applications in power devices.

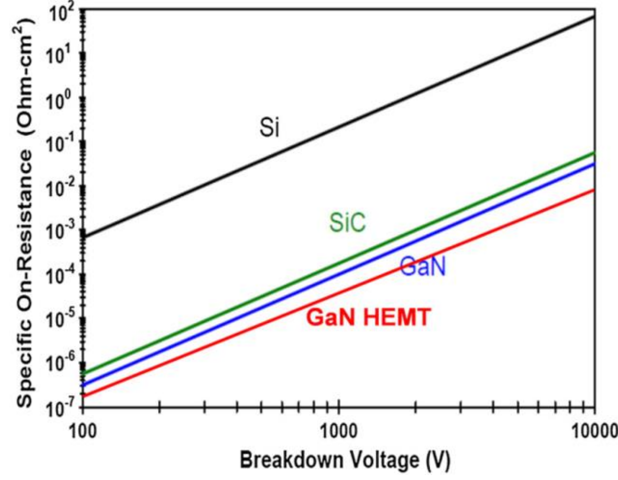


Fig. 1.2. Comparison of the ideal specific on-resistance and breakdown voltage of GaN with those of Si and SiC.[9)]

As energy problems become more and more serious, power devices with low on-resistance are demanded. For vertical structure power devices, the ideal specific on-resistance is defined as the resistance of the drift region per unit cross-sectional area and is given as:

$$R_{ON} = \frac{4\,\mathrm{BV}^2}{\varepsilon_s \mu_n E_C^3} \tag{1.1}$$

In Formula (1.1), BV is the breakdown voltage, ε_s is the dielectric constant, μ_n is the mobility of the drift region, and E_C is the critical breakdown field. The trade-off relationship between on-resistance and breakdown voltage can be seen in this formula. The relationship between on-resistance and breakdown relationship for GaN is plotted and compared with those of Si and SiC in Fig. 1.2.[9)] The on-resistances of GaN-based power devices are expected to be three orders of magnitude lower than those of Si-based power devices at the same breakdown voltage. As mentioned before, GaN-based HEMTs can achieve radio frequency switching speed by high mobility 2DEG channel. The on-resistance of a GaN-based HEMT is obtained by Formula (1.2):

$$R_{ON} = \frac{BV^2}{q\,\mu\,Q_S E_C^2} \tag{1.2}$$

where μ is the free carrier mobility in the 2DEG channel, Q_S is the sheet carrier density, and $E_{C,L}$ is the critical electric field for breakdown in a structure with uniform electric field along the drift region. The on-resistance of a GaN-based HEMT is plotted in red in Fig. 1.2. The low on-resistance is the reason that GaN-based power devices could decrease the energy loss of an inverter system by about 60%.

GaN-based power devices are attracting interest due to the low on-resistance and high-frequency performance. Until now, GaN-based power devices are usually applied by HEMT. As GaN is a wide-bandgap semiconductor material, GaN-based power devises are also expected exhibit high-power performance. However, this remains difficult to achieve with GaN-based power devices due to current collapse (Fig. 1.3).[10] Current collapse is defined as a recoverable decrease in drain current caused by the trapping effect of electrons. The reason for current collapse has been discussed in many papers.[11-14] In the case of HEMT, the device structure is a lateral structure, and the device channel is formed by the 2DEG. To resolve the current collapse problem, we should develop new device structures. For this reason, vertical device structures have received considerable attention. The details of vertical structure devices are discussed in the next section.

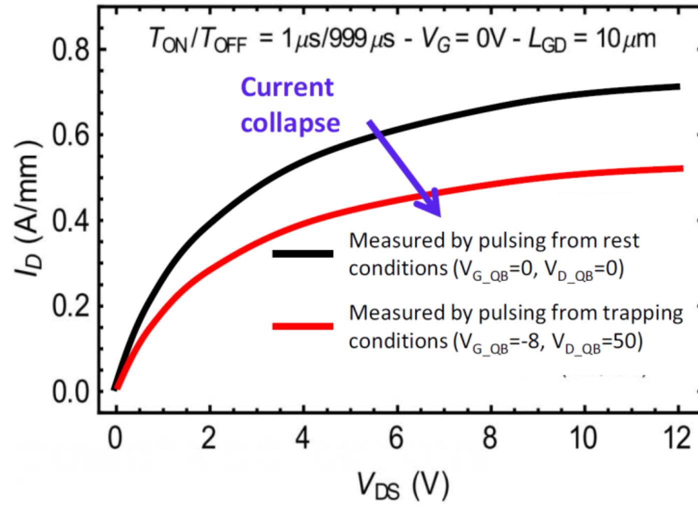


Fig. 1.3. Current collapse effect in a GaN-based lateral power device.[10)]

1.3 Vertical Structure GaN Power Devices

To further improve the performances of GaN-based power devices, a revolution in GaN lateral device structure is necessary. A vertical device structure has been suggested to overcome problems such as traps and low current density. In the case of silicon, a vertical device structure is common for high-power applications. Moving the channel to the bulk enables high current and high blocking voltage performances with small chip size. In addition, the current collapse problem is expected to be resolved because the device channel is moved from the near-surface region. The fabricated high-power devices could provide direct drive for high-power applications without using a voltage transformer. At the same time, HT operation could further enhance their performances.

1.3.1 GaN-based Vertical Power Device Structure

A current aperture vertical electron transistor (CAVET) has been employed in

GaN-based vertical structure power devices.[15-16)] The structure of the CAVET is illustrated in Fig. 1.4; it consists of a source region separated from a drain region by an insulating layer containing a narrow aperture that is filled with a conducting material. The gate metal and the source metal separately contact the p-type and AlGaN regions. The drain metal contacts the n-type region below the aperture. Elections flow from the source contacts along the 2DEG. They then flow through the aperture into n-type GaN and are collected at the drain. The conductivities of the material inside the aperture as well as in the drain region must be much larger than that of the 2DEG so that the total current passing through the device is determined by the conductivity of the 2DEG. Simultaneously, the conductivity of the 2DEG must be much higher than that of the adjacent bulk GaN directly below the 2DEG to ensure current flow through the 2DEG rather than through the bulk GaN. A Schottky gate located directly above the aperture is used to modulate the charge in the 2DEG, thereby controlling how much current passes through the aperture and is collected at the drain.

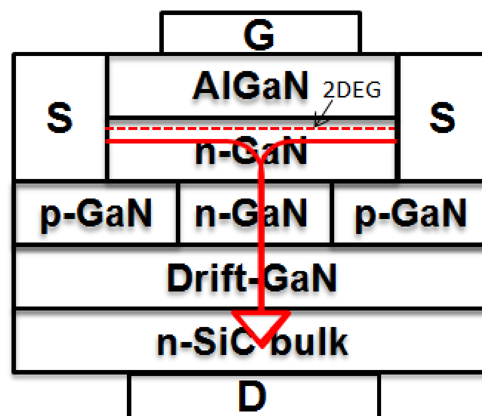


Fig. 1.4. Electron flow in the GaN-based CAVET.

1.3.2 Ion Implantation in GaN-based Vertical Structure Power Devices

The main challenge in realizing GaN-based vertical structure devices is generating a current-blocking region consisting of a lateral pnp layer. The electrical conductivity can only be controlled layer-by-layer when using the metalorganic vapor phase epitaxial (MOVPE) growth method. Etching and regrowth techniques have also been employed to produce the lateral pnp current-blocking region. Damage caused by the etching generated a low-crystal-quality regrowth layer, resulting in an unacceptable device performance. In the case of silicon, vertical structure power devices are fabricated by ion implantation using a mask to achieve the lateral pnp region. With ion implantation, the electrical conductivity can be laterally controlled by using a mask. In addition, we can control the accelerating voltage to modulate the thickness of the implantation layer. Thus, we can easily generate the pnp current-blocking region.

Applying ion implantation to GaN, n-type GaN can be realized by silicon ion implantation. However, the realization of p-type GaN by magnesium ion implantation has rarely been reported. To achieve GaN-based vertical structure power devices, it is necessary to apply magnesium ion implantation to realize p-type GaN. Thus, I propose a pre-sputter technique for the realization of p-type GaN by ion implantation. The details of this approach are described in Chapter 2.

1.3.3 Direct Growth of GaN on SiC for GaN-based Vertical Structure Power Devices

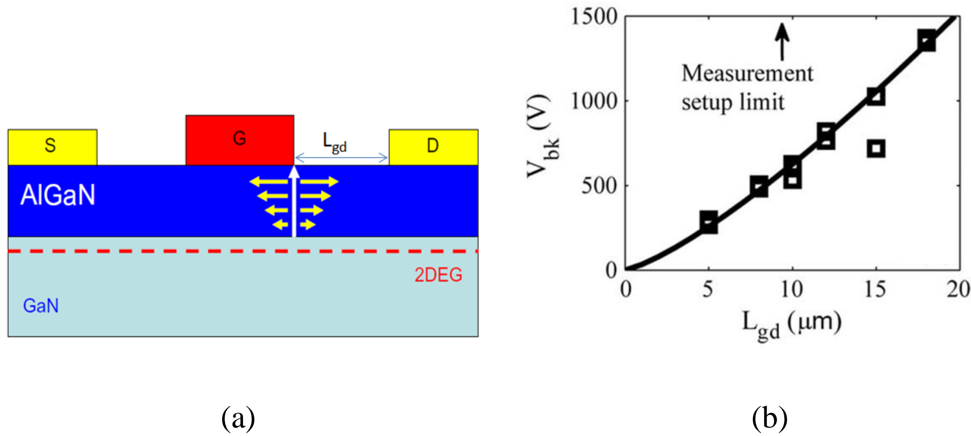
One of the advantages of vertical structure power devices is the ability to achieve a high breakdown voltage with small chip size, as explained in Fig. 1.5. For GaN-based lateral power devices, the high electric field appears under the gate edge near the drain electrode side, as shown in Fig. 1.5(a).[17] The breakdown voltage of a GaN-based lateral

power device linearly increased with increasing distance between the gate electrode and drain electrode, as shown in Fig. 1.5(b).[18] It also enlarged chip size. In the case of vertical structure power devices, the breakdown voltage is determined by the layer thickness of the drift region, the structure of which is shown in Fig. 1.4. Thus, it is possible to fabricate high-power devices with small chip size. However, the small chip size concentrates heat within the devices.

To realize GaN-based high-power devices, it is important to decrease the junction temperature (T_j) within the devices. When T_j is higher than an available value, the current is greatly enhances, causing breakdown performance. To describe the thermal dispersion, the thermal resistivity (R_T) was defined. The relationship between T_j and R_T is described by Formula (1.1):

$$T_j - T_a = P \times R_T \tag{1.1}$$

where T_a is the temperature of the environment, and P is the dissipation power of the device. To obtain high-power performance, the R_T should be reduced. Table 1.1 indicates that SiC substrates are advantageous due to their thermal conductivity, which is equal to the reciprocal of R_T. If GaN could be directly grown on SiC substrates and with low vertical resistance, we could obtain GaN/SiC CAVETs. Due to improved thermal dispersion, GaN/SiC CAVETs are expected to operate at high power with small chip size. The commercialization of this technology currently favors the use of SiC over GaN due to availability of high-quality 6-inch SiC substrates in large volumes. I realized the direct growth of GaN on SiC using a preflowed trimethylaluminum (TMAl) treatment process. The details are given in Chapter 3.



(a) (b)

Fig. 1.5. (a) Schematic of the high-field region in a GaN-based lateral structure with white vertical arrow.[17)] (b) The relationship between L_{gd} and breakdown voltage.[18)]

1.3.4 Direct Growth of GaN on Non-polar SiC Substrates

To apply the GaN/SiC growth technique to vertical structure power devices, we should consider the effect of the band offset of the GaN/SiC interface on the performance of the vertical power device. One approach is to grow GaN on trench-patterned SiC substrates. A scanning electron microscopy (SEM) image of a trench-patterned substrate is shown in Fig. 1.6. The non-polar face of SiC appeared on the wall of the trench-patterned c-plane SiC substrate. It is important to understand the growth conditions and the band offset of non-polar GaN/SiC. We realized the direct growth of non-polar GaN on non-polar SiC substrates. The details are discussed in Chapter 4.

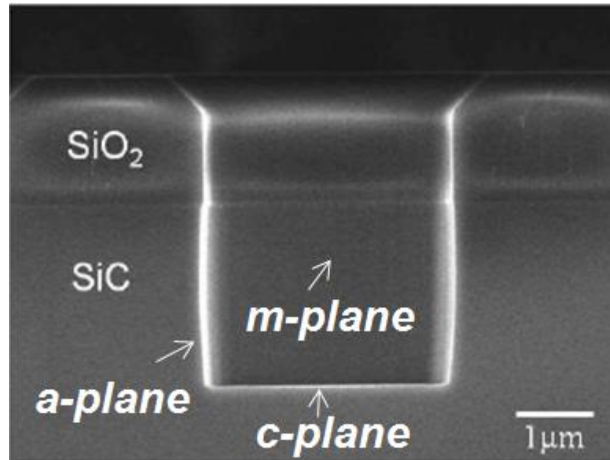


Fig. 1.6. SEM image of a trench-patterned c-plane SiC substrate.[19)]

1.4 My Research and the Structure of This Thesis

As mentioned above, the goal of this thesis is to apply new technologies to the fabrication of GaN-based vertical structure power devices. A block diagram showing the concept of each chapter in this thesis is shown in Fig. 1.7, and this thesis is organized as follows.

Chapter 1 introduces the background of the thesis starting from history of GaN materials. Chapter 1 also discusses why vertical structure power devices are necessary and how the research described herein contributes to GaN-based vertical structure power devices.

Chapter 2 introduces the background of magnesium ion implantation and proposed a pre-sputter technique for magnesium ion implantation. The simulation and experimental results related to the pre-sputter technique are discussed.

Chapter 3 introduces the MOVPE growth process and describes the experiments on the direct growth of GaN on SiC substrates. An analysis of the GaN/SiC interface is also reported.

Chapter 4 describes the direct growth of non-polar GaN on non-polar SiC substrates. To test the GaN/SiC structure, c-plane GaN/SiC samples were fabricated into vertical GaN/SiC Schottky barrier diodes (SBD), which were then compared to GaN/AlN/SiC and GaN/GaN SBDs.

The summary and conclusions of the thesis are given in Chapter 5.

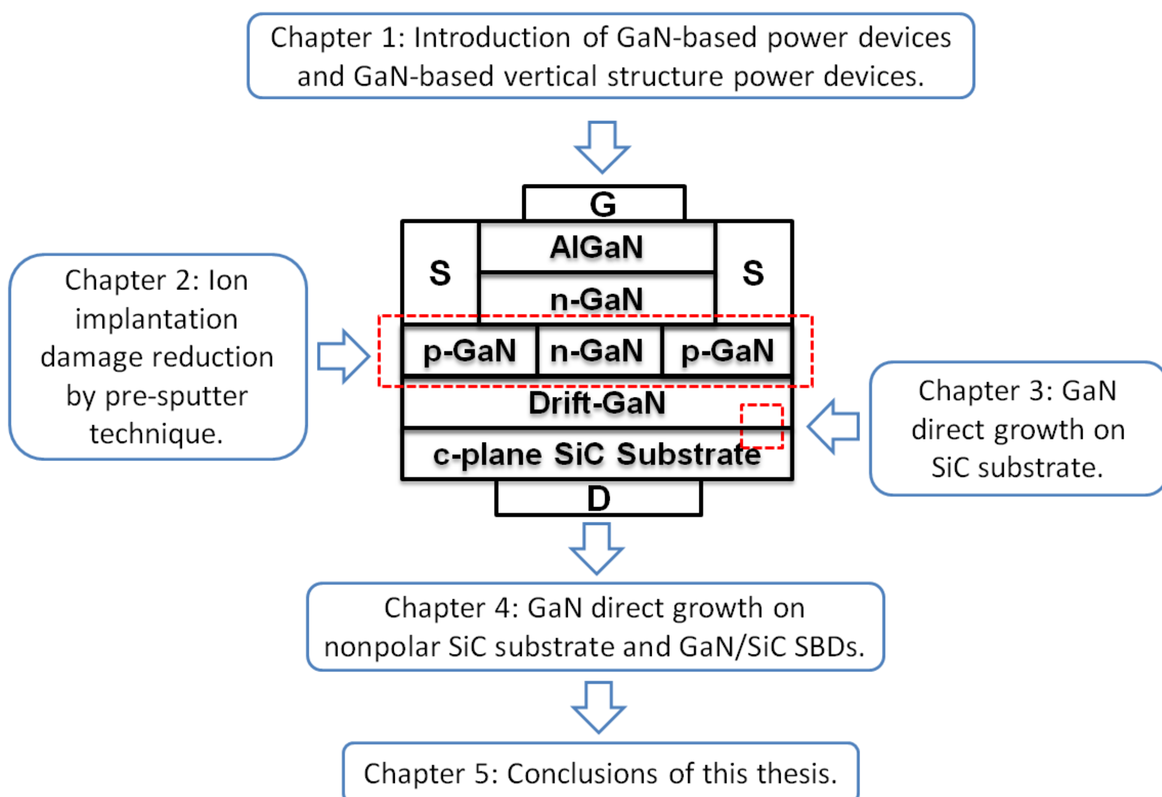


Fig. 1.7. Block diagram showing the concept of each chapter in this thesis.

References

1） http://eneken.ieej.or.jp/data/3862.pdf

2） http://techon.nikkeibp.co.jp/article/HONSHI/20091026/176926/

3) W. C. Johnson, J. B. Parsons, and M. C. Crew, J. Phys. Chem. **234**, 2651 (1932).

4) R. Juza E. Hahn and Z. Anorg. Allgem, Chem. **234,** 282 (1938).

5) H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, Appl. Phys. Lett. **48,** 353 (1986).

6) I. Akasaki, H. Amano, Y. Koide, K. Hiramatu, and N. Sawaki, J. Cryst. Growth **98,** 209 (1989).

7) T. Sugiyama: Master Thesis, Study on temperature dependence and analysis of Ⅲ-Nitride semiconductor power-devices, University of Meijo, Nagoya, 2010 [in Japanese].

8) http://www.optochina.net/html/zx/scfx/16056.html

9) B. J. Baliga, Semicond. Sci. Technol. **28**, 074011 (2013).

10) M. Meneghini, G. Meneghesso, and E. Zanoni, Materials Research Society Fall meeting (2014).

11) J. Joh and J. A. del Alamo, IEEE TED **58**, 1 (2011).

12) C. Y. Hu and Tamotsu Hashizume, J. Appl. Phys. **111**, 084504 (2012).

13) C. H. Yu, Q. Z. Luo, X. D. Luo, and P. S. Liu, the Scientific Word Journal **2013**, 931980 (2013).

14) M. Meneghini, C. D. Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso, and E. Zanoni, IEEE TED **60**, 10 (2013).

15) I. Ben-Yaacov, Y. Seck, U. K. Mishra, and S. P. DenBaars, J. Appl. Phys. **95**, 4 (2004).

16) S. Chowdhury, B. L. Swenson, and U. K. Mishra, IEEE EDL **29**, 6 (2008).

17) J. A. Alamo and J. Joh, Microelectronics Reliability **49**, 1200 (2009).

18) B. Lu and T. Palacios, IEEE EDL **31**, 9 (2010).

19) http://www.samcointl.com/tech/iframe/SiC/photo_04.html

2. Magnesium Ion Implantation in GaN with a Pre-sputter Technique

2.1 Introduction

Ion implantation is a widely used in semiconductor materials such as silicon and silicon carbide to locally alter the conductivity of the semiconductor material, either by increasing the doping concentration or compensating for free carrier concentrations. Ion implantation involves the introduction of impurity species into the semiconductor via high-energy bombardment. In this way, the depths and concentrations of the impurities can be carefully controlled both vertically, by specifying the ion energy and dose, and laterally, by using appropriate masking techniques. However, during the implantation process, the semiconductor crystal incurs significant damage, and the implanted dopants do not necessarily occupy the preferred substitutional lattice sites. Therefore, to repair the implantation-induced damage and promote the incorporation of the dopant species at the proper lattice sites, HT post-implantation annealing is performed. Generally, the annealing is performed at a temperature that is roughly two thirds of the semiconductor's melting point. For GaN, which has a melting temperature of over 2538 K at 1 atm[1], a post-annealing temperature of over 1419°C is expected for the activation of implanted ions. However, since GaN will dissociate and sublime at much lower temperatures, care must be taken during the annealing process to maintain the crystal stoichiometry.[2]

Although n-type GaN can be realized by Si-ion implantation,[3-7] the realization of p-type GaN by Mg-ion implantation has rarely been reported.[8-9] In this chapter, I proposed a pre-sputter technique and carried out the Mg-ion implantation process to

demonstrate the ability of this new technique to reduce the implantation damage.

2.2 Pre-sputter Technique

As mentioned before, it remains challenging to realize p-type GaN by Mg-ion implantation, primarily due to the high thermal activation energy of magnesium (about 200 meV) and the resulting low activation efficiency (below 1% at room temperature),[10] which make high-dose implantation necessary. Thus, post-annealing at high temperature is required to repair the implantation damage and activate the implanted ions. Many researchers have tried to optimize the material and thickness of the cap layer to protect the surface of the GaN sample from losing nitrogen atoms.[11-16] Other studies have tried to optimize the post-annealing process to further protect the cap layer during such a process.[2] My approach focuses on decreasing the damage caused by ion implantation.

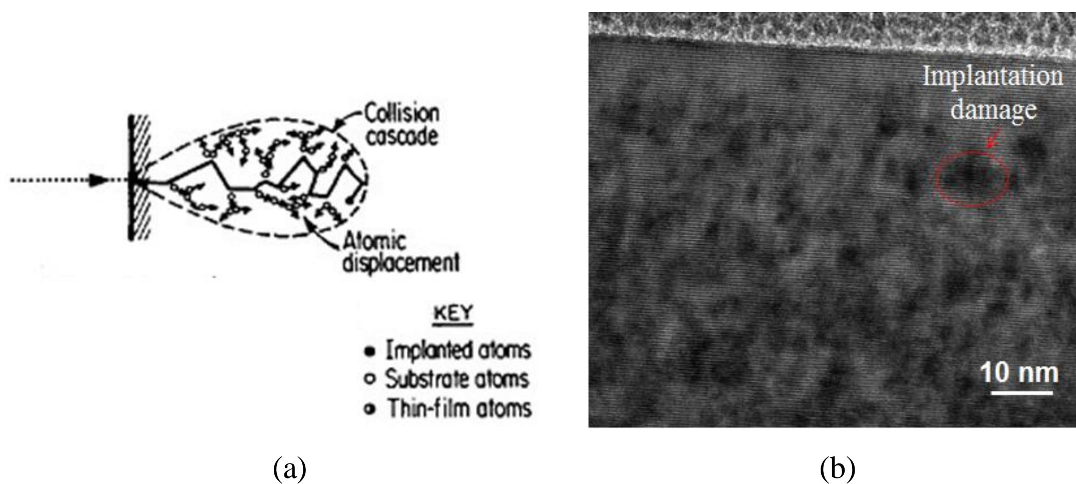


Fig. 2.1 (a) Schematic of implantation damage[17] and (b) an high-resolution transmission electron microscopy (HRTEM) image showing implantation damage.

Ion-implantation is a process by which ions are accelerated in an electrical field and implanted into the target material. The accelerated ions lose their energy and stop via

the nuclear stopping and electronic stopping mechanisms. The implantation damage is caused by nuclear stopping, during which the lattice atoms collide via energy nuclear collisions and move from their origin positions. This produces many point defects inside the target crystal, including vacancies and interstitials. The displaced atoms may cause cascades of secondary displacements of nearby atoms to form a tree of disorder along the ion path, as shown in Fig. 2.1(a)[17)]. The atomic arrangement of the GaN crystal film was detected using high-resolution transmission electron microscopy (HRTEM). The damage caused by the implantation ions resulted in the disorder of the atomic arrangement within the GaN film, leaving the black point regions shown in Fig. 2.1(b). When the number of displaced atoms per unit volume approaches the atomic density, the material becomes amorphous.

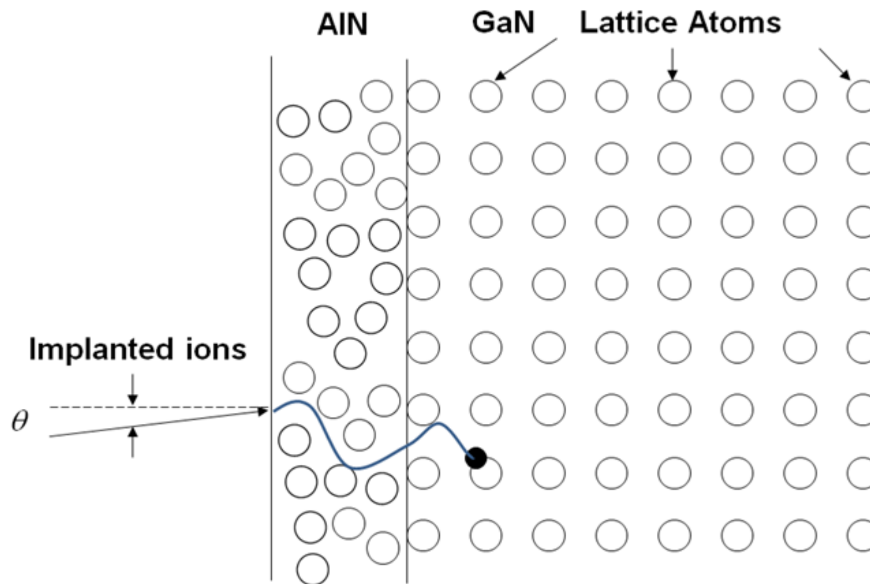


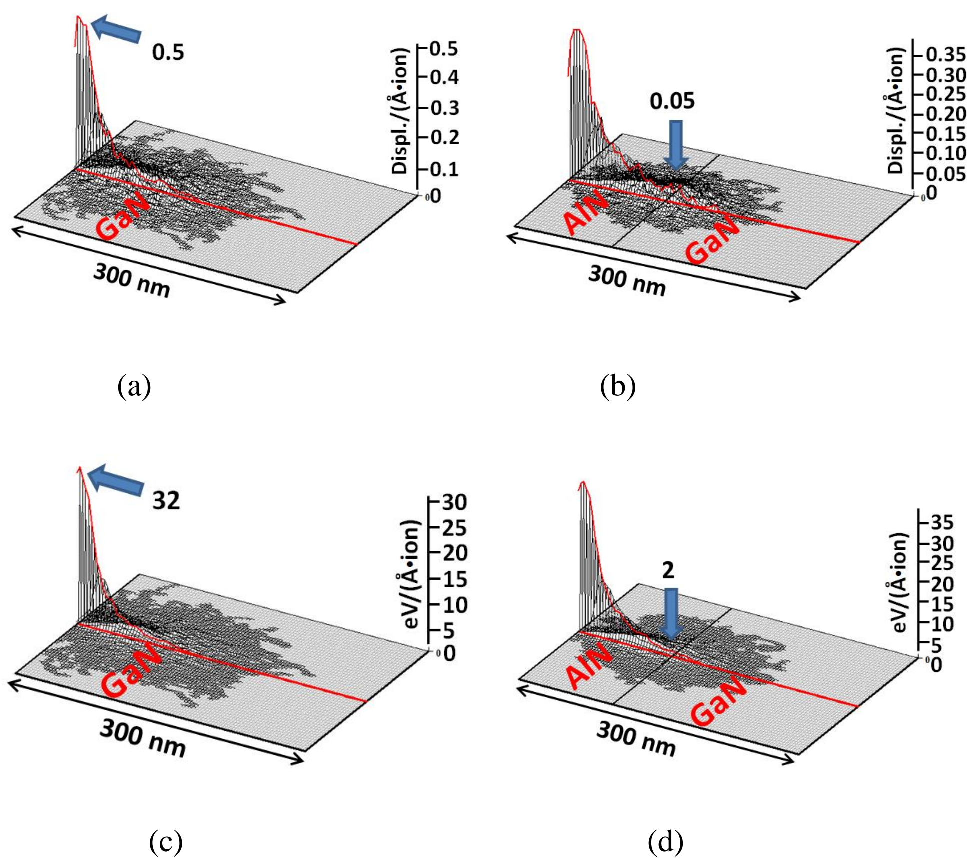
Fig. 2.2 Schematic of ion implantation into a pre-sputtered AlN/GaN sample.

To reduce the implantation damage, I propose adding an extra layer with a disordered atomic arrangement to generate more nuclear collisions outside of the sample surface. I

propose to pre-sputter (PS) an amorphous layer on the implantation sample surface. The pre-sputtered amorphous layer is expected to cause more nuclear collisions, absorbing the implantation damage within the PS layer (Fig. 2.2). The implantation angle shown in Fig. 2.2 is optimized to decrease the number of tunneling ions, which is a common method in the implantation process. This technique is referred to as the PS technique in this thesis. Using the PS technique, I hope to decrease the implantation damage so that it is easier to activate the implanted ions.

To demonstrate this concept, we simulated the ion implantation process with and without the PS technique using the simulation software TRIM, which calculates the stopping and range of ions into matter using a quantum mechanical treatment of the ion-atom collisions.[18)] TRIM uses statistical algorithms that allow the ions to jump between calculated collisions and then averages the collision results over the intervening gap. During the collisions, the ion and atom have a screened coulomb collision, including exchange and correlation interactions between the overlapping electron shells. The ion has long-range interactions that create electron excitations and plasmons within the target.[18)] Using TRIM, I compared the Mg-ion implantation of a GaN sample with that of a PS-AlN/GaN sample. The three-dimensional damage distribution results, including the number of Ga vacancies, N vacancies, and collisions, are shown in Figs. 2.3(a) and (b). Originally, all lattice sites were considered to be occupied. If an energetic incident atom knocked a lattice atom from its site, it left the vacancy. If the incident atom still left energy after forming the vacancy, it continued moving and transferred energy to other lattice to make another vacancy or displacement, causing a cascade of collisions. Figures 2.3(a) and (b) show that the sample without the PS-AlN layer was greatly damaged, and the damage was concentrated near the GaN surface [Fig. 2.3(a)]. In the sample with the PS-AlN layer, most of the damage was

localized in the PS-AlN layer, and the damage to the GaN layer was markedly reduced by about 95% [Fig. 2.3(b)]. The ionization energies of the implanted ions were calculated, and the results are shown in Figs. 2.3(c) and (d); in addition to reducing the damage, the PS technique also significantly decreased the ionization energy [Fig. 2.3(d)].



(a) (b)

(c) (d)

Fig. 2.3 TRIM simulation results: (a) 3D damage distribution for Mg-ion implantation into single-layer GaN; (b) 3D damage distribution for Mg-ion implantation into PS-AlN/GaN; (c) 3D ionization distribution for Mg-ion implantation into single-layer GaN; and (d) 3D ionization distribution for Mg-ion implantation into PS-AlN/GaN.

In this section, the challenge in realizing p-type GaN via the implantation process is

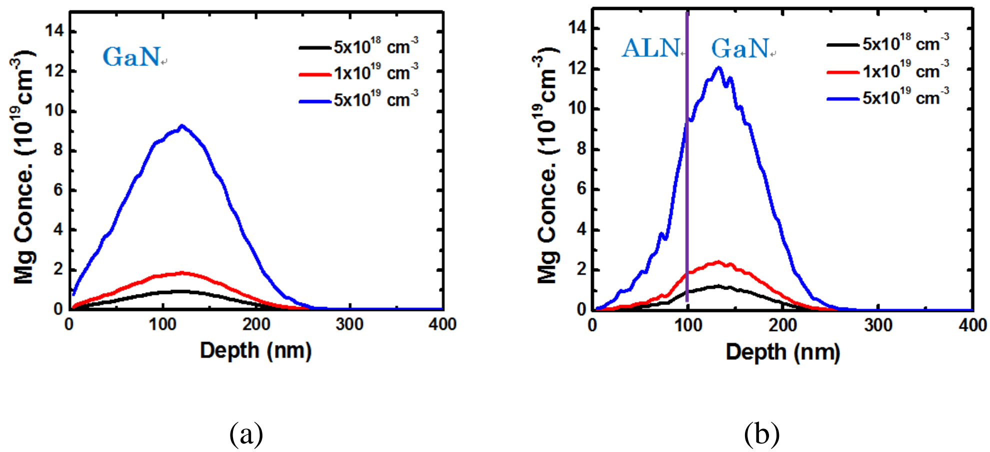
related to the considerable implantation damage, which cannot be repaired using the traditional annealing conditions. Thus, I proposed the PS technique for Mg-ion implantation to reduce implantation damage. This idea came from the pre-amorphous technique, by which a high-dose implantation with low acceleration energy is applied to other semiconductor materials to form an amorphous layer before the main implantation process.[19)] In the case of GaN, pre-amorphous implantation will also cause significant implantation damage that is difficult to repair. The PS technique offers a simple method to deposit an amorphous layer before the implantation process. The PS layer can be easily etched using developer fluid after the implantation process, allowing us to obtain samples with low implantation damage (see the paper in which I reported the PS technique for GaN[20)]). The TRIM simulations indicated that the PS technique reduced the implantation damage by approximately 95%. The reduced implantation damage also lowered the ionization energy. The PS technique could also get high surface ion concentration and lower the contamination while HT implantation process. Using the PS technique, we expect to achieve p-type GaN by post-annealing implanted samples with low implantation damage.

2.3 Reduction in Implantation Damage using the Pre-sputter Technique

2.3.1 Experimental Conditions of Mg-ion Implantation in GaN

Undoped GaN/sapphire templates with thicknesses of 2 μm were grown by MOVPE and used for Mg-ion implantation. To evaluate the effect of the PS technique on ion implantation damage, GaN templates with and without PS AlN layers were prepared. PS AlN layers with thicknesses of approximately 100 nm were deposited by reaction

sputtering at room temperature, and the Mg-ion implantation process was then carried out at an implantation ion energy of 110 keV. To decrease the number of tunneling ions, the implantation was carried out at an angle of 7°. The PS technique was tested under different ion implantation conditions; different Mg-ion implantation concentrations (5×10^{18}, 1×10^{19}, and 5×10^{19} cm^{-3}) and implantation temperatures (room temperature and 500°C) were tested. As implantation concentration increases, the implantation damage is thought to increase due to the increased number of collisional ions. Compared to room-temperature ion implantation, high-temperature ion implantation is expected to result in less damage because part of the implantation damage can be recovered by thermal motion. The high-temperature ion implantation temperature used herein was only 500°C due to the limitations of the implantation equipment.



(a) (b)

Fig. 2.4 Mg-ion distributions simulated by TRIM.

The magnesium-ion implantation profile was simulated by TRIM with an ion energy of 110 keV. The implantation angle was set at 7° to reduce the tunnel effect on the implantation profile. The ion concentration profiles of GaN and PS-AlN/GaN samples are shown in Fig. 2.4. The profile of the PS-AlN/GaN sample exhibited a sharper peak,

which is attributed to the decreased number of channeling ions. After the implantation process, sub-peaks were observed in the 2θ-ω x-ray diffraction (XRD) pattern. Also, the sub-peaks changed by the number and the intensity with different implantation damages. Thus, I used the 2θ-ω XRD mode to characterize the ion implantation damage. The details are given in Section 2.3.3.

2.3.2 Demonstration of XRD Measurement

Figure 2.5 shows the schematic diagram of the XRD technique. Figure 2.5(a) shows the simple structure of the XRD equipment.[21] An X-ray source and a detector are the necessary elements of an X-ray system. X-rays are produced in an X-ray tube by accelerating a high-energy electron beam toward a metal anode, resulting in characteristic X-ray transitions in the anode. Beam conditioners are used to collimate and monochromate the X-rays. The specimen is mounted on a sample holder that can rotate along three axes: phi (Φ), psi (ψ), and omega (ω). A detector that can move through the Bragg angle while scanning is used to collect the diffracted X-rays. Materials with different lattice constants can be detected using the 2θ-ω mode of XRD. In the next section, XRD is used to characterize the samples before and after the implantation process.

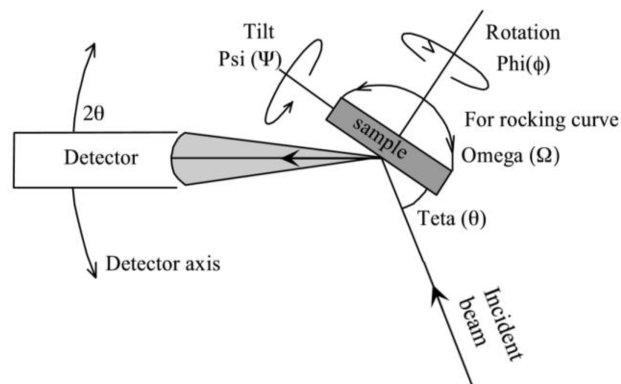


Fig. 2.5. Schematic diagram of the XRD technique.[21]

2.3.3 Experimental Results and Discussion

The 2θ-ω scan XRD patterns of samples before and after the implantation process are shown in Fig. 2.6. The implantation process caused the formation of the sub-peaks, demonstrating the formation of a material with a different lattice constant. I interpret this as follows: the implantation process formed a damaged layer with a different lattice constant. The thickness of the formed damage layer could be estimated by comparing the ratio of the implantation damage and the GaN original peak's intensities. The estimated thickness of the damage layer changed from 35 to 355 nm. The positions and numbers of the peaks changed under different implantation conditions, demonstrating the formation of one or multiple crystalline layers with different lattice constants. The peaks' positions were shifted as the implantation conditions changed. In addition, the sub-peaks formed due to implantation damage moved away from the original GaN peak when the damage was significant. The samples with considerable damage formed multiple sub-peaks. Thus, I think the characterization of these peaks could find and compare the implantation damages by the analysis of the sub-peaks. The lattice constant and damage layer x-ray density were calculated and are discussed below to further understand the relationship between the implantation damage and these sub-peaks.

The lattice constants $\boldsymbol{a}$ and $\boldsymbol{c}$ of the samples determined by XRD were compared to those of free-standing GaN substrates. According to Bragg's rule, $\boldsymbol{c}$ for GaN was calculated from the (0002) plane's result. Then, the lattice constant $\boldsymbol{a}$ could be calculated from the (10-12) plane using Formula (2.1):

$$\frac{1}{d^2} = \frac{4}{3}\left(\frac{h^2+h\mathrm{k}+k^2}{a^2}\right) + \frac{l^2}{c^2} \qquad (2.1)$$

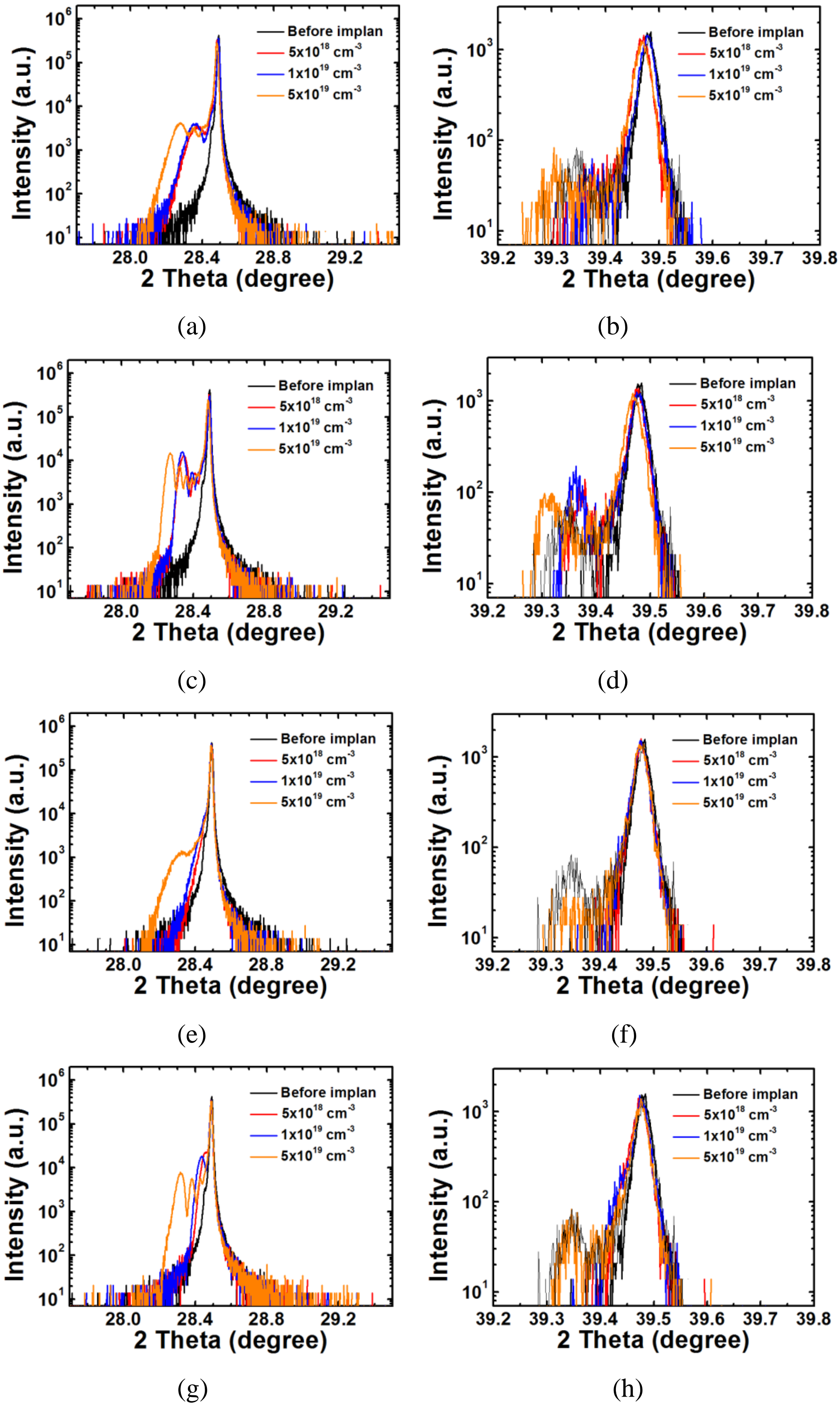
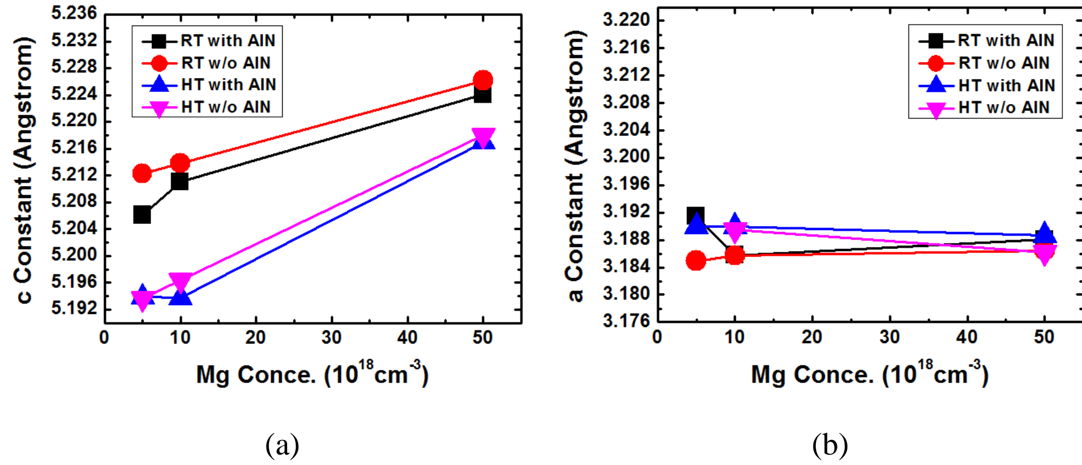


Fig. 2.6. 2θ-ω XRD patterns before and after implantation under various conditions: (1)

RT implantation with AlN on the (a) (0002) and (b) (10-12) planes; (2) RT implantation without AlN on the (0002) and (10-12) planes; (3) HT implantation with AlN on the (0002) and (10-12) planes; and (4) HT implantation without AlN on the (0002) and (10-12) planes.

The lattice constants of the samples before and after implantation under different conditions were calculated from the 2θ-ω XRD patterns. For the samples with multiple peaks, the peak on the far-left side was taken to represent the change in lattice constant. The results are shown in Fig. 2.7. Secondary ion mass spectrometry (SIMS) was used to confirm the implantation concentrations to verify that the experimental results could be compared to the simulation results. Compared to the lattice constants of free-standing GaN (***a*** = 5.189 Å, ***c*** = 3.186 Å), the damage layers showed large ***a*** and ***c*** constants. The lattice constant ***c*** increased linearly with increasing magnesium concentration. The lattice constant ***a*** remained nearly the same. If we consider that the implantation damage increased with increasing implantation dose, we could compare the implantation damage because of the linear change of the lattice constant ***a*** with increasing the magnesium concentration. Figure 2.7 suggests that HT implantation resulted in less implantation damage due to the small change in ***c***. This is attributed to the recovery of implantation damage due to the thermal movement of atoms during the implantation process. Using the PS technique, we could further reduce the implantation damage via the absorption of nuclear collisions.



(a) (b)

Fig. 2.7 Changes in the lattice constants (a) ***c*** and (b) ***a*** under different implantation conditions.

In the previous calculation of lattice constants, only the peak at the curve's left-most side was considered when multiple peaks were present. This peak was considered to represent the change in lattice constant caused by implantation damage. To also consider the sub-peaks, the areas of the sub-peaks were calculated by separating each peak using Gauss function (misalignment < 1 %). The dependencies of sub-peaks/area of all peaks in XRD results on Mg implantation concentration under different implantation conditions are plotted in Fig. 2.8; sub-peak area increased with increasing implantation concentration, indicating a direct proportional relationship between sub-peak area and implantation damage in the case of using PS technique. When the implantation concentration was above 1×10^{19} cm^{-3}, implantation damage could not be controlled by HT implantation, which observed different trend of change as indicated by the changes in the lattice constants (Fig. 2.7). I could not explain this difference. By the area calculation, damage reduction by PS technique could be observed more clearly under HT-implantations. This further proved the ability of the PS technique to reduce implantation damage. The reduction in implantation damage achieved by the PS

technique is attributed to the absorption of nuclear collisions by the amorphous PS layer. In the next section, the post-annealing of the implanted samples is discussed.

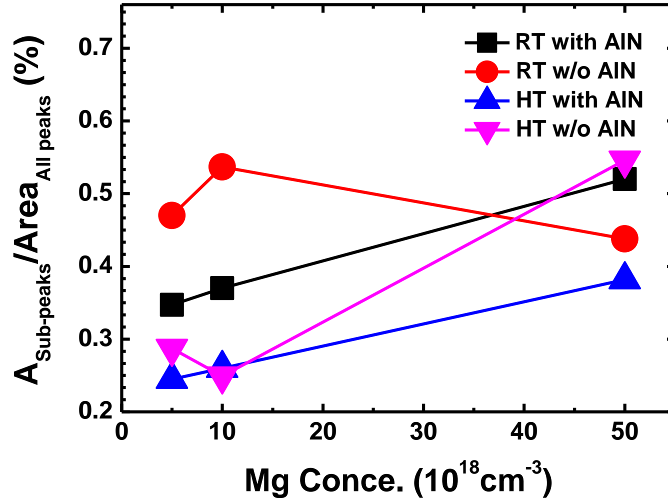


Fig. 2.8. Dependence of area of sub-peaks/area of all peaks in XRD results on Mg implantation concentration under different implantation conditions.

2.4 Mg-ion Implantation with the Pre-sputter Technique

2.4.1 GaN Implantation with Low Mg-ion Concentration (10^{17} cm^{-3})

Here, I describe the growth of a 1.5-µm-thick GaN epilayer on a c-plane sapphire substrate via a low-temperature GaN buffer layer at 150 Torr by MOVPE. The prepared samples were pre-sputtered by reactive sputtering using an Al target and N_2 plasma. The thickness of the sputtered AlN layer was 94 nm. Subsequently, a single-implantation process was carried out at an accelerating voltage of 85 keV with an Mg-ion concentration of 2×10^{17} cm^{-3} at 500°C with an angle of 7°. Post-annealing was carried out in a MOVPE chamber in an ammonia and H_2 environment using a pressure of 300 Torr and a sample surface temperature of 1200°C. The post-annealing

time was 10 or 15 min.

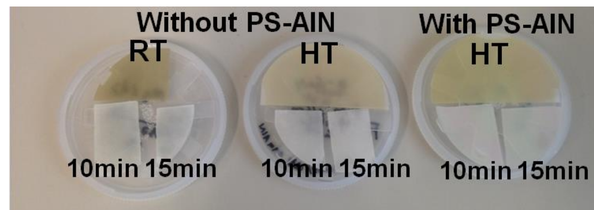


Fig. 2.9. Photographs of samples formed under different implantation conditions before and after post-annealing.

The Mg-ion concentrations were determined by SIMS to be 2×10^{17} cm^{-3}. Photographs of the samples before and after post-annealing are shown in Fig. 2.9. After implantation, the color of the sample changed to brown due to the ion implantation damage. After post-annealing, the colors of all samples recovered to transparent, indicating that the implantation damage was repaired to some degree.

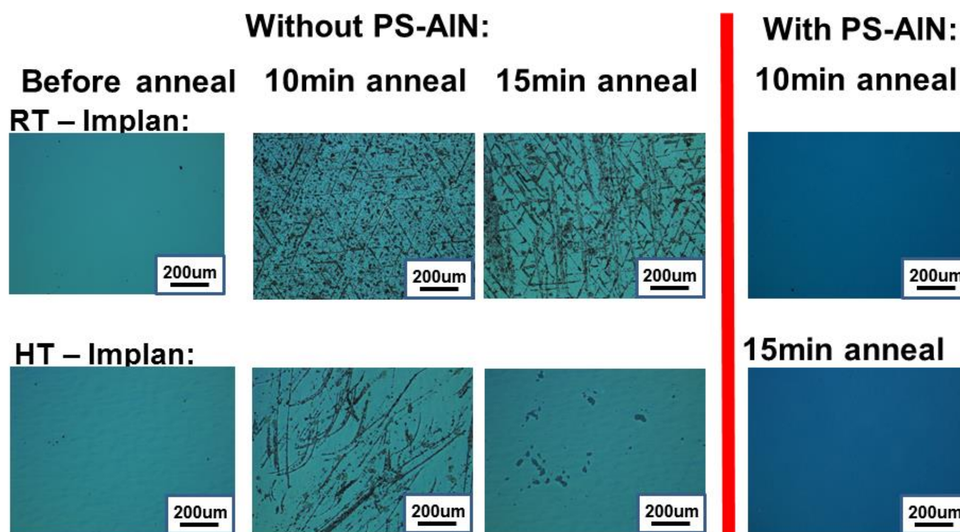
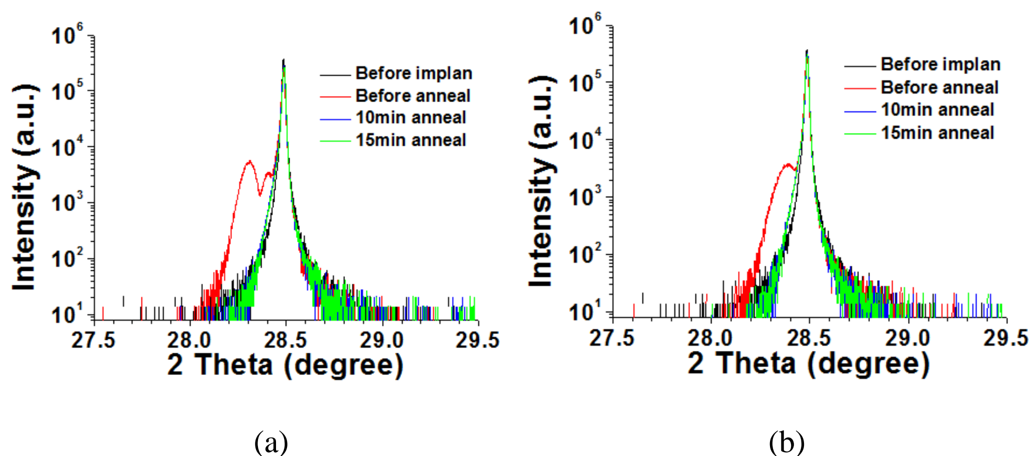


Fig. 2.10 Optical microscopy (OM) images of samples formed under different implantation conditions before and after post-annealing.

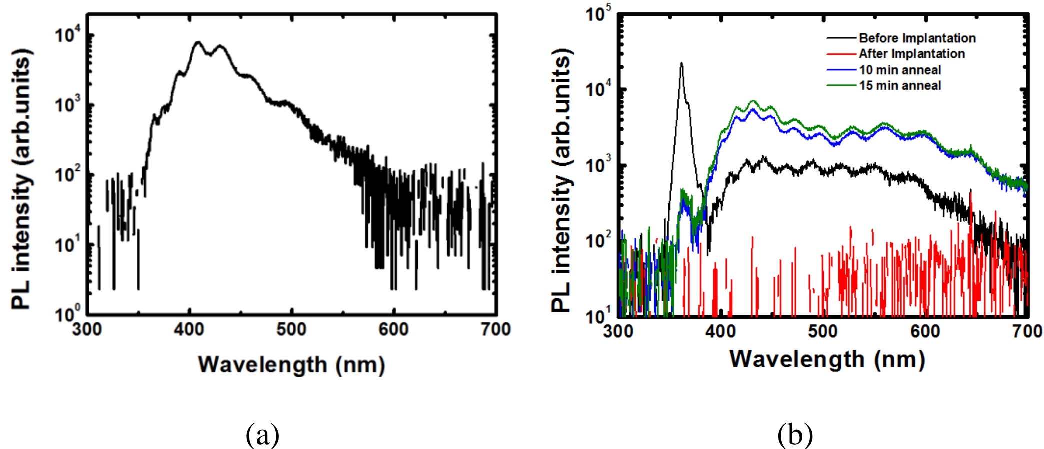
The optical microscopy (OM) images shown in Fig. 2.10 show that the pre-sputtered AlN layer well protected the samples formed with the PS technique after 10 or 15 min of post-annealing at 1200°C. In the case of ion implantation without the PS technique, AlN layers were deposited after the ion-implantation process and used as a cap layer to protect the sample surface from losing nitrogen atoms during the HT post-annealing process. The experimental results showed that the PS AlN layer deposited before the implantation process could better protect the sample surface than the AlN layer deposited after the implantation process under the same sputtering conditions. This is attributed to the different implantation damage within the samples with and without the PS technique. Without the PS technique, the sample surfaces exhibited cracks or were partly decomposed due to strain caused by the lattice constant and thermal mismatches. In the PS-AlN layers, I considered that the implantation process generated defects inside the AlN layer; these defects released part of the strain and made the AlN layer more stable, protecting the sample surface. This theory will be tested further in future work.



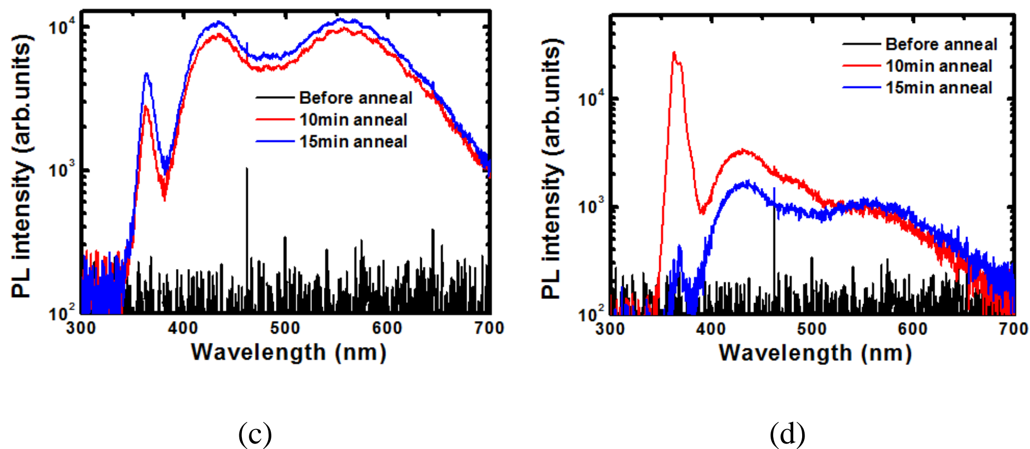
(a) (b)

Fig. 2.11. XRD patterns of samples formed (a) without PS and (b) with PS before and after post-annealing at 1200°C.

In the previous part, I reported that ion implantation damage could be detected by the sub-peaks in the 2θ-ω XRD spectra. The samples formed with and without the PS technique before and after post-annealing were analyzed, and the results are plotted in Fig. 2.11. Without the PS technique, two sub-peaks were observed, which are considered to be both formed by implantation damage but not diffraction effect judging from the peaks' shape. When the PS technique was used, the number of sub-peaks formed by implantation damage decreased from two to one, again verifying the ability of the PS technique to reduce implantation damage. After post-annealing for 10 or 15 min at 1200°C, the sub-peaks disappeared, indicating that part of the implantation damage was repaired during the post-annealing process. As other possibilities, it is also considered to be magnesium atoms are desorbed by the post-annealing. To confirm these results, SIMS measurements will be performed in a future study.



(a) (b)



(c) (d)

Fig. 2.12. PL spectra of (a) p-type GaN grown by MOVPE, (b) HT implantation with a PS layer, (c) RT implantation without a PS layer, and (d) HT implantation without a PS layer before and after post-annealing at 1200°C for 10 and 15 min.

Photoluminescence (PL) measurements were employed to determine the optical properties of the samples using a 325-nm He-Cd laser at room temperature (Fig. 2.12). The RT PL spectra of undoped GaN and p-type GaN grown by MOVPE are shown in Fig. 2.12(a) as references to evaluate the optical properties of p-type GaN doped with magnesium. The PL spectrum of p-type GaN formed by MOVPE is dominated by blue luminescence (BL). Figures 2.12(b), (c), and (d) show the RT PL spectra of samples implanted with Mg ions before and after post-annealing. The samples showed weak luminescence after the implantation process, indicating that ion implantation damaged the optical properties of the samples. After annealing, optical properties were recovered, as indicated by the strong enhancement in their luminescence peaks. For HT implantation with the PS technique, the > 100-fold decrease in edge emission luminescence and the greatly enhanced BL-to-edge emission ratio indicated that a large number of magnesium ions had correctly entered the Ga sites, as shown in Fig. 2.12(b). The spectra of the Mg-implanted samples after post-annealing were similar to

the spectrum of the Mg-doped GaN sample, indicating the formation of p-type GaN by Mg-ion implantation. Without using PS technique, similar optical property change could only be found in the case of HT implantation after 15 min anneal at 1200°C [Fig. 2.12(d)]. In other cases, the anneal condition is not enough to active the Mg-ions' optical property. In this experiment, only samples with PS layers had both flat and uniform surfaces and spectra similar to the p-type GaN spectrum.

Next, the samples with PS layers were subjected to capacitance-voltage (C-V) measurements to observe their electrical properties. Schottky contacts and quasi-Ohmic electrodes were formed on the sample surfaces using a mercury probe. For the large difference between the two electrodes' areas, the reverse charge region under the small electrode (1 mm) could be approximately calculated. The doping concentration was obtained from the dC/dV slope of the C-V curve. The depth at which the doping concentration was evaluated was obtained from the capacitance.[22] The sample carrier density profile was calculated by Formulas (2.1) and (2.2) as

$$N_A(W) = -\frac{C^3}{qk_S\varepsilon_0 A^2 dC/dV}, \qquad (2.1)$$

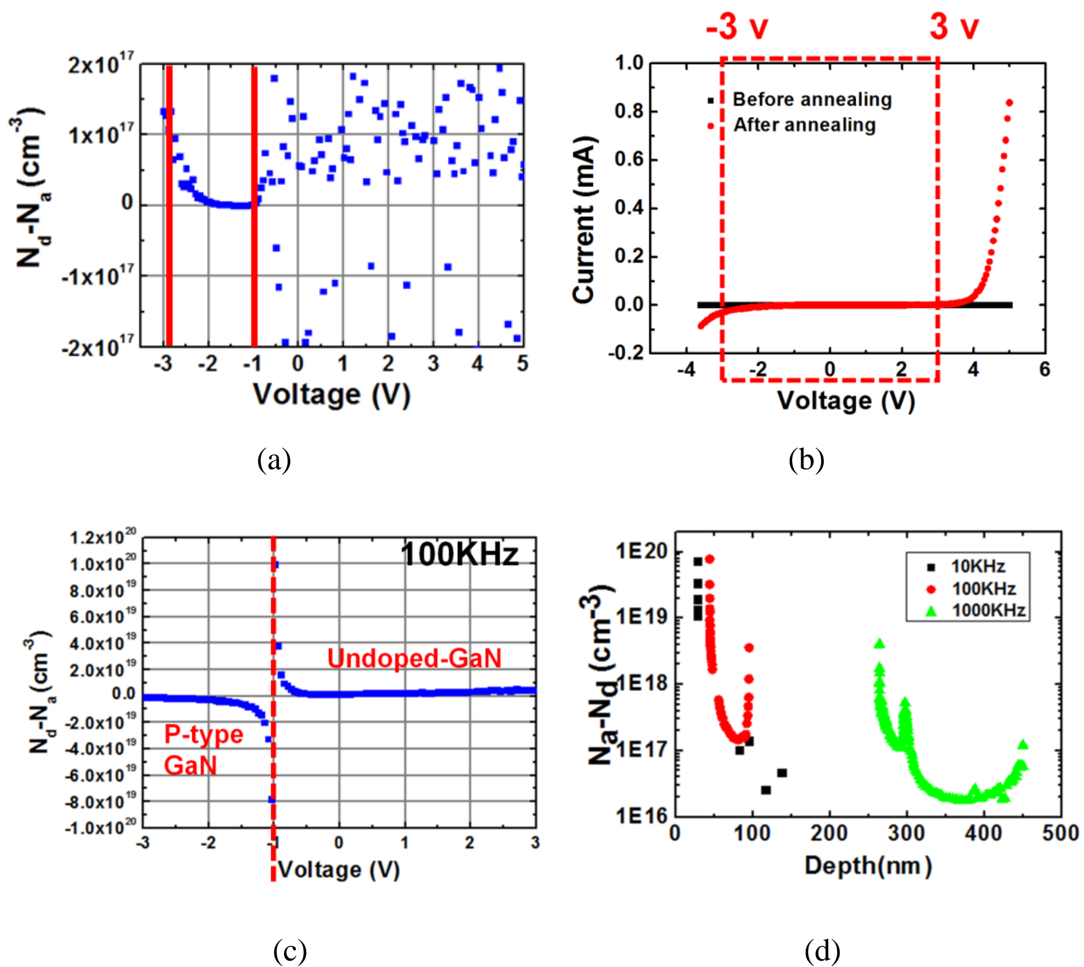
where,

$$W = \frac{k_S\varepsilon_0 A}{C}, \qquad (2.2)$$

and A is the area under the electrode.[23] The samples before and after implantation were measured, and the results are shown in Fig. 2.13. First, the original sample without ion implantation was measured. The relationship between N_d-N_a and voltage is plotted in Fig. 2.13(a). The continuous signal was only be detected in the plus region of N_d-N_a, which showed the signal of unintentional doped n-type GaN. The effective donor concentration was observed to be 5×10^{14} cm^{-3} in the sample before implantation. The samples after the ion implantation were then measured. The current-voltage (I-V) curves of the samples before and after post-annealing are plotted in Fig. 2.13(b). After

ion implantation, low current was observed in the sample (black curve) due to the semi-insulator layer formed by the implantation damage. After post-annealing, the sample's electrical property was recovered. The I-V curve is plotted as the red line in Fig. 2.13(b). The Schottky contact formed by the mercury probe on the sample surface was confirmed. The Schottky barrier region (-3~3 V) was used to estimate the carrier density profile in the sample. The dependence of voltage on N_d-N_a is plotted in Fig. 2.13(c). The implanted GaN sample after post-annealing showed a reversed region in the N_d-N_a-to-voltage relationship, indicating that the acceptor density was higher than the donor density. It also indicated that the activated Mg ions entered the Ga sites and became acceptors. We also measured the post-annealed sample at different frequencies (10 to 1000 kHz), and the results are plotted in Fig. 2.13(d). p-Type signals were found at each frequency. The depth and acceptor concentration signals changed with frequency, which was considered to be related to the electron-trapping effect of the deep levels formed by Mg-ion implantation. During C-V measurements, the carried density profiles were estimated by Formulas (2.1) and (2.2) according to the AC voltage signal. At low frequency, the number of trapped electrons is higher than that at high frequency. The capacitance used in these formulae did not consider the electron-trapping effect. It caused a high capacitance to be used and decreased the width of the charged depletion layer in Formula (2.2). At the same time, the calculated carried density in Formula (2.1) would become high the reason of which is the trap effect. With increasing AC voltage frequency, the changing frequency of the depletion layer width increased, decreasing the number of trapped electrons. Thus, the calculated depletion layer width increased, and carrier density decreased. A similar trap phenomenon was also found in my Mg-doped p-type GaN samples. I consider this to be caused by the defects formed by magnesium or the deep level of magnesium. It is

difficult to accurately estimate the carrier density because of the trap effect, as mentioned before. However, the formation of p-type GaN could be judged from the stable plus region of N_a-N_d. All in all, p-type GaN formation was confirmed by the C-V measurements in samples formed under HT implantation using the PS technique. Similar results were also found for RT implantation with the PS technique. Without the PS technique, the rough sample surface after annealing made it difficult to obtain the electrical properties of the samples.



(a) (b)

(c) (d)

Fig. 2.13. C-V measurement results of (a) the sample without implantation and (c) the 10 min post-annealed implantation GaN sample. (b) I-V curves of before and after 10 min post-annealed implantation GaN samples. (d) N_a-N_d carrier density and depth

profiles of post-annealed implantation GaN samples under different C-V frequencies.

Hall measurements were used to determine the carrier density, carrier type, and the mobility of the implanted samples. Although the carrier type by ion implantation could be judged to be p-type. The optical properties also offered evidence for the formation of p-type GaN by ion implantation. The accurate carrier density was left to be judged because of the trap effect. First, RT Hall measurements were carried out on the implanted samples formed using the PS technique. All the samples exhibited n-type GaN. The reason is considered to be effected by the unintentional doped n-typed GaN, which is under the implanted layer. The p-type layer formed by implantation was too thin (around 100 nm) with a low acceptor density [around 10^{16} cm^{-3}; Fig. 2.13(d)]. To observe p-type GaN by Hall measurement, I think it is necessary to increase the implantation concentration and implanted layer. In the next section, the details of high-concentration implantation are discussed.

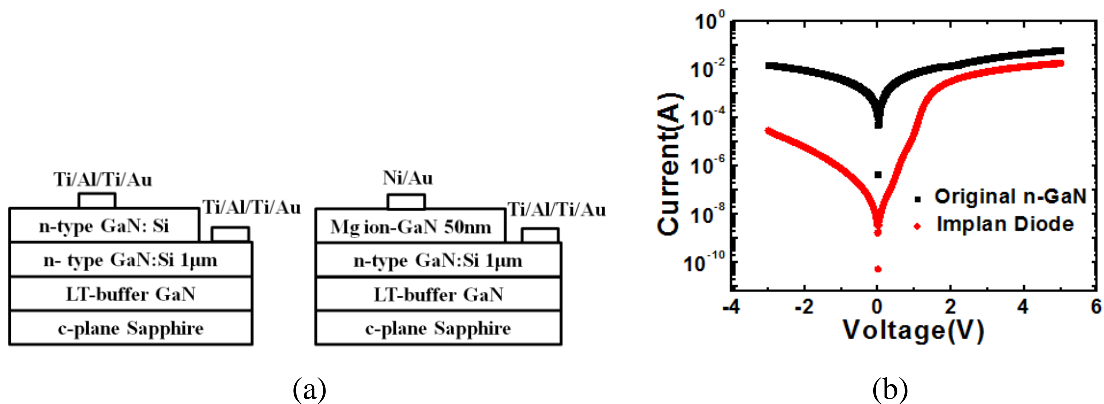


Fig. 2.14. (a) Schematic view of the structures of the fabricated devices and (b) I-V curves of the implanted p-n diode and original n-GaN sample.

Finally, p-n junction diodes with Mg-ion implantation were fabricated and compared

with the sample without implantation. The structures of the fabricated devices are shown in Fig. 2.14(a). For the p-n junction diode, the p-type GaN layer used Mg-ion implantation into a PS-AlN (100 nm)/n-GaN (2 μm, 3×10^{18} cm^{-2}) template. The sample was implanted by Mg ions with an ion-energy of 85 keV at a peak Mg concentration of 2×10^{17} cm^{-3}. The implantation angle was 7°, and the implantation temperature was 500°C. After HT post-annealing for 15 min, the PS-AlN layer was removed by wet etching while the sample was placed into a developing fluid. The device was then fabricated as follows: (1) mesa etching using an Ni mask and dry etching by inductively coupled plasma (ICP); (2) Ti/Al/Ti/Au contact deposition by EB; (3) annealing at 650°C in N_2 for 5 min; (4) Ni/Au contact deposition by EB; and (5) annealing at 525°C in O_2 for 5 min. Steps 2 and 3 made an Ohmic contact on the n-type GaN layer, and steps 4 and 5 made an Ohmic contact on the Mg-ion implanted GaN layer. The I-V curves of the fabricated devices were shown in Fig. 2.14(b). The curve of the sample without implantation exhibited a near-Ohmic property. The implanted sample exhibited a diode curve; however, the threshold voltage was less than 2 V because the implanted p-type GaN layer was too thin (less than 50 nm).

All in all, for implementation with a low Mg ion concentration (10^{17} cm^{-3}) with the PS technique followed by 15 min of post-annealing at 1200°C, optical recovery was observed by RT PL measurements. The formation of a p-type layer was observed by C-V. Hall measurement revealed that the carrier types of the implanted samples were n-type. To observe p-type carriers by Hall measurement, a thick implanted layer with a high implantation concentration should be realized. The details of the implantation with high Mg concentration is discussed in the next section.

2.4.2 Implantation of GaN with High Mg-ion Concentration (>10^{17} cm^{-3})

The Mg implantation concentration was then increased. GaN templates (2 μm) were pre-sputtered using an Al target and N_2 plasma. The thickness of the sputtered AlN layer was 94 nm. The single-implantation process was then carried out at an accelerating voltage of 110 keV with Mg concentrations of 5×10^{18}, 1×10^{19}, and 5×10^{19} cm^{-3} at RT or 500° C with an angle of 7° with or without PS-AlN. The post-annealing process was carried out in a MOVPE chamber in an ammonia and H_2 gas environment at a pressure of 500 Torr. A 1150°C post-annealing process was carried out for 10 min for the HT-implanted PS-AlN/GaN samples.

After ion implantation, all the samples were brown in color because the implantation damage changed the light absorption properties of the samples. After the post-annealing process, all the samples recovered to a transparent color, again indicating that part of the implantation damage could be recovered by the post-annealing process.

In the previous sections, I demonstrated the use of 2θ-ω XRD to analyze implantation damage. The XRD results of samples implanted at high Mg concentrations are shown in Section 2.3.3. After post-annealing, the XRD sub-peaks disappeared in the HT-implanted PS-AlN/GaN samples, indicated that the crystal damage caused by implantation had been repaired. The recovery in the optical properties of the samples was then evaluated by RT PL. The recovery of the electrical properties was analyzed by C-V and Hall measurements.

For low-concentration implantation (10^{17} cm^{-3}), optical recovery was found by RT PL; Fig. 2.12 shows the enhancement in BL. The RT PL spectra of the HT-implanted PS-AlN/GaN samples are shown in Fig. 2.15. After implantation and before post-annealing, extremely weak luminescence was observed, similar to for the sample

after low-concentration implantation. After 10 min of post-annealing at 1150°C, the samples' optical properties were weakly recovered with an enhancement in yellow luminescence (YL) at around 2.25 eV. No Mg-related luminescence was found.

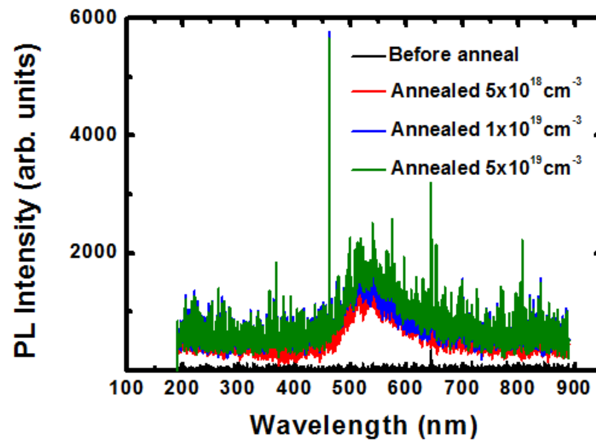


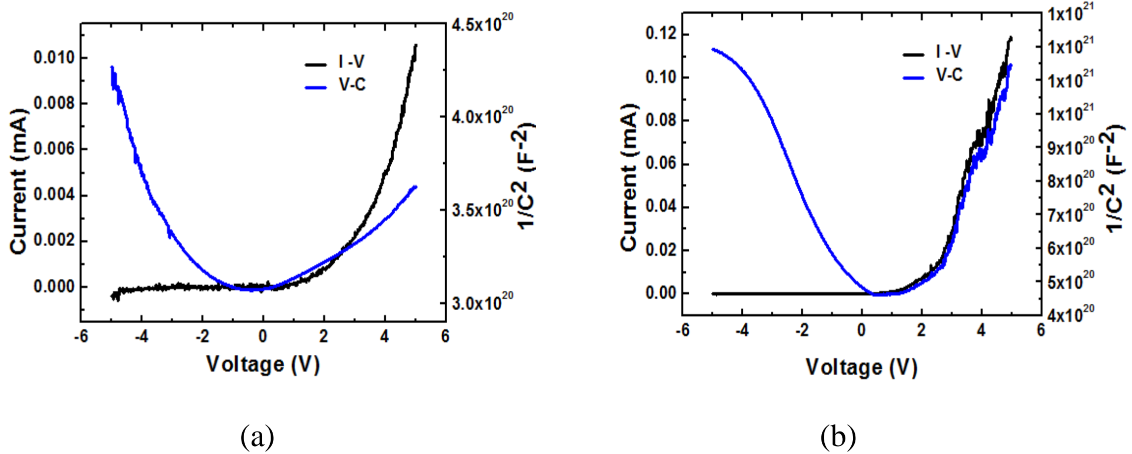
Fig. 2.15. PL spectra of samples implanted at various concentrations and annealed at 1150°C for 10 min.

C-V and Hall measurements were used to determine the electrical properties of the samples. All the samples showed insulator properties, indicating that the electrical properties of the samples were not activated. Thus, more effective post-annealing is necessary.

Therefore, the HT-implanted PS-AlN/GaN samples were post-annealed at 1200°C and 1250°C for 10 min. Only a weak recovery in the optical properties was indicated by the RT PL spectra, which showed an enhancement in YL, similar to in the spectra shown in Fig. 2.15.

Based on the C-V measurements, current and $1/C^2$ were plotted as a function of voltage for the HT-implanted PS-AlN/GaN sample (implantation concentration = 1×10^{19} cm^{-3}) post-annealed for 10 min at 1200°C and 1250°C (Fig. 2.16). For

low-concentration implantation, a stable N_a-N_d signal was observed, and the carrier type changed from p-type to n-type inside the Schottky barrier region at around -1 V in Fig. 2.13(c). In Fig. 2.16, low currents were observed in the I-V curve compared to in Fig. 2.13. The carrier type changed at the same time when the capacitance trend changed; it changed at around 0 V in Fig. 2.16(a) and at 1 V in Fig. 2.16(b). When the carrier type changed, the current increased, resulting in a decrease in electrons charging into the depletion layer. It is difficult to determine the reason for the change in carrier type caused by the increased current or the acceptors activated from the implanted ions. Thus, I could not obtain a reliable p-type GaN signal using C-V measurements. Hall measurements were also carried out; only the n-type signal could be obtained for the sample implanted at a concentration of 5×10^{18} cm^{-3}. Insulator properties were observed in the samples implanted at concentrations of 1×10^{19} and 5×10^{19} cm^{-3}.

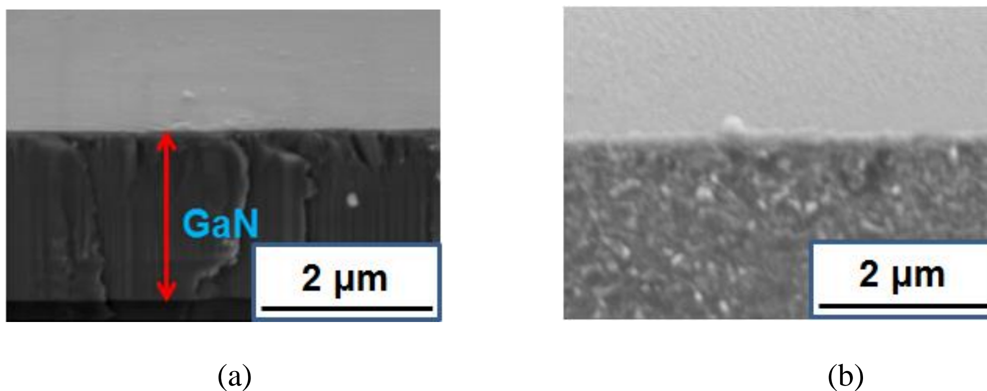


(a) (b)

Fig. 2.16. C-V curves for the sample implanted at a concentration of 1×10^{19} and post-annealed for 10 min at (a) 1200° C and (b) 1250°C.

The HT-implanted PS-AlN/GaN samples were also post-annealed at a higher

temperature of 1280°C. The cross-sectional images of the HT-implanted (concentration = 1×10^{19} cm^{-3}) PS-AlN/GaN sample are shown in Fig. 2.17. Before post-annealing, the 2-μm-thick GaN layer can be observed in Fig. 2.17(a). After post-annealing at 1280°C for 10 min, the GaN layer was decomposed, and only the sapphire substrate was left. Due to the charging effect of the insulator sapphire substrate, a clear SEM image could not be obtained. The PS-AlN layer (thickness = ~100 nm) could not be afford to the post-annealing for 10 min if the post-annealing temperature was higher than 1280°C. Thus, new approaches need to be considered to realize post-annealing at temperatures higher than 1250°C.



(a) (b)

Fig. 2.17. SEM images of samples (a) before annealing and (b) after post-annealing for 10 min at 1280°C.

2.5 Conclusions

This chapter discussed reducing the implantation damage during Mg-ion implantation using a pre-sputter technique. The TRIM simulation results indicated that the implantation damage near the surface could be reduced by 95% by using a 100-nm-thick PS layer. The PS technique was found to be effective at reducing the

implantation damage based on the 2θ-ω XRD results. The lattice constants of the implantation damage layer were determined. The implantation damage mainly changed the ***c*** constant, while the ***a*** constant remained nearly constant. The implanted and post-annealed PS-AlN/GaN samples were characterized. For samples implanted at a concentration of 2×10^{17} cm^{-3}, p-type GaN deformation was confirmed from the optical properties based on the weak near-band-edge emission and enhanced BL luminescence in the RT PL spectra and from the electrical properties based on the p-type electrical signal in the C-V curves. The p-type carrier signal could not be obtained from Hall measurements due to the thin p-type GaN layer with low hole density.

Post-annealing experiments were carried out on sp-AlN/GaN samples after HT implantation. The 100-nm-thick sputter-coated AlN layer could well protect the GaN surface during annealing at 1250°C for 10 min. The RT PL spectra indicated only weak luminescence dominated by YL. The p-type carrier could not be confirmed by C-V measurement due to the large current leakage. The Hall measurement did not show any p-type result because the post-annealing conditions were not sufficient to activate the implanted ions. Future work is expected to involve post-annealing at higher temperatures and for longer times.

References

1) K. Harafuji, T. Tsuchiya, and K. Kawamura, J. Appl. Phys. **96**, 5 (2004).

2) B. N. Feigelson, T. J. Anderson, M. Abraham, J. A. Freitas, J. K. Hite, C. R. Eddy, and F. J. Kub, Journal of Crystal Growth **350**, 21 (2011).

3) S. O. Kucheyev, J. S. Williams, and S. J. Pearton, Mater. Sci. Eng. **33**, 51 (2011).

4) Y. Niyama, S. Ootomo, J. Li, H. Kambayashi, T. Nomura, S. Yoshida, K. Sawano, and Y. Shiraki, Jpn. J. Appl. Phys. **47**, 5409 (2008).

5) T. Shiino, T. Saitoh, T. Nakamura, and T. Inada, Nucl. Instrum. Methods Phys. Res. Sect. **B 267**, 1571 (2009).

6) ML. Lee, JK. Sheu, LS. Yeh, MS. Tsai, CJ. Kao, CJ. Tun, SJ. Chang, and GC Chi, Solid – State Electron. **46**, 2179 (2002).

7) C. E. Hager IV, K. A. Jones, M. A. Derenge, and T. S. Zheleva, J. Appl. Phys. **105**, 033713 (2009).

8) Y. Irokawa, O. Fujishima, T. Kachi, and Y. Nakano, J. Appl. Phys. **97**, 083505 (2005).

9) K. T. Liu, Y. K. Su, S. J. Chang, and Y. Horioshi, J. Appl. Phys. **98**, 073702 (2005).

10) S. J. Pearton, Comprehensive Semiconductor Science and Technology **4**, 25 (2011).

11) S. C. Jain, M. Willander, J. Narayan, and R. Van Overstraeten, J. Appl. Phys. **87**, 965 (2000).

12) Y. Irokawa, O. Fujishima, T. Kachi, S. J. Pearton, and F. Ren, Appl. Phys. Lett. **86**, 112108 (2005).

13) S. Matsunaga, S. Yoshida, T. Kawaji, and T. Inada, J. Appl. Phys. **95**, 2461 (2004).

14) X. Cao, R. G. Wilson, J. C. Zolper, S. J. Pearton, J. Han, R. J. Shul, D. J. Rieger, R.

K. Singh, M. Fu, V. Scarvepalli, J. A. Sekhar, and J. M. Zavada, Journal of Electronic Materials **28**, 261 (1999).

15) Y. Irokawa, J. Kim, F. Ren, H. H. Balk, B. P. Gila, C. R. Abermathy, S. J. Pearton, C. C. Pan, G. T. Chen, and J. I. Chyl, Appl. Phys. Lett. **83**, 4987 (2003).

16) Y. Nakano and T. Jimbo, J. Appl. Phys. **92**, 3815 (2002).

17) National Academy of Engineering and National Research Council: Advance Materials Research, p.63 (1987).

18) C. Hayzelden and J. L. Batstone, J. Appl. Phys. **73**, 12 (1993).

19) H. Morkoc: Handbook of Nitride Semiconductors and Devices, Vol. 1 (2008).

20) Z. Sun, M. Olsson, T. Nagayama, Y. Honda, and H. Amano, IEICE Tech. Report **109**, SDM2014-38 (2014).

21) K. Schroder, *Semiconductor Material and Device Characterization* (Wiley – Interscience, New Jersey, 2006) 3rd ed, p. 65.D. K. Schroder, Semiconductor Material and Device Characterization, p. 65 (2006).

3. Direct Growth of GaN c-plane SiC Substrates

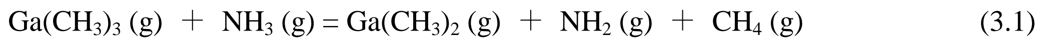
3.1 Introduction

GaN and SiC are both candidate semiconductor materials for next-generation high-power applications due to their electronic properties and ability to operate at high temperature. GaN has been directly grown on SiC using hydride vapor phase epitaxy (HVPE)[1-2], molecular beam epitaxy (MBE)[3], and MOVPE[4-6]. This new technique has been used to fabricate GaN/SiC vertical structure devices.[7-10] The optimization of the hetero-epitaxial interface was found to be easiest using the MOVPE growth method, and the growth time could be reduced by avoiding the use of a high-vacuum environment. Thus, our research focuses on using the MOVPE method to grow GaN on SiC substrates. Other groups have reported the direct growth of GaN on SiC using a three-step growth method.[5] Jeong et. al. reported the direct growth of cracked GaN on SiC with a low Ga/N ratio at low pressure. It is necessary to identify a growth method to obtain crack-free GaN on SiC substrates. In this chapter, discuss the direct growth of GaN on bulk SiC substrates.

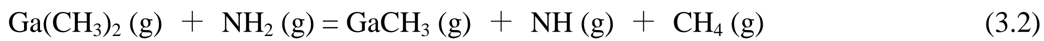
3.2 MOVPE System and Chemical Reaction of GaN in MOVPE

MOVPE is the premier technique for the epitaxial growth of group III nitrides. The success of MOVPE in the production of high-brightness LEDs[11] and short-wavelength injection lasers[12] has resulted in the rapid expansion of research and development related to this materials system. MOVPE was applied by Manasevit et al.[13] to the deposition of GaN and AlN in 1971. Using triethylgallium (TEG) and ammonia (NH_3) as source gases for group III and V species, respectively, the authors obtained c-axis-oriented films on sapphire (0 0 0 1) and on 6H-SiC (0 0 0 1) substrates. For GaN

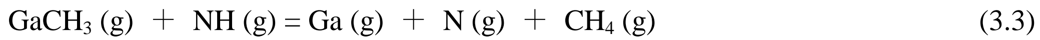
growth using the MOVPE method, trimethylgallium ($(CH_3)_3Ga$) and NH_3 are the group III and V species, respectively, and hydrogen (H_2) is the carrier gas used to transfer the organic metal source into the reaction chamber. GaN crystals are synthesized at extremely high temperatures of about 1000° C. Many chemical reactions occur in the action chamber:



$$Ga(CH_3)_3\,(g) + NH_3\,(g) = Ga(CH_3)_2\,(g) + NH_2\,(g) + CH_4\,(g) \qquad (3.1)$$



$$Ga(CH_3)_2\,(g) + NH_2\,(g) = GaCH_3\,(g) + NH\,(g) + CH_4\,(g) \qquad (3.2)$$



$$GaCH_3\,(g) + NH\,(g) = Ga\,(g) + N\,(g) + CH_4\,(g) \qquad (3.3)$$

$$Ga\,(g) + N\,(g) = GaN\,(s) \qquad (3.4)$$

The analysis of the mechanisms involved in the MOVPE process clearly indicates that any precursor must balance the requirements of volatility and stability, which often counter each other, to be transported to the surface and decomposed for deposition. The pressure, growth temperature, and the V:III ratio are the main parameters in the growth process.

In this thesis, all the GaN samples were grown using an SH4001-HTA MOVPE apparatus (Nagoya University MOVPE NO. 5; EpiQuest). Figures 3.1 and 3.2 show the schematics of the MOVPE system and the system's reaction chamber, respectively. The system was a horizontal-type GaN MOVPE system, and all the flow sources were controlled by the mass flow controller (MFC). The liquid-state organic metal source TMG was carried by the carrier gas (H_2); TMG was saturated into the H_2 and transferred into the action chamber. In this way, the liquid source was supplied by the gas state and could be easily controlled by the MFC. The saturated concentration of TMG in H_2, which is usually calculated using Formula (3.5), is strongly affected by the temperature. In our case, TMG was kept at 5° C:

$$\log_{10}P = 8.07 - 1705/T\ (K) \qquad (3.5)$$

In order to avoid the solidification of the source on the way to the reaction chamber, a tape heater set at 55°C was used, allowing the source gas to reach the reaction chamber after travelling through the flow channel.

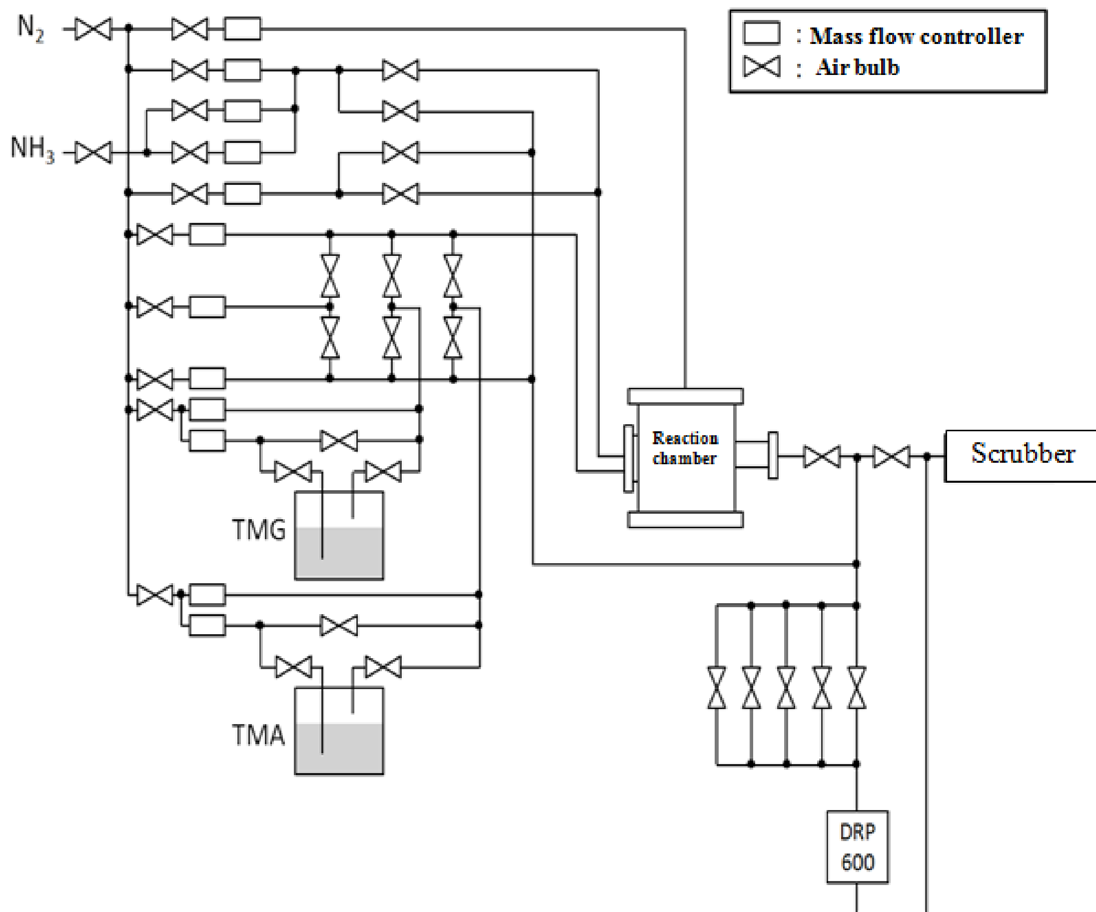


Fig 3.1. Schematic of the MOVPE system.

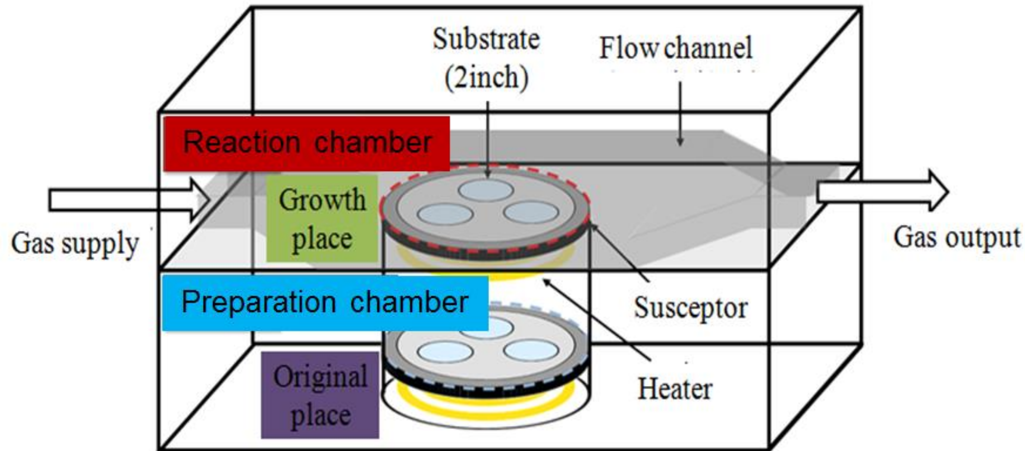


Fig. 3.2. Schematic of the reaction chamber.

3.3 Direct Growth of GaN at an 4°-off c-SiC Substrates

SiC leads GaN one step in commercialization because of its large size and high-quality bulk growth technique. With the six-inch SiC substrate in product, on-SiC power devices are expected to be low-cost and applied in more fields. In case of the epitaxial growth of SiC, off-cut SiC substrates are usually used because homo-epitaxial growth of SiC still relies on the step flow growth method. Among SiC substrates, off-cut SiC substrates are cheap and easy to obtain. Nowadays, 4°-off SiC substrates are standard for the homo-epitaxial growth of SiC in commercial applications. The steps on SiC substrates present a challenge for GaN due to the change of migration of initial GaN growth, which is caused by the step flow on the SiC substrate. An example of an 8°-off SiC substrate is shown in Fig. 3.3; the steps along the [1-100] direction can be seen. If we could directly grow GaN on 4°-off SiC substrates, we could obtain GaN/Drift-SiC/n-SiC vertical power devices. Thus, we tried to grow GaN directly on 4°-off SiC substrates in the first experiments.

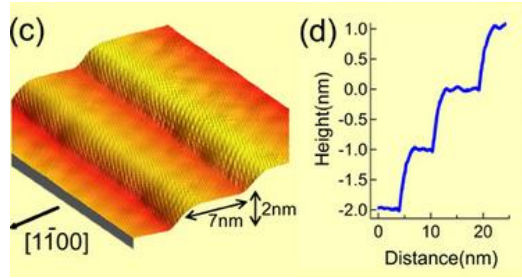
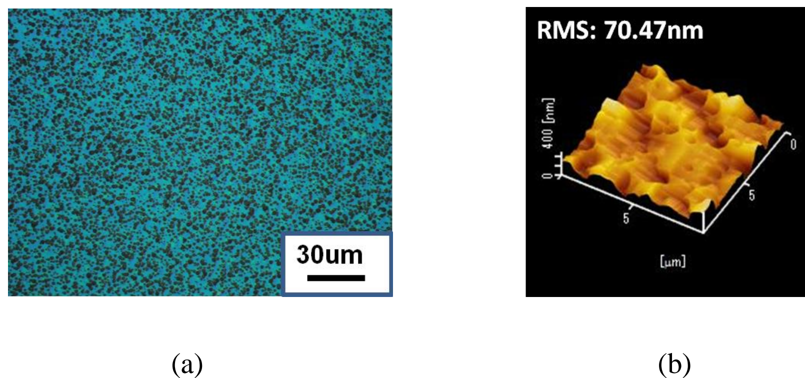


Fig. 3.3. Schematic of the surface step distribution image of 8°-off SiC surface.[14)]

Experiments were performed using a horizontal MOVPE system. TMGa and NH_3 were used as the precursors for gallium and nitrogen, respectively. A (0001) n-type single-polished 4H-SiC wafer (4°-off) with an Si face was used as the substrate for GaN epitaxial growth. After increasing the temperature to 1000°C, the SiC substrate was thermally cleaned for 3 min in hydrogen. GaN was then directly grown on the SiC substrate for 40 min at 1000°C. The growth pressure was 150 Torr. The V:III ratio was 2161. The TMGa flow rate was 108 μmol/min.



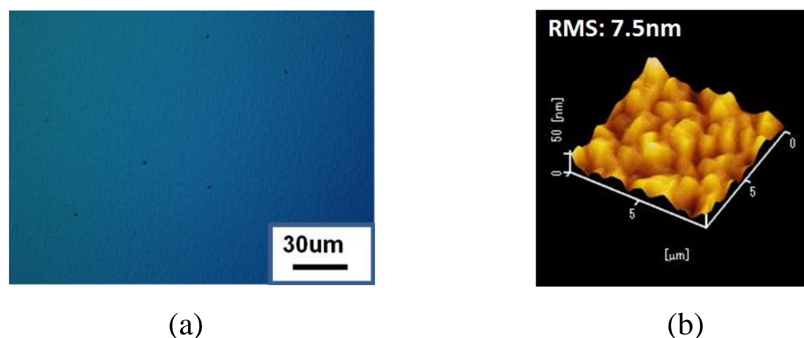
(a) (b)

Fig. 3.4. (a) OM image and (b) atomic force microscopy (AFM) image GaN grown directly on a 4°-off SiC substrate.

An OM image of the surface of the GaN/SiC sample is shown in Fig. 3.4(a). A high density of pits was observed on the growth surface. The morphology of a 10 × 10 μm^2

area of the growth sample was analyzed by atomic force microscopy [AFM; Fig. 3.4(b)]. The sample exhibited a rough morphology with a root mean square (RMS) value of 70.47 nm and a high density of pits, as in the OM image. Pits with different sizes were found and may have been caused by the steps on the SiC surface. PL measurement revealed the near-band-edge peak of GaN at 3.39 eV, indicating GaN growth on SiC.

In the previous experimental results, GaN was directly grown on SiC substrates; however, a rough surface morphology and high pit density were observed. To reduce the pit density, the growth conditions were optimized for temperature, V:III ratio, and pressure. The TMAl treatment was also carried out. The best growth conditions were a temperature of 1030°C, a V:III ratio of 1010, and a pressure of 100 Torr. Before the GaN growth step, a 20-s preflow TMAl treatment was carried out; the details are discussed in Section 3.4.



(a) (b)

Fig. 3.5. (a) OM image and (b) AFM image of the direct growth of GaN on a 4°-off SiC substrate under the optimized growth conditions.

The OM and AFM images of the surface of the GaN/SiC sample formed under the optimized growth conditions are shown in Fig. 3.5. The surface was improved and few pits were observed. However, the AFM image [Fig. 3.5(b)] indicates that the surface

was not flat, and micron-sized islands were observed. The RMS value was 7.5 nm. XRD analysis indicated that the full width at half maximum (FWHM) values were 152 arcsec on (0002) and 336 arcsec on (10-12). GaN's near-band-edge peak was observed at 3.39 eV in the PL spectrum. In summary, we grew GaN directly on a 4°-off SiC substrate with a low pit density; however, AFM analysis revealed micron-sized islands and a surface RMS value of 7.5 nm. Thus, the surface is still too rough for application in power devices. Improving the surface roughness will be the focus of a future work.

3.4 Direct Growth of GaN on 0°-off c-SiC Substrates

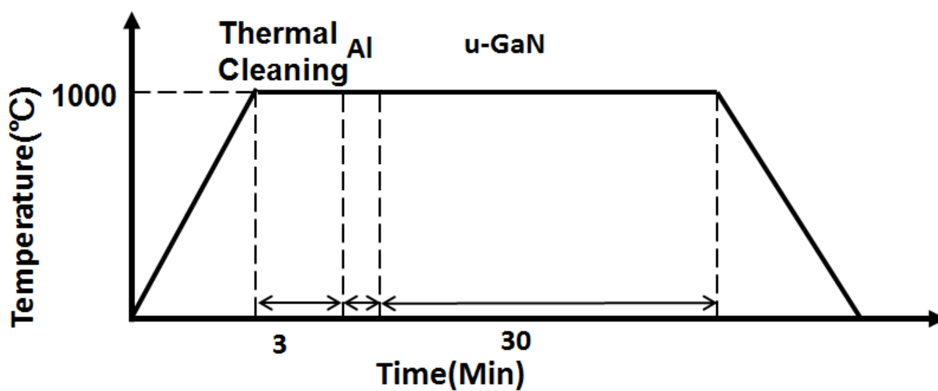
In the previous section, GaN was directly grown on offcut SiC substrates; however, we could not obtain atomically flat GaN films. In this section, we discuss the direct growth of GaN on on-axis c-plane SiC substrates. Compared to epitaxial growth on offcut substrates, growth on-axis SiC substrates offers more benefits for GaN because the offcut substrates impact the performances of GaN-based devices. For power devices, the offcut angle diminishes the internal electric field resulting in lower 2DEG. For optical devices, a smaller indium incorporation into InGaN grown on off-cut GaN.[15)] Thus, it is necessary to grow GaN directly on on-axis SiC substrates, although it is a challenge to achieve homo-epitaxial growth on on-axis SiC templates.

3.4.1 Direct Growth of GaN on on-axis SiC Substrates by TMAl Treatment

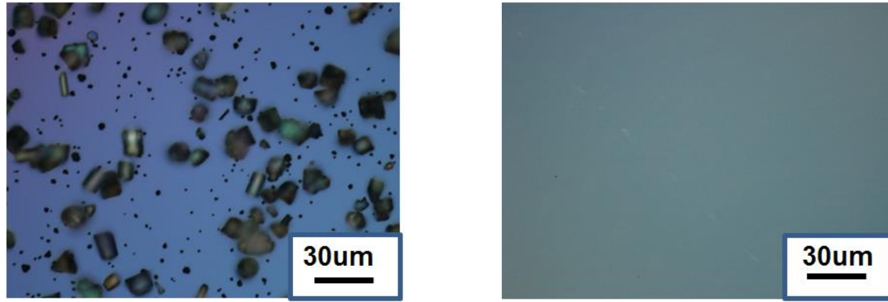
Due to the poor surface wetting of gallium, the direct growth of GaN on 6H-SiC (0001) substrates still results in a high density of three-dimensional (3D) islands when using conventional GaN growth conditions on sapphire substrates.[15)] Thus, GaN is usually grown on SiC at high temperatures around a 100-nm-thick AlN intermediate layer.[16)] The high-resistance AlN interlayer makes it difficult to fabricate vertical structure devices. A cracked GaN layer was reported to form by direct growth on SiC after

cleaning the substrate[17] or by using a low growth pressure and a low Ga/N ratio[14]. Three-step growth involving the formation of a high-temperature 3D interlayer[18] has been reported to enable direct GaN growth on SiC. It is necessary to find a way to grow crack-free GaN on SiC substrates.

Experiments were also performed using a horizontal MOVPE system. TMGa and NH_3 were used as the precursors for gallium and nitrogen, respectively. An (0001) n-type single polished 6H-SiC wafers (0° off) with an Si face was used as the substrate for GaN epitaxial growth. The growth temperature profile with respect to time is shown in Fig. 3.6(a). After increasing the temperature to 1000°C, the SiC substrate was thermally cleaned for 3 min in hydrogen. GaN was then directly grown on the SiC substrate for 40 min at 1000°C. The growth pressure was 150 Torr. The V:III ratio was 2161. The TMGa flow rate was 108 μmol/min. Two samples were grown: (a) without TMAl treatment and (b) with TMAl treatment. For sample (b), before GaN growth, a 20-s TMAl treatment with a preflow of TMAl at a rate of 18 μmol/min without NH_3 was applied. The samples were then characterized, and the results are discussed in the following section.



(a)



(b) (c)

Fig. 3.6. (a) Temperature profile with time. OM images of the as-grown samples (b) without TMAl treatment and (c) with TMAl treatment.

The OM images of the as-grown samples are shown in Figs. 3.6(b) and (c). Sample (a) showed irregular island-like growth, indicating the poor wetting of gallium on the SiC surface. With the application of TMAl treatment without NH_3, the morphology improved; sample (b) showed a crack-free and smooth surface with a GaN thickness of around 1.5 μm. The growth rate was about 2.3 μm/hour. The morphology of sample (b) was further analyzed by AFM (Fig 3.7), indicating an atomically flat GaN morphology. The RMS value of a 2×2 μm^2 area was 1.1 Å. Using X-rays generated by an Au-target, the crystalline quality of sample (b) was characterized using an X-ray rocking curve technique. The FWHMs were 241 aresec on GaN's (0002) plane and 297 arcsec on GaN's (10-12) plane. From the XRD two theta-omega scan results, GaN's lattice constants were calculated according to Bragg's rule. The details of the calculation method are shown in the previous chapter.

The optical properties of sample (b) were analyzed by PL spectroscopy at RT. A strong band-edge emission peak was found at 3.41 eV [Fig. 3.8(a)]. The electrical properties were confirmed by C-V measurements using a mercury probe, which easily formed two Schottky contact electrodes on the sample surface. Based on the difference between the

two electrodes' areas, we approximated the reverse charge region under the small electrode (1 mm). The doping concentration was obtained from the dC/dV slope of the C-V curve. The depth at which the doping concentration was evaluated was obtained from the capacitance[19)]. The n-type 6H-SiC substrate and GaN carrier density were separately measured. The results are plotted in Fig. 3.8(b). The different profiles of the depletion layers were caused by the different carrier densities. The SiC substrate's donor density was around 10^{18} cm^{-3}. The undoped GaN donor density was around 10^{15} cm^{-3}.

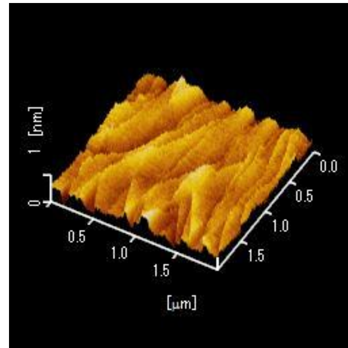
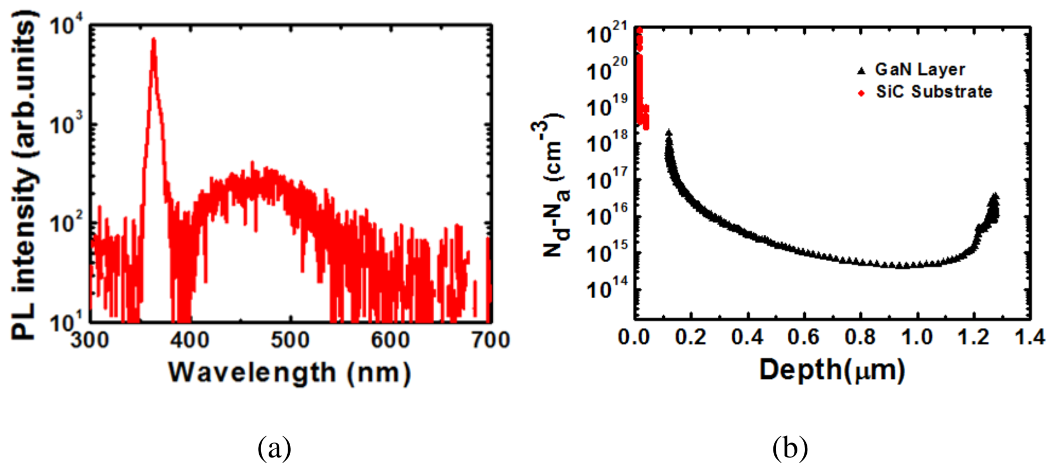


Fig. 3.7. Three-dimensional view of the GaN/SiC sample treated with TMAl.

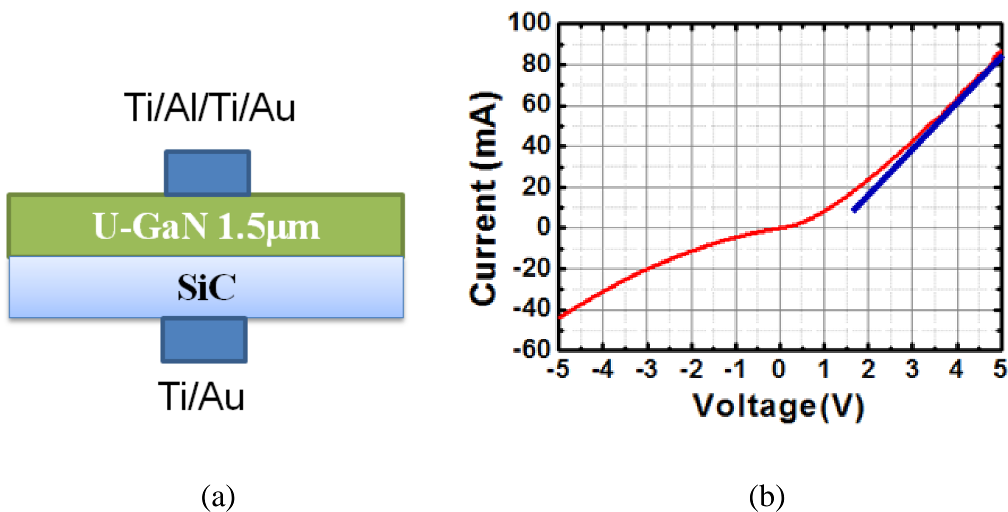
To apply GaN/SiC structures to future vertical power devices, high-quality growth materials with low vertical resistances are required. Thus, we also measured the vertical resistance of the GaN (1.5 μm)/SiC (300 μm) structure. The device structure is shown in Fig. 3.8(a). The device fabrication process was as follows: (1) Ti/Al/Ti/Au contact deposition on GaN by electron-beam sputtering (EB); (2) annealing at 650°C in N_2 for 5 min to form an Ohmic electrode contact on GaN; and (3) Ni/Au contact deposition on the unpolished backside of SiC by EB. Normally, to obtain Ohmic contacts on SiC, it is necessary to anneal at temperatures over 900°C[20)]. For the GaN/SiC structure, such high temperatures damage the GaN surface. To avoid damage to the GaN layer, the electrode was placed on the backside of SiC, forming a Schottky

contact. The sample's vertical I-V curve is shown in Fig. 3.8(b) and was used to estimate the vertical resistance of the GaN/SiC structure. The size of the contact was 0.5 mm^2. The vertical resistance was found to be around 82.1 Ω. A lower resistance is expected to be achieved by the growth of n-GaN on SiC substrates.



(a) (b)

Fig. 3.8. (a) RT PL spectrum of GaN/SiC with TMAl treatment and (b) carrier concentration versus depth profile of undoped GaN and SiC substrates.



(a) (b)

Fig. 3.9. (a) Fabricated GaN/SiC vertical device structure and (b) its I-V curve.

GaN was directly grown on 6H-SiC using a single two-dimensional growth step. Before the GaN growth, a TMA treatment process without NH_3 was applied to prevent the reaction between the source gas (TMGa and NH_3) and the SiC substrate. GaN(1.5 μm)/SiC showed a smooth surface and an atomically flat morphology with an RMS value of 1.1 Å (based on a 2×2 μm^2 area). The FWHM on (0002) was 241 arcsec. The FWHM on (10-12) was 297 arcsec. The GaN band-edge emission was found at 3.41 eV. The undoped GaN's donor density was around 10^{15} cm^{-3}. The vertical resistance was estimated to be about 82.1 Ω. We hope that the new single-step GaN/SiC epitaxial growth method will be applied in future GaN/SiC high-power devices with high switching speeds.

3.4.2 Effect of TMAl treatment on GaN/SiC and Interface Analysis

Crack-free GaN with a thickness of 1.2 μm was directly grown on a 6H-SiC substrate using a single two-dimensional growth step with a preflowed TMAl treatment. It is necessary to further understand the preflow TMAl process and analyze the GaN/SiC interface. In this part, the preflow TMAl treatment time was varied, and the as-grown samples were characterized.

Materials were grown using a MOVPE system. TMGa and NH_3 were used as sources of gallium and nitrogen, respectively. A c-plane (0001) n-type single-sided polished 6H-SiC wafer (0° offcut) with an Si face was used as the substrate for GaN epitaxial growth. After increasing the temperature to 1000^oC, the substrate was thermally cleaned for 3 min under hydrogen-ambient without NH_3. The TMAl treatment process was carried out with a TMAl flow rate of 18 μmol/min. Samples were prepared with different TMAl treatment times (0, 5, 10, 20, and 30 s). GaN (1.2-μm-thick) was grown for 30 min using a TMGa flow rate of 108 μmol/min at a pressure of 150 Torr. The V:III ratio was 2161.

SEM images of the samples are shown in Fig. 3.10. Without the TMAl treatment, the poor surface wetting of gallium atoms[18-19] inhibited the growth coalescence and left 3D islands, as shown in Fig. 3.10(a). When the TMAl treatment was carried out for 5, 10, 20, and 30 s, the resulting samples showed crack-free surfaces. For example, an SEM plan-view image of the surface of the sample subjected to TMAl treatment for 5 s is shown in Fig 3.10(b). AFM was used to observe the morphology of a 5×5 μm^2 area on the surface. Without TMAl treatment, the sample showed a rough surface with many 3D islands. The morphologies of samples subjected to TMAl treatment exhibited atomically flat surfaces with RMS values under 0.5 nm.

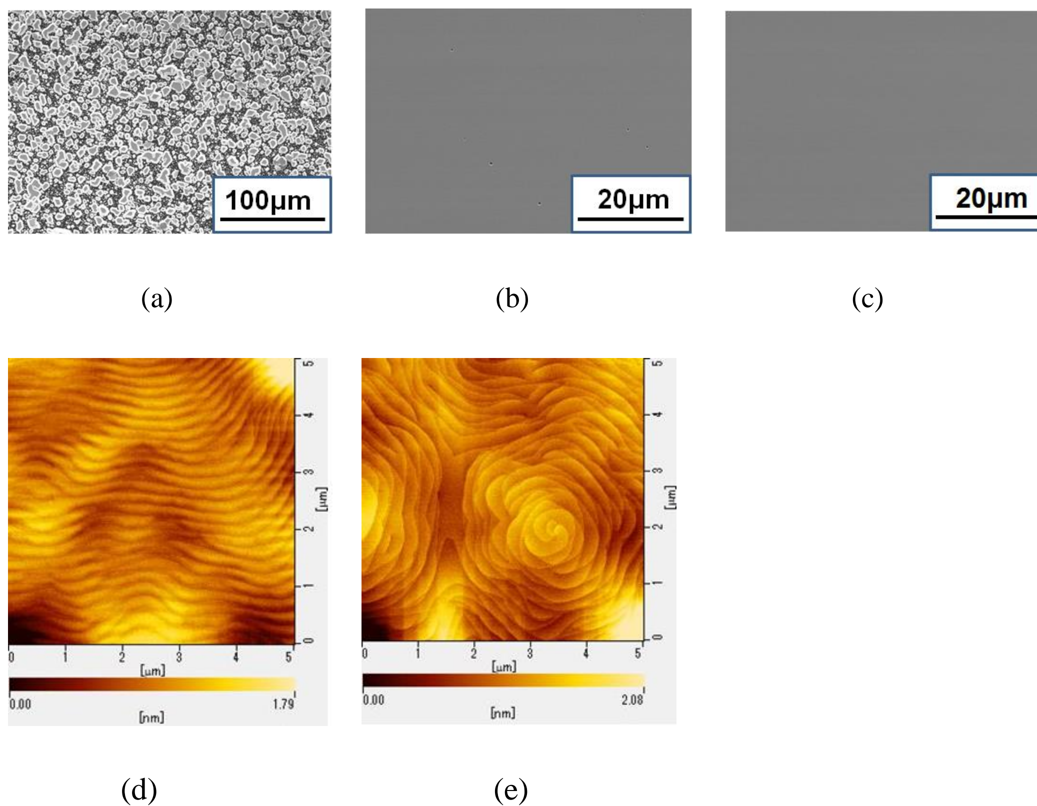


Fig. 3.10. SEM images of samples treated by TMAl for (a) 0, (b) 5, and (c) 20 and AFM images of samples treated by TMAl for (d) 5 and (e) 20 s.

Because of strain generated by the lattice and thermal expansion mismatches between GaN and SiC, the direct growth of GaN on SiC was reported to produce cracks.[14] To understand why our GaN/SiC samples were crack-free, we calculated the samples' lattice constants ***a*** and ***c*** from the 2θ-ω XRD patterns and compared them with the lattice constants of the free-standing GaN substrates. The calculated ***a*** and ***c*** values are plotted for the different TMAl treatment times in Figs. 3.11(a) and (b), respectively. The ***a*** and ***c*** values of the TMAl-treated samples were larger and smaller, respectively, than those of free-standing GaN, which is attributed to the tensile strain resulting from the thermal mismatch between GaN and SiC. When the TMAl treatment time was shorter than 10 s, ***a*** became larger, while ***c*** became larger and then smaller compared to the constants of the GaN/SiC sample obtained by 3D growth. We attribute the initial change in ***a*** to the thermal strain from the different thermal expansion coefficients. The calculated thermal strain caused by the difference in the thermal expansion coefficients from growth temperature to RT could change the lattice constant ***a*** from 3.189 to 3.193 Å. By Hooke's law[20], lattice constant ***c*** was calculated to be 5.183 Å. These values are near to the experimental results for the sample treated with TMAl for 10 s. For untreated sample, the effect of thermal mismatch was small due to the 3D growth. We could not make sense of the results of the sample treated for 5 s. Increasing the TMAl treatment time above 10 s decreased ***a***, and its value approached that of free-standing GaN. At the same time, the lattice constant ***c*** increased, approaching that of free-standing GaN. We think that long TMAl treatment time (>20 s) generated dislocations and enabled the tensile strain originating from the thermal mismatch to be released.

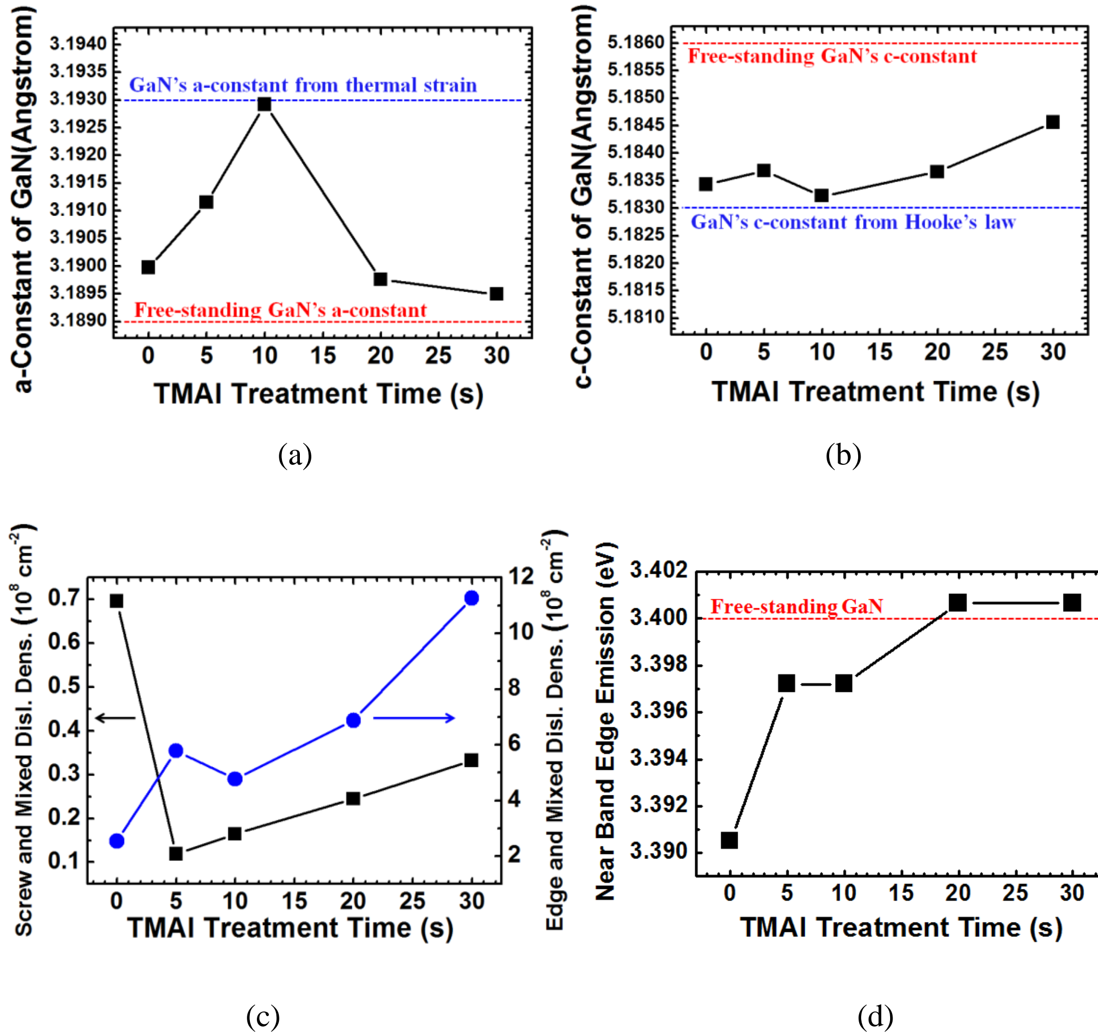


Fig. 3.11. (a) Lattice constant ***a*** (calculated by XRD), (b) lattice constant ***c*** (calculated by XRD), (c) screw and mixed dislocation density and edge and mixed dislocation density (calculated by XRC), and (d) near-band-edge emission position (calculated by RT PL) as functions of TMAl treatment time.

The reason for the strain release seems to be the dislocations generated by the TMAl treatment. The samples' dislocation densities were estimated from the X-ray rocking curves (XRCs) of the GaN (0002) and (10-12) planes. The screw and mixed

dislocation densities and the edge and mixed dislocation densities of GaN were determined from the (0002) and (10-12) planes, respectively.[21-24] The dislocation density was calculated from the FWHM of XRC ω-scan (0002) and (10-12) diffractions by

$$N = \frac{\beta^2}{4.35|b|^2} \ , \tag{3.6}$$

where N is the dislocation density, $|b|$ is the magnitude of the Burgers vector, and β is the FWHM of the XRC.[25-26] Screw and mixed dislocation densities and edge and mixed dislocation densities for different TMAl treatment times are plotted in Fig. 3.11(c). Compared to the 3D-grown sample, the films grown with TMAl treatment had lower densities of screw dislocations and higher densities of edge dislocations. TMAl treatment is considered to promote the wetting of gallium atoms on the SiC surface, increasing the density of GaN islands. The edge dislocations may be generated during the coalescence of islands.[28] Increasing the TMAl treatment time increased the initial island density and also the number of edge dislocations. The cross-sectional TEM images of the samples treated by TMAl for 5 and 20 s are shown in Figs. 3.12(a) and (b), respectively. The dislocation type is also indicated in the TEM images. The dominant dislocations were found to be edge dislocations, which were considered to be formed by the TMAl treatment. The edge and mixed dislocation densities samples treated for 5 and 20 s were estimated to be 9.7×10^{9} and 1.1×10^{10} cm^{-2}, respectively, from the cross-sectional TEM images. These values are higher than the dislocation densities calculated from the XRC FWHM values. This is attributed to the non-uniform distribution of dislocations within the GaN layer. We also found that the edge dislocations coalesced and disappeared when the GaN thickness was under approximately 300 nm, as shown in Fig. 3.12(a). The bandgap of GaN near the surface region was estimated from the near-band-edge emission wavelength of the RT PL

spectrum. The results are plotted for different TMAl treatment times in Fig. 3.11(d). The bandgap values were found to be near the bandgap value (3.4 eV) of free-standing GaN in all four samples. Together with the cross-sectional TEM results, this indicated that the TMAl treatment released the strain from the SiC substrates by generating edge dislocations at the GaN/SiC interface.

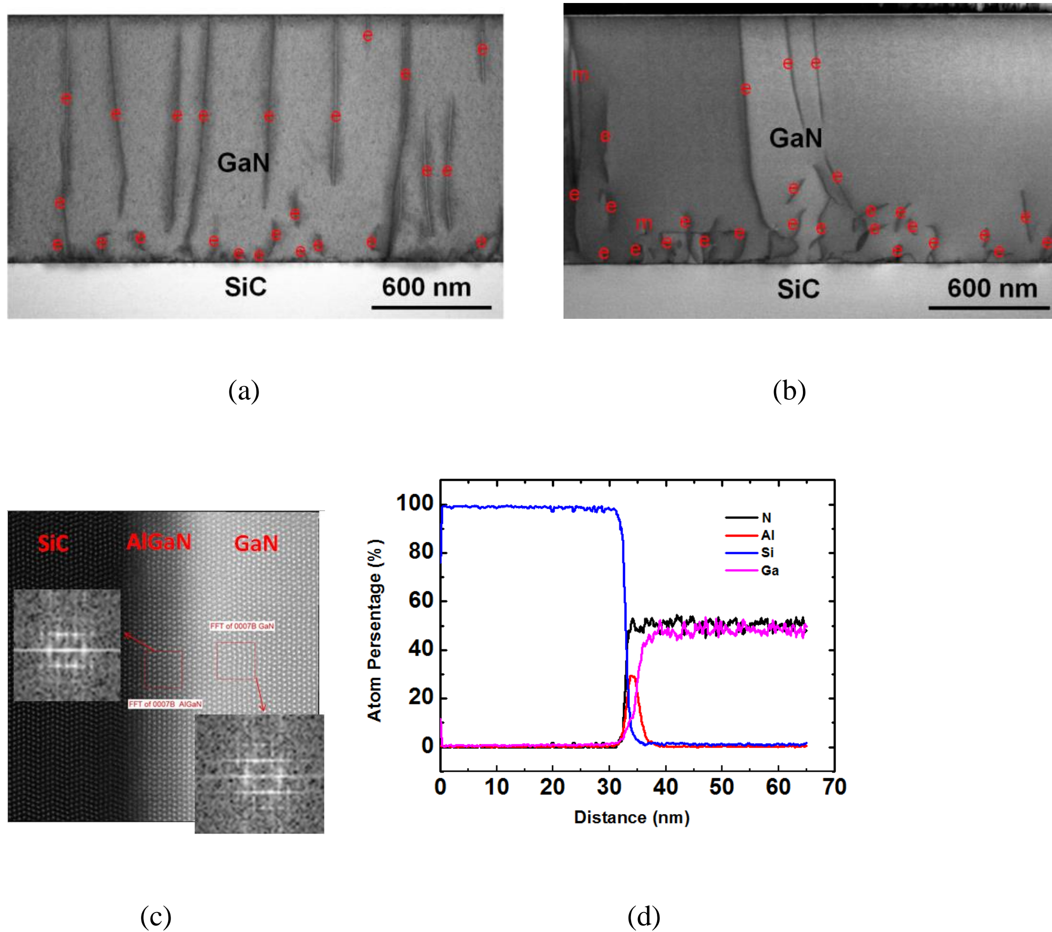


Fig. 3.12 Cross-sectional on-axis TEM images of GaN/SiC samples subjected to TMAl treatment for (a) 5 and (b) 20 s. (c) Cross-sectional HRTEM images of the GaN/SiC sample treated by AMAl for 20 s and analyzed by FFT. (d) High-resolution energy dispersive spectrometry (HREDS) profile of GaN/SiC (the left side is the SiC substrate).

The FFT mappings were taken from the interface and the GaN growth region of the HRTEM scan of the interface region [Fig. 3.12(c)]; however, the lattice constants from the two FFT readings could not be resolved. While the AlN-GaN interfaces appeared distinct in the FFT mappings, the AlGaN-GaN interfaces were not clear in the TEM images. Thus, the interlayer in Fig. 3.12(c) was believed to be AlGaN. The AlGaN was thought to be derived from the nitridation reaction between Al (decomposed from TMAl) and Ga (decomposed from GaN by baking recipe). High-resolution energy dispersive spectrometry (HREDS) was used to analyze the element profile at the GaN/SiC interface [Fig. 3.12(d)]. The space resolution energy was defined to be 0.2~0.3 nm. Even when we consider the space resolution energy changes from the electron beam effect inside different materials, the space resolution energy inside the material was thought to be at least 1 nm. Thus, the thickness of the Al-treat layer was estimated to be 2~3 nm. Based on the HRTEM image, we thought that the Al-treat step formed an AlGaN interlayer. Figure 3.12(d) shows that the Al content of AlGaN decreased as the measured position moved from the interface towards the surface. Thus, the pre-treatment of the SiC substrate with TMAl was thought to induce the formation of a thin AlGaN layer, which enabled GaN to grow on SiC.

3.5 Conclusions

GaN was growth directly on 4°-off SiC substrates. Direct growth with low pit density was achieved by optimizing the growth conditions; however, forming atomically flat GaN films remained a challenge.

By applying TMAl treatment, high-quality, 1.2-μm-thick undoped GaN films were successfully formed on 0° offcut 6H-SiC substrates. Smooth surface morphology was

confirmed by SEM and AFM, and the RMS value of a 5 × 5 μm^2 section of the surface was 0.298 nm. The FWHM values determined by XRC analysis were 153 arcsec for the (0002) face and 518 arcsec for the (20-24) face. The dislocation densities were estimated as 4.7×10^7 cm^{-2} for screw-type and 1.4×10^9 cm^{-2} for edge-type. A strong edge emission at 3.40 eV was detected by PL spectroscopy. Under the thickness of around 200 nm, a high density of interface-generated dislocations was confirmed TEM in bright-field mode. The interlayer formed by TMAl treatment was thought to be AlGaN with a thickness of 2~3 nm, as observed by HREDS. XRD analysis indicated that a long TMAl treatment time (> 20 s) released the tensile stress from thermal mismatch between GaN and SiC. The XRC and TEM results indicated that the dominant dislocations generated by the TMAl treatment were edge dislocations at the GaN/SiC interface. The generated edge dislocations released strain from the SiC substrate and shifted the positions of the near-band-edge peaks in the RT PL spectra towards the bandgap of the free-standing GaN substrate. The ultrathin interlayer growth technique is expected to be applied to high-power and high-frequency GaN/SiC devices in the future.

References

1) O. Yu. Ledyaev, A. A. Lebedev, A. M. Strel'chuk, A. N. Kuznetsov, A. E. Nikolaev, A. S. Zubrilov, and A. A. Volkova, Semiconductors **39**, 1452 (2005).

2) E. Danielsson, C. -M. Zetterling, M. Ostling, K. Linthicum, D. B. Thomson, O. -H. Nam, R. F. Davis, Solid-State Electron. **46**, 827 (2002).

3) Y. Nakano, J. Suda, and T. Kimoto, Phys. Stat. Sol. (c) **2**, 7 (2005).

4) J. T. Torvik, M. W. Leksono, J. I. Pankove, C. Heinlein, J. K. Grepstad, and C. Magee, J. Electron. Mater. **28**, 3 (1999).

5) M. Lahreche, M. Leroux, M. Laugt, M. Vaille, B. Beaumont, and P. Gibart, J. Appl. Phys **87**, 577 (2000).

6) J. K. Jeong, J. H. Choi, H. J. Kim, H. C. Seo, H. J. Kim, E. Yoon, C. S. Hwang, and H. J. Kim, J. Cryst. Growth **276**, 407 (2005).

7) J. T. Torvik, M. Leksono, and J. I. Pankove, Appl. Phys. Lett. **72**, 11 (1998).

8) J. T. Torvik, J. I. Pankove, and B. V. Zeghbroeck, Solid-State Electron. **44**, 1229 (2000).

9) B. V. Zeghbroeck, S. -S Chang, R. L. Waters, J. Torvik, and J. Pankove, Solid-State Electron. **44**, 265 (2000).

10) J. T. Torvik, M. Leksono, J. I. Pankove, and B. V. Zeghbroeck, MRS Internet J. Nitride Semicond. Res. **4**, 3 (1999).

11) T. Hino, S. Tomiya, T. Miyajima, K. Yanashima, S. Hashimoto, and M. Ikeda, Appl. Phys. Lett. **76,** 3421 (2000).

12) D. A. Stocker, E. F. Schubert, and J. M. Redwing, Appl. Phys. Lett. **73**, 2654 (1998).

13) S. K. Hong, T. Yao, B. J. Kim, S. Y. Yoon, and T. I. Kim, Appl. Phys. Lett. **77**, 82 (2000).

14) http://komori.issp.u-tokyo.ac.jp/research-e3.shtml

15) M. Sarzynski, M. Leszczynski, M. Krysko, J. Z. Domagala, R. Czernecki, and T. Suski, Cryst. Res. Technol. **47**, 321 (2012).

16) J. K. Jeong, J. H. Choi, H. J. Kim, H. C. Seo, H. J. Kim, E. Yoon, C. S. Hwang, and H. J. Kim, J. Cryst. Growth **276**, 407 (2005).

17) F. A. Ponce, B. S. Krusor, J. S. Major Jr., W. E. Plano, and D. F. Welch, Appl. Phys. Lett. **67**, 410 (1995).

18) J. T. Torvik, M. W. Leksono, J. I. Pankove, C. Heinlein, J. K. Grepstad, and C. Magee, J. Electron. Mater. **28**, 3 (1999).

19) K. Schroder, Semiconductor Material and Device Characterization (Wiley – Interscience, New Jersey, 2006) 3rd ed, p. 63.

20) E. D. Luckowski, J. M. Delucca, J. R. Williams, S. E. Mohney, M. J. Bozack, T. Isaacs-Smith, and J. Crofton, J. Electronic Material **27**, 4 (1998).

21) M. Lahrèche, M. Leroux, M. Laügt, M. Vaille, B. Beaumont, and P. Gibart, J. Appl. Phys **87**, 577 (2000).

4. Direct Growth of GaN on a- and m-plane SiC Substrates and Application in GaN/SiC Schottkey Diodes

4.1 Introduction

Ⅲ-Nitride semiconductors have made remarkable contributions to the commercial fabrication of LEDs[1-2], LDs[3], and HEMTs[4-5]. Epitaxial growth along nonpolar directions is free of internal electrical fields. Thus, nonpolar GaN-based optical devices are expected to realize higher internal quantum efficiency compared to polar devices with shorter radiative lifetimes.[6] At the same time, although the nonpolar GaN-based power devices cannot have polarization-generated channel charge ($> 1\times10^{13}$ cm^{-2}), it will allow the doping level to be independent of the polarization and the strain-related effect[7], which is the approach used in GaAs- and InP-based devices.[8] Nonpolar GaN is also expected to overcome the limitation of p-type magnesium doping level problems.[9] Nonpolar GaN epitaxial growth has been reported on nonpolar bulk GaN[10], r-plane Al_2O_3[11], and nonpolar SiC substrates[12-13]. Nonpolar bulk GaN substrates are still expensive and limited by their small sizes. Research on nonpolar GaN hetroepitaxy became important in making affordable, nonpolar GaN-based devices for commercial use.

Both GaN and SiC are wide-bandgap semiconductors. John et al. reported that GaN/SiC heterojunction bipolar transistors (HBTs) can be operated at 300°C[14], attracting attention to devices that use both GaN and SiC. As a substrate, SiC offers not only the ability to realize high breakdown voltage performance at high operation

temperature, but also high thermal conductivity (4.9 W/cm•K). GaN growth on nonpolar SiC substrates has only been reported via a buffer layer with a thickness around 100 nm.[12-13] In this chapter, we first report direct GaN growth on nonpolar substrates. Using conductive 4H-SiC substrates, nonpolar GaN/SiC direct epitaxial growth is expected to help realize vertical nonpolar devices in the future. On the other hand, nonpolar direct growth is also important to understand GaN growth on the walls (a-plane or m-plane) of c-plane SiC trench structures.

In the previous chapter, the direct growth of GaN on c-plane SiC substrates was realized by using a preflow TMAl treatment, and low vertical resistance was confirmed. Future work will focus on improving the crystal quality of the GaN epilayer and releasing the strain from the SiC substrate. On approach is to grow GaN on c-plane SiC trench structures. To prepare for this future approach, the direct growth of GaN on nonpolar SiC was realized, and the details are explained in Section 4.2. This represents the first report of the direct growth of GaN on a nonpolar SiC substrate.

4.2 Direct GaN Growth on a- and m-plane SiC

Experiments were performed using a horizontal MOVPE system. TMGa and NH_3 were used as precursors for gallium and nitrogen, respectively. The a-plane (11-20) and m-plane (1-100) of bulk 4H-SiC were used as substrates. Before loading the substrate into the growth chamber, the substrate was cleaned in acetone, methanol, and DI water for 5 min each, and the organic material was removed using an ultrasonic cleaner followed by cleaning with aqua regia solution ($HCl:HNO_3$ = 3:1). Finally, the substrates were placed into 5% HF to remove the native oxide layer and dried with N_2 gas. Previously, we reported the direct growth of GaN on the c-plane (0001) of an SiC

substrate. After increasing the GaN growth temperature, the substrate was thermally cleaned in H_2 gas environment for 3 min. We then began flowing TMAl without NH_3 before the growth step to prevent the reaction between the source gas and the SiC substrate. The a-plane and m-plane bulk SiC substrates were used for GaN epitaxial growth. The optimized conditions for the direct growth of GaN on the c-plane were used initially (see Section 3.4).

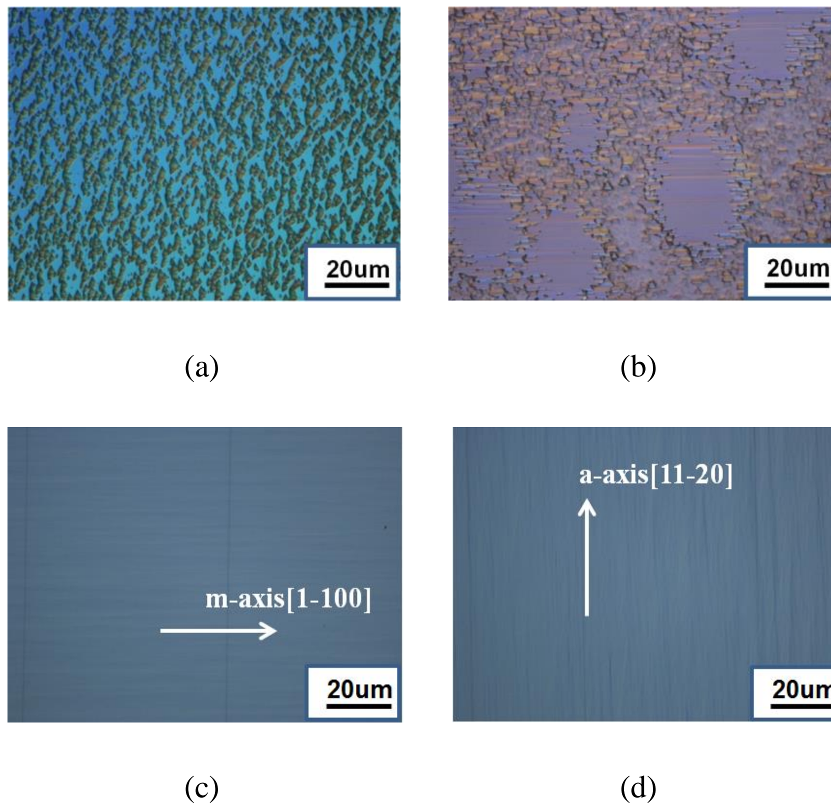
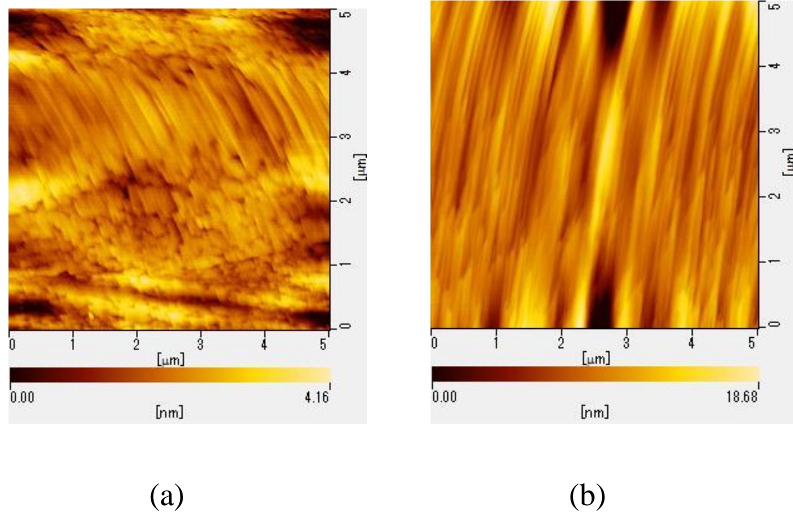


Fig. 4.1. OM images of non-polar GaN/SiC: (a) a-plane and (b) m-plane GaN/SiC formed under the conditions optimized for c-GaN/SiC; and (c) a-plane and (d) m-plane GaN/SiC formed under low pressure and low Ga/N ratio.

First, The conditions optimized for the direct growth of GaN on the c-plane were used. OM birds-eye-view images of the a-plane GaN/a-plane SiC and m-plane

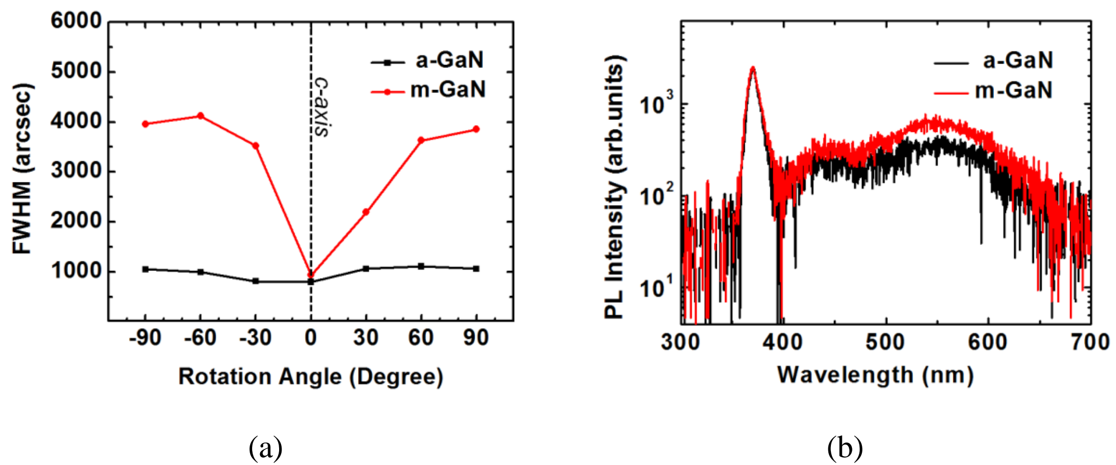
GaN/m-plane SiC are shown in Figs. 4.1(a) and 4.1(b), respectively. Figure 4.1(a) shows triangular GaN islands distributed on the surface of the a-plane SiC substrate, while GaN islands were observed on only some parts of the m-plane SiC substrate in Fig. 4.1(b). These results can be attributed to the different growth rates between the c-plane direction and the a- and m-plane directions. A low Ⅴ/Ⅲ ratio was reported to enhance the growth rate of the c- and m-planes. Another group also reported that a low reactor pressure (76 Torr) and a low N/Ga supply ratio increased the growth rate of the a- and m-planes. Thus, we changed the growth conditions by using a Ⅴ/Ⅲ ratio of 250 under a reactor pressure of 60 Torr. The TMGa flow rate was 87 μmol/min. The corresponding surface images are shown in Figs. 4.1(c) and (d). Both a-plane GaN on a-plane SiC and m-plane GaN on m-SiC formed mirror-flat GaN epitaxial films under these growth conditions. Based on the SEM cross-sectional images, the growth rate for a-plane GaN on a-SiC was determined to be 4.26 μm/h, while that for the m-plane on m-SiC was 3.36 μm/h. Figure 4.1(c) shows a flat surface. Crack was found to in a period of around 60 μm, which was thought to be caused by the lattice mismatch and thermal mismatch between GaN and SiC. Figure 4.1(d) indicates a high density of striation along the in-plane a-axis [11-20]; a similar surface image was obtained when m-GaN was grown on m-SiC via an AlN buffer layer.



(a) (b)

Fig. 4.2. AFM images of (a) a-plane and (b) m-plane GaN/SiC.

AFM was used to visualize the morphologies of 5 × 5 μm^2 areas of the samples (Fig. 4.2). In Fig. 4.2(a), the different morphology of a-GaN in the area along the m-axis can be attributed to stack faults; a flat surface was achieved with an RMS of 0.62 nm. m-GaN [Fig. 4.2(b)] exhibited a rougher surface morphology compared to a-GaN [Fig. 4.2(a)], which was attributed to the large density of striations along the a-axis. The RMS value of m-GaN was 2.64 nm.

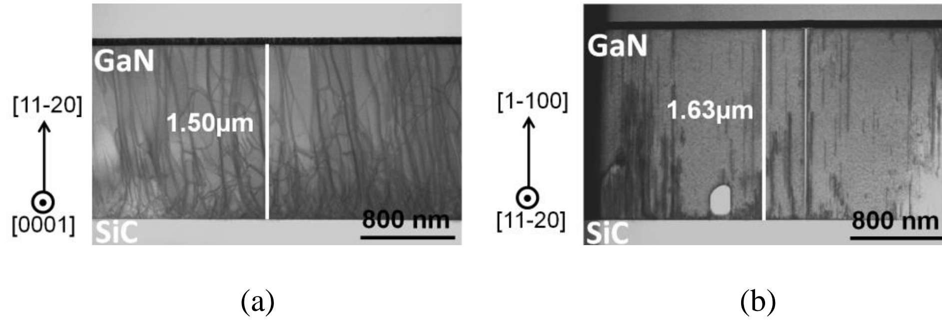


(a) (b)

Fig. 4.3. (a) Dependence of the FWHM on azimuth angle determined by XRD and (b)

PL spectra of GaN grown directly on non-polar SiC substrates.

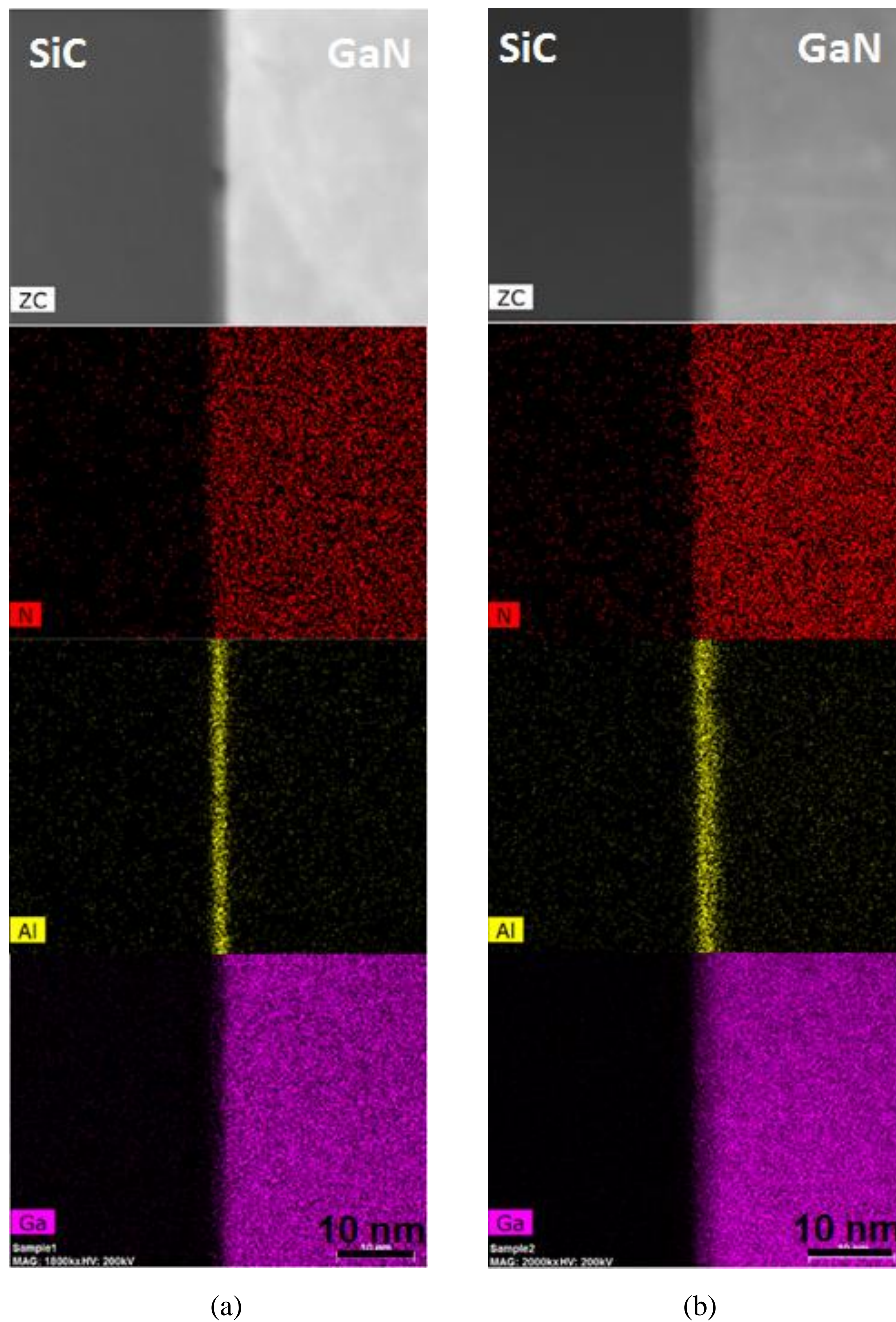
The crystalline qualities of the samples were determined by XRC in ω-scan mode for the GaN (0002) plane with different X-ray injection directions. The in-plane anisotropy of the FWHM of the (22-40) plane for a-plane GaN and the (2-200) plane for m-plane GaN is plotted for the Φ-scan of each specimen in Fig. 4.3(a). Under the experimental conditions, a-plane GaN showed better crystalline quality than m-plane GaN. The FWHM values ranged between 796 and 1107 arcsec for a-plane GaN and from 938 to 4120 arcsec for m-plane GaN. The optical properties of the samples were characterized by RT PL spectroscopy. The luminescence profile is shown in Fig. 4.3(b); both a-plane and m-plane GaN exhibited an ultraviolet near-band emission peak at 3.346 eV. The FWHM of a-plane GaN was calculated to be 108 meV, and the FWHM of m-plane GaN was calculated to be 111 meV. The broader near-band-edge emission of m-plane GaN was attributed to its larger defect density, which was in agreement with the XRC results. BL at around 2.82 eV and broad YL at around 2.28 eV were also observed in the RT PL spectra. The enhanced BL was attributed to the absorption of carbon impurities when low reactor pressure was used. The broad YL was attributed to the point defect V_{Ga} under Ga-rich conditions. The m-plane GaN spectrum exhibited higher BL and YL intensities than the a-plane spectrum, which was attributed to the higher impurity absorption efficiency of a-plane GaN compared to m-plane GaN.



(a) (b)

Fig. 4.4. Cross-sectional TEM images of (a) a-plane GaN on a-plane SiC and (b) m-GaN on m-plane SiC.

The GaN/SiC interfaces were observed using bright-field TEM cross-sectional images (Fig. 4.4). In the case of a-plane GaN growth on a-plane SiC, a high density of dislocations was generated on the a-GaN/a-SiC surface. The high density of dislocations was attributed to lattice mismatch and thermal efficiency mismatch. The high dislocation region near the a-GaN/a-SiC interface was estimated to be around 500 nm. Compared to the a-plane GaN/a-plane SiC sample, a low dislocation density was found on the m-plane GaN/m-plane SiC interface. Before the GaN growth step, the sample was treated with Al to prevent the reaction between the source gas and the SiC substrate. We used HREDS to analyze the GaN/SiC interface; the results are shown in Fig. 4.5. The left side of Fig. 4.5 represents the SiC substrate. The HREDS mapping shows that the aluminum atoms were located to the left of the GaN/SiC interface. By comparing the aluminum map with the nitrogen and gallium maps, the left aluminum atoms were considered to have formed an AlN layer (1.7 nm) at the a-GaN/a-SiC interface. In contrast, at the m-GaN/m-SiC interface, the aluminum atoms were considered to have formed an AlGaN layer (2.3 nm). As for EDS mapping consider the layer to be formed in the interface, noise signal came if only partly left AlN interlayer. These interfaces will be analyzed further in a future study.



(a) (b)

Fig. 4.5 HREDS cross-sectional element maps of (a) a-GaN and (b) m-GaN at the GaN/SiC interface.

In summary, by using a low pressure and low Ⅴ/Ⅲ ratio to enhance the lateral growth speed of non-polar GaN, the direct growth of a-plane GaN or m-plane GaN was realized on a-plane SiC or m-plane SiC substrates, respectively. Mirror-flat

surfaces were confirmed by OM and AFM. The RMS value of a-plane GaN was 0.62 nm, while that of the m-plane GaN was 2.64 nm. The crystalline qualities of the samples were characterized by XRC. The FHWM value of the directly grown a-plane GaN changed by around 40% by changing the X-ray injective direction, while that of the m-plane GaN changed by around 370%. The directly grown interfaces were confirmed by HREDS mapping. The thicknesses of the interlayers generated by TMAl-treatment were estimated; the AlN interlayer thickness in a-GaN/a-SiC was estimated to be 1.7 nm, while the AlGaN interlayer thickness in m-GaN/m-SiC was estimated to be 2.3 nm. The non-polar direct growth technique is expected to help us understand the growth process when the sidewalls of trench SiC structures are used for the direct growth of GaN/SiC. We also hope that this new technique will contribute to future non-polar vertical optical or power devices.

4.3 GaN/SiC and GaN/GaN Vertical Schottkey Barrier Diodes

To test the performances of devices containing GaN directly grown on SiC with TMAl treatment, c-plane GaN/SiC and GaN/AlN/SiC vertical SBDs were fabricated by the deposition of Al on the backsides of SiC substrates using an EB evaporation system to form Ohmic contacts on the backsides of the SiC substrates. Ni/Au contacts were then deposited on the GaN epilayer using EB and annealed at 525°C in oxygen for 5 min, forming a Schottky contact. GaN/GaN homo-epitaxial vertical SBDs were fabricated by the deposition of a Ti/Al/Ti/Au Ohmic contact on the backside of the GaN substrate followed by annealing at 650°C in N_2 for 5 min. Ni/Au contacts (Schottky contacts) were then deposited on GaN and annealed at 525°C in O_2 for 5 min.

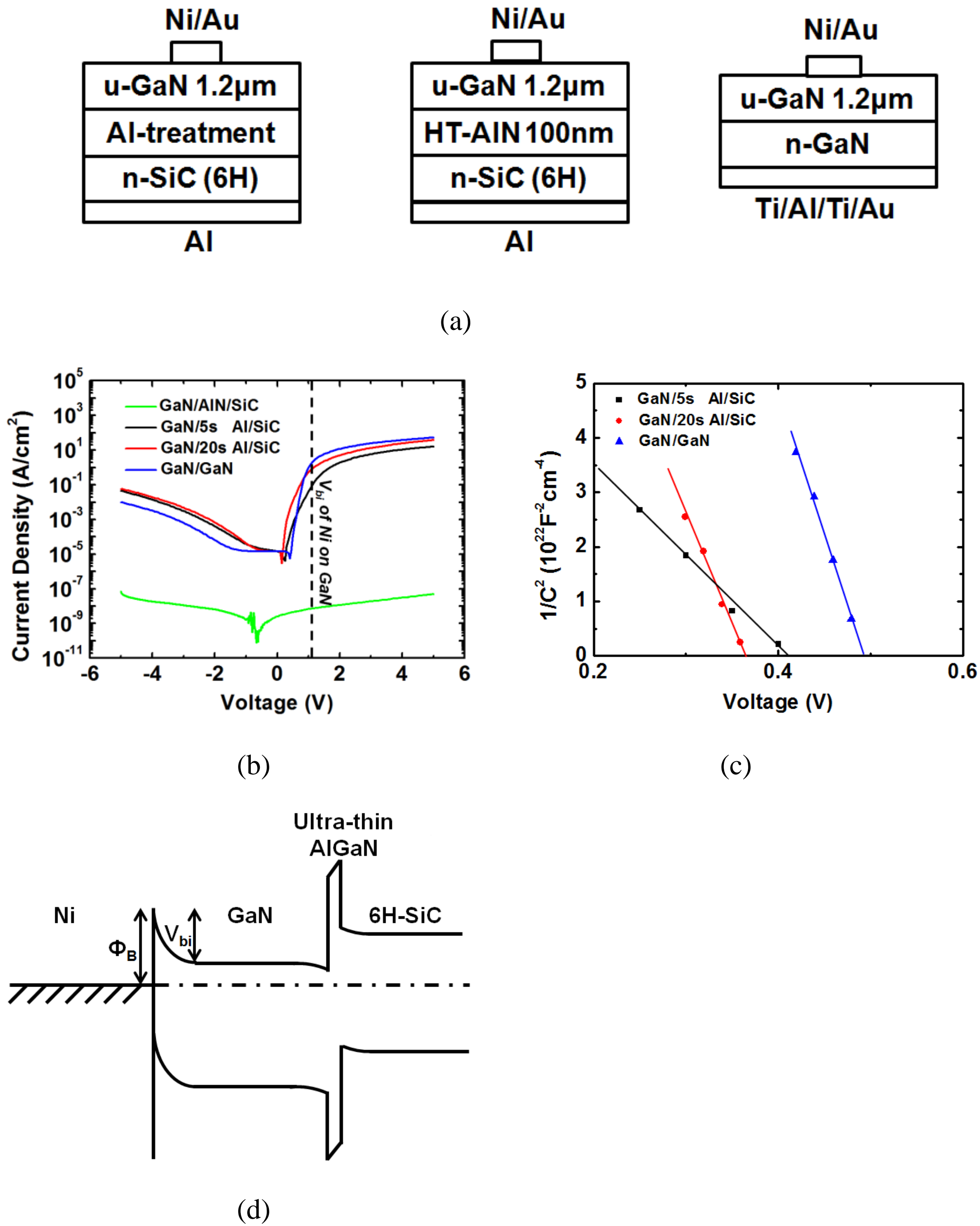


Fig. 4.6. (a) Structures of the fabricated devices; (b) room-temperature I-V and (c) C-V curves of the fabricated SBDs; and (d) band graph of the GaN/SiC Ni SBD.

To evaluate the effect of the ultrathin interlayers on the performances of the vertical devices performance, GaN/SiC, GaN/AlN/SiC, and GaN/GaN SBDs were fabricated

using 200-μm-diameter Schottky contacts on GaN epilayer surfaces. The structures of these SBDs are shown in Fig. 4.6(a). The SiC and GaN substrates are both n-type bulk substrates with carrier densities of 2.1×10^{18} and 2.9×10^{18} cm^{-3} and resistivities of 3.4×10^{-2} and 1.0×10^{-2} Ω•cm, respectively. The samples were characterized by current-voltage (I-V) and capacitance-voltage (C-V) measurements. Each SBD was measured with 10-20 samples, and the typical I-V and C-V curves are shown in Figs. 4.6(b) and 4.6(c), respectively. The black lines in Fig. 4.6 correspond to the SBD fabricated with GaN grown on SiC via a 100-nm-thick HT-AlN interlayer. Compared to the SBD with a high-resistance AlN interlayer, the series resistance of the SBD decreased from 4.0×10^{7} to 2.0×10^{-1} Ω•cm^2 for the sample treated with TMAl for 5 s and to 8.5×10^{-2} Ω•cm^2 for the sample treated with TMAl for 20 s. The difference in series resistivity between the samples treated by TMAl for 5 and 20 s could not be explained and will be explored further in future work. The higher resistance of the GaN/SiC sample compared to the GaN/GaN sample should be attributed to the ultrathin interlayer or the band offset of GaN/SiC for which the band graph is shown in Fig. 4.6(d). By optimizing the TMAl treatment time, a forward performance nearly the same as that of the GaN/GaN structure was achieved. The Ni Schottky diode parameters were calculated and are shown in Table 4.1. The barrier heights (Φ_{B_IV} and Φ_{B_CV}) were determined by both I-V and C-V methods using Formulas (4.1) and (4.2), respectively:

$$\Phi_{B_IV} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_s}\right) \quad (4.1)$$

$$\Phi_{B_CV} = V_i + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) + \frac{kT}{q} \quad (4.2)$$

The large variation between the two methods makes it difficult to accurately determine the Schottky barrier height due to the large leakage current, which is caused by the leakage path originating from the substrate or device processing. It also made our

experimental barrier height value lower than the barrier height of 0.89–0.99 eV reported by J. Suda et al.[6)] Because our samples were subjected to the same device processing, we can still compare GaN/SiC with GaN/GaN to assess the effect of the ultrathin interlayer on the performances of the vertical devices. For the sample treated with TMAl for 5 s, a smaller built-in voltage and lower barrier height were observed compared to those of the GaN/GaN sample. When homo-epitaxial GaN was grown on the GaN bulk substrate, a GaN epilayer with the same quality as the free-standing GaN substrate was obtained. For GaN grown on an SiC bulk substrate, more dislocations were generated by the lattice and thermal mismatches between GaN and SiC. The increased number of dislocations might be due to the leakage path, which caused a large saturation current and decreased the experimental barrier height according to Formula (4.1). It also caused a small intercept voltage, which also decreased the experimental barrier height according to Formula (4.2). The XRC results indicated that the sample treated by TMAl for 20 s generated more dislocations, resulting in a smaller experimental barrier height. All in all, the ultrathin interlayer resulted in a significant decrease in the series resistance compared to the use of a 100-nm-thick AlN interlayer. Compared with the GaN/GaN SBD, the GaN/SiC SBDs showed smaller barrier heights as a result of more leakage paths formed by the increased number of dislocations within the hetero-epitaxial GaN layer on the SiC substrates.

Table 4.1. Parameters of the fabricated Ni SBDs determined by C-V and I-V measurements.

	V_{bi} [V]	N_D [cm^{-3}]	Φ_{b_CV} [V]	Φ_{b_IV} [V]	n	R_{series} [$\Omega \cdot cm^2$]
GaN/AlN/SiC						4.0×10^{7}
GaN/TMAl 5 s/SiC	0.44	6.6×10^{14}	0.52	0.36	1.01	2.0×10^{-1}
GaN/TMAl 20 s/SiC	0.39	2.7×10^{14}	0.45	0.36	1.07	8.5×10^{-2}
GaN/GaN	0.52	3.1×10^{14}	0.58	0.33	1.07	7.8×10^{-2}

4.4 Conclusions

By using a low pressure and low Ⅴ/Ⅲ ratio to enhance the lateral growth speed of non-polar GaN, the direct growth of a-plane GaN and m-plane GaN were realized on a-plane SiC and m-plane SiC substrates, respectively. Mirror-flat surfaces were confirmed by OM and AFM. The RMS value of the a-plane GaN was 0.62 nm, while that of the m-plane GaN was 2.64 nm. The crystalline qualities of the samples were characterized by XRC. The FHWM value of the directly grown a-plane GaN changed by around 40% by changing the X-ray injective direction, while that of the m-plane GaN changed by around 370%. The directly grown interfaces were confirmed by HREDS mapping. The thickness of the AlN interlayer in a-GaN/a-SiC was estimated to be 1.7 nm, and the thickness of the AlGaN interlayer in m-GaN/m-SiC was estimated to be 2.3 nm. The non-polar direct growth technique is expected to help us understand the growth process when the sidewalls of trench SiC structures are used for the direct growth of GaN/SiC. We also hope that this new technique will contribute to future non-polar vertical optical or power devices.

GaN/SiC SBDs were fabricated and compared with GaN/AlN/SiC and GaN/GaN structures to determine the effect of TMAl treatment on the performances of the vertical devices. The GaN/SiC structure exhibited a significant decrease in series resistance after the TMAl treatment compared to the GaN/AlN/SiC structure. The GaN/SiC samples had higher series resistances than the GaN/GaN sample, which was attributed to the ultrathin interlayer or the band offset of GaN/SiC. By optimizing the TMAl treatment time, we obtained nearly the same forward performance achieved by the GaN/GaN structure. We believe that the GaN/SiC samples obtained by TMAl

treatment will be competitive with other materials due to the higher thermal conductivity of the SiC substrate, allowing it to operate at a high power.

References

1） P. Waltereit, O. Brandt, A. Trampert, HT. Grahn, J. Menniger, M. Ramsteiner, M. Reiche, and KH. Ploog, Nature **406**, 865 (2000).

2） I. Akasaki, S. Sota, H. Sakai, T. Tanaka, M. Koike, and H. Amano, Electronics Letters **32**, 1105 (1996).

3） B. J. Zhang, T. Egawa, H. Ishikawa, Y. Liu, and T. Jimbo, Jpn. J. Appl. Phys. **42**, L226 (2003).

4） T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. Denbaars, J. S. Speck, and U. K. Mishra, IEEE Electron Device Lett. **26**, 11 (2005).

5） M. Micovic, A. Kerdoghlian, P. Hashimoto, M. Hu, M. Antcliffe, P. J. Willadsen, W. S. Wong, R. Bowen, I. Milosavljevic, A. Schmitz, M. Wetzel, and D. H. Chow, IEDM Tech. Dig. **425** (2006).

6） J. Suda, K. Ymaji, Y. Hayashi, T. Kimoto, K. Shimoyama, H. Namita, and S. Nagao, Appl. Phys. Express **3**, 101003 (2010).

5. Summary and Conclusions

To apply GaN to high-power devices, vertical structure devices are preferable. Ion implantation, which is the main technique used to fabricate vertical structure devices, was the first focus of this thesis. We proposed a pre-sputter technique with the goal of reducing the ion implantation damage. When an Mg ion concentration of 2×10^{17} cm^{-3} was used, p-type GaN was realized, as demonstrated PL spectroscopy and C-V analysis. The formation of p-type GaN using higher ion concentrations will be the focus of future work. As the second focus of this study, we studied the direct epitaxial growth of GaN on bulk SiC substrates. The mass production of SiC substrates could push GaN-based vertical power devices into production, and the good thermal conductivity of the SiC substrate could allow the fabrication of GaN-based high-power devices in the future. The conclusions of each chapter are summarized below.

1. Preface

The contributions that GaN makes to peoples' everyday lives were introduced, and the merits and main issues of GaN-based lateral structure power devices were explained. We then introduced how our research could contribute to future vertical structure power devices. Finally, we summarized the structure of this thesis.

2. Magnesium Ion Implantation in GaN with a Pre-sputter Technique

In this chapter, we introduced the background of magnesium-ion implantation and proposed a pre-sputter technique to reduce the implantation damage. Experiments were carried out to assess the effect of our new technique. A p-type GaN layer was realized when the Mg implantation concentration was 10^{17} cm^{-3}, as demonstrated by C-V measurements. The implantation damage in samples implanted with higher Mg

concentrations could be recovered by post-annealing; however, the optical and electrical properties could not be recovered. Both the simulated and experimental results demonstrated that the pre-sputter technique reduced implantation damage.

3. Direct Growth of GaN on c-plane SiC Substrates

In this chapter, we reported original research in which TMAl treatment was applied to the direct growth of GaN on SiC bulk substrates. The as-grown samples were characterized, and we used XRD and PL spectroscopy to understand why our samples were cracked. We also confirmed the formation of an AlGaN ultrathin interlayer at the GaN/SiC interface.

4. Direct Growth of GaN on a- and m-plane SiC Substrates and Application in GaN/SiC Schottkey Diodes

In this chapter, GaN was grown directly on a-plane and m-plane SiC substrates. The as-grown samples were characterized to obtain information on the growth mobility on the walls of trench c-plane SiC bulk substrates. The directly grown GaN/SiC structures were also used to fabricate SBDs, which were then compared with GaN/AlN/SiC and GaN/GaN structures. The ultrathin interlayer formed as a result of the TMAl treatment generated a dramatic reduction in vertical series resistance compared to the use of a thick AlN interlayer.

Much work remains to be done. We need to find ways to realize p-type GaN using high Mg implantation concentrations. In addition, the formation of thick p-type GaN layers with high hole concentrations by ion implantation is necessary for vertical power device applications.

Although the direct growth of GaN on SiC was realized, vertical structure power transistors still need to be fabricated. Furthermore, the growth and device fabrication

process need to be optimized to generate SBDs with high breakdown voltages and high current performances.

Finally, I hope that the work described in this thesis will contribute to future GaN-based hybrid high-power and high-frequency devices.

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Research Achievements

Ⅰ. Publications

[1] “P–GaN by Mg Ion Implantation for Power Device Applications”, Zheng Sun, Marc Olsson, Tsutomu Nagayama, Yoshio Honda, and Hiroshi Amano, IEICE Technical Report **109**, SDM2014-38 (2014).

[2] “GaN/SiC Epitaxy Growth for High Frequency and High Power Device Applications”, Zheng Sun, Shigeyoshi Usami, Zheng Ye, Takahiro Ishii, Di Lu, Marc Olsson, Kouhei Yamashita, Yoshio Honda, and Hiroshi Amano, MRSF14-1736-T05-12.R1 (2014).

[3] “The Interface Analysis of GaN Grown on 0° off 6H-SiC with an Ultrathin Buffer Layer”, Zheng Sun, Akio Ohta, Seiichi Miyazaki, Kentaro Nagamatsu, Hojun Lee, Marc Olsson, Zheng Ye, Manato Deki, Yoshio Honda, and Hiroshi Amano, Japanese Journal of Applied Physics **55**， 010303 (2016).

[4] “Pre-Al Treatment Influence for GaN Growth on SiC with an Ultrathin Buffer Layer”, Zheng Sun, Shugo Nitta, Kentaro Nagamatsu, Marc Olsson, Peifeng Song, Manato Deki, Yoshio Honda, and Hiroshi Amano, Japanese Journal of Applied Physics, in press (2016).

Ⅱ. International Conferences

[1] "P – GaN by Mg Ion Implantation for Power Device Applications", Zheng Sun, Tsutomu Nagayama, Yoshio Honda, and Hiroshi Amano, International Symposium on Advanced Plasma Science and its Applications for Nitrides and Nanomaterials: 2014/3/2-6 (Oral).

[2] "GaN/SiC Epitaxy Growth for High Frequency and High Power Device Applications", Zheng Sun, Shigeyoshi Usami, Di Lu, Takahiro Ishii, Marc Olsson, Kouhei Yamashita, Yoshio Honda, and Hiroshi Amano, Materials Research Society 2014- Fall, 2014/11/30-2014/12/5(Poster).

[3] "Mg-ion-implantation Damage Influence on the Lattice Deformation of GaN", Zheng Sun, Marc Olsson, Zheng Ye, Tsutomu Nagayama, Tetsuya Wataneba, Yoshio Honda, and Hiroshi Amano, The 7th Asia-Pacific Workshop on Widegap Semiconductors, 2015/05/17-20 (Poster).

[4] "Reduction of Residual Carbon on Un-doped GaN Grown using Metal Organic Hydrogen Chloride Vapor Phase Epitaxy", Zheng Ye, Zheng Sun, Kentaro Nagamatsu, Manato Deki, Yoshio Honda, and Hiroshi Amano, The 6th International Symposium on Growth of III-Nitrides, 2015/11/8-13 (Poster).

[5] "Pre-Al Treatment Influence for GaN Growth on SiC with an Ultrathin Buffer Layer", Zheng Sun, Peifeng Song, Zheng Ye, Marc Olsson, Manato Deki, Yoshio Honda, and Hiroshi Amano, The 6th International Symposium on Growth of III-Nitrides, 2015/11/8-13 (Poster).

Ⅲ. Domestic Conferences

[1] “C2H2 を用いたカーボンドープ GaN の結晶成長とその評価”, Zheng Sun, Takayuki Sugiyama, Yoshio Honda, Masahito Yamaguchi, and Hiroshi Amano, 応用物理学会東海支部 第 19 回基礎セミナーポスターセッション, 2012/9/3 (Poster).

[2] “Pre-sputter Technology for GaN Acceptor Doping by Mg-ion Implantation”, Zheng Sun, Tsutomu Nagayama, Yoshio Honda, and Hiroshi Amano, 第 61 回応用物理学会春季学術講演会,2014 /3/17-20(Oral).

[3] “P – GaN by Mg Ion Implantation for Power Device Applications”, Zheng Sun, Marc Olsso, Tsutomu Nagayama, Yoshio Honda, and Hiroshi Amano, 電子情報通信学会, 2014/5/29 (Oral).

[4] “Detail Study on Lattice Deformation and Recovery of GaN by Mg-ion-implantation and the Subsequent Thermal Annealing”, Zheng Sun, Takayuki Sugiyama, Yoshio Honda, Masahito Yamaguchi, and Hiroshi Amano, 第 75 回応用物理学会秋季学術講演会, 2014/9/17-20 (Poster).