Influence of precursor gas on SiGe epitaxial material quality in terms of structural and electrical defects

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We have investigated the structural and electrical properties of n-type doped $Si_{1-x}Ge_x$ epitaxial layers (x=24−26%) grown by chemical vapor deposition with conventional [SiH_2Cl_2 (DCS)/GeH_4] and high-order (Si_2H_6/Ge_2H_6) precursor combinations. X-ray diffraction, atomic force microscopy, and deep-level transient spectroscopy (DLTS) measurements were performed for characterization. The crystalline properties and surface morphology of the $Si_{1-x}Ge_x$ layer with Si_2H_6/Ge_2H_6 grown at temperatures as low as 550 °C show good structural quality similar to that with DCS/GeH_4 grown at 615 °C. On the other hand, in terms of electrical properties, the DLTS measurement reveals the existence of vacancy-related complexes in the as-grown layer with Si_2H_6/Ge_2H_6. We found that post-deposition annealing at 200 °C for the $Si_{1-x}Ge_x$ epitaxial layer is effective for annihilating vacancy-related defects with densities down to as low as that of conventional precursors.

1. Introduction

With the downscaling of complementary metal-oxide-semiconductor (CMOS) devices beyond the 10 nm technology node, it is required to reduce thermal budgets during epitaxial growth for fabricating group-IV-based electronic devices. Silicon germanium ($Si_{1-x}Ge_x$) alloy has been attracting attention not only as a channel material for pMOSFETs[1-3] because of its high hole mobility, but also as a source/drain (S/D) stressor for applying a local uniaxial strain to Si and Ge for pMOSFETs[4-6] and nMOSFETs[7-8], respectively, to improve their carrier mobility.

For strained channel FETs with $Si_{1-x}Ge_x$ S/D stressors, the growth temperature of $Si_{1-x}Ge_x$ should be reduced to avoid undesired strain relaxation and unintentional out-diffusion of the dopant in $Si_{1-x}Ge_x$ during epitaxial growth. Considering the fabrication of nanoscale strained Ge channel FinFETs with $Si_{1-x}Ge_x$ stressors, the growth temperature should be reduced below 600 °C to realize well-defined nanoscale structures by suppressing the surface reflow of Ge in a narrow trench.[9]

On the other hand, Knights *et al.*[10] reported positron annihilation spectroscopy (PAS) results, which indicate that the concentration of vacancy-related defects in $Si/Si_{0.64}Ge_{0.36}/Si$ heterostructures increases with decreasing growth temperature in molecular beam epitaxy (MBE). There is a concern that point defects in an epitaxial layer seriously affect the device performance. For example, the presence of defects in the channel region might lead to a reduced carrier mobility owing to the fact that such defects act as additional scattering centers. Deep-level traps also cause the issues of gate controllability at the high-*k*/channel interface. For the S/D region, the deactivation of the impurity dopant and the enhancement of junction leakage between the S/D and the channel would be possible risks.

Additionally, in view of the integration of optical devices with CMOS circuits, it is also needed to deposit a $Si_{1-x}Ge_x$[11] or Ge[12-14] layer at low thermal budgets in order not to affect the underlying MOS devices. However, grown-in point defects possibly play a role as nonradiative recombination centers, leading to the degradation of optical performance.

To achieve a lower growth temperature of $Si_{1-x}Ge_x$ formation, the introduction of high-order precursor gases is proposed in some reports.[15-18] High-order silanes and germanes enable us to decrease the growth temperature owing to the low thermal energy necessary for breaking Si-Si or Ge-Ge bonds in the molecules.[17-18] The characteristics of $Si_{1-x}Ge_x$ film growth with high-order precursors have already been well studied by chemical vapor deposition (CVD)[15-16, 18-21] and gas source MBE[22]. In a recent study[15], a low-temperature $Si_{1-x}Ge_x$ growth down to 400 °C has been achieved using high-order

precursors.

However, the effects of lowering growth temperature on electronic properties related to defects have not been understood in detail yet. Understanding and controlling the crystalline and electrical properties of grown-in defects introduced during the CVD growth of $Si_{1-x}Ge_x$ are important for establishing an appreciable low thermal budget process.

Thus, in this study, we investigate the effect of reducing the growth temperature using high-order precursor gases on the crystalline quality of $Si_{1-x}Ge_x$ epitaxial layers in terms of structural and electrical defects. The impact of post-deposition annealing on the grown-in defect density is also investigated.

2. Experimental procedure

All *in situ* arsenic (As)-doped $Si_{1-x}Ge_x$ layers were grown on n-Si(001) substrates using a reduced-pressure chemical vapor deposition (RP-CVD) module, which is integrated into an ASM Intrepid^{TM} XP 300 mm epitaxial deposition system.[23)] Dichlorosilane (SiH_2Cl_2, DCS), disilane (Si_2H_6), germane (GeH_4), digermane (Ge_2H_6), and arsine (AsH_3) were used as precursor gases for Si, Ge, and the n-type As-doping source, respectively. H_2 was used as a carrier gas. The nominal Ge content was 25%. The thickness of all $Si_{1-x}Ge_x$ layers was 180 nm, which is below the critical thickness for strain relaxation.[24)] The growth temperature and growth rate of $Si_{1-x}Ge_x$ layers were 615 and 550 °C, and 6.3 and 38.2 nm/min for precursor combinations of DCS/GeH_4 and Si_2H_6/Ge_2H_6, respectively. The details of $Si_{1-x}Ge_x$ epitaxial growth using high-order precursors were reported in Ref. 15. The average carrier concentration in As-doped $Si_{1-x}Ge_x$ layers was estimated to range from 6×10^{17} cm^{-3} to 8×10^{17} cm^{-3} by capacitance-voltage (*C*-*V*) measurement. For some samples, post-deposition annealing (PDA) was performed at 200 and 500 °C for 10 min in N_2 ambient.

To measure *C*-*V* and DLTS characteristics, we prepared metal/n-$Si_{1-x}Ge_x$ Schottky diode samples. After the growth of the $Si_{1-x}Ge_x$ layer, its surface was chemically cleaned with a diluted HF (HF:H_2O=1:100) solution to remove the native oxide, followed by the deposition of circular gold (Au) contacts by thermal evaporation in vacuum. Then, back-side Ohmic contacts were formed by indium gallium (InGa) eutectic and a piece of In foil.

The possible presence of defects was examined by deep-level transient spectroscopy (DLTS), which was performed using a Fourier transform digital system operating at a frequency of 1 MHz.[25-26)] The composition and the degree of strain relaxation of the

$Si_{1-x}Ge_x$ layers were measured by X-ray diffraction two-dimensional reciprocal space mapping (XRD-2DRSM using a Phillips X'Pert MRD Pro diffractometer). XRD ω-2θ and ω-rocking curve scans were also performed to investigate the crystalline properties of the $Si_{1-x}Ge_x$ layers prepared with each precursor combination. Atomic force microscopy (AFM) was performed to observe the surface morphology of the $Si_{1-x}Ge_x$ layers.

3. Results and discussion

3.1 Crystalline property and surface morphology of the $Si_{1-x}Ge_x$ epitaxial layers

In this section, we compare the crystalline qualities of as-grown $Si_{1-x}Ge_x$ layers prepared using two kinds of precursor combinations with DCS/GeH_4 and Si_2H_6/Ge_2H_6.

Figure 1 shows XRD-2DRSM results obtained around the Si 224 reciprocal lattice point for the $Si_{1-x}Ge_x$ epitaxial layer grown on a Si substrate with each DCS/GeH_4 and Si_2H_6/Ge_2H_6 precursor set. The diffraction intensity of the contour maps is presented on a logarithmic scale. The vertical and diagonal lines across the Si 224 reciprocal lattice point indicate the trajectory lines of pseudomorphic and fully strain-relaxed states, respectively, for $Si_{1-x}Ge_x$ layers with various contents. We can clearly observed the diffraction peak related to $Si_{1-x}Ge_x$ as shown in Fig. 1, which indicates the pseudomorphic growth of a $Si_{1-x}Ge_x$ epitaxial layer with respect to the underlying Si substrate in both precursor sets since the in-plane reciprocal lattice Q_x of the $Si_{1-x}Ge_x$ layer corresponds to that of the Si substrate. From the results of XRD-2DRSM, the Ge contents of the $Si_{1-x}Ge_x$ layers were estimated to be 24 and 26% for DCS/GeH_4 and Si_2H_6/Ge_2H_6 cases, respectively.

Figure 2(a) shows XRD ω-2θ profiles for two $Si_{1-x}Ge_x$/Si samples prepared with each precursor combination. The XRD profiles of both $Si_{1-x}Ge_x$/Si samples show the presence of well-defined thickness fringes, indicating the formation of an abrupt interface between the $Si_{1-x}Ge_x$ epitaxial layer and the Si substrate. It should be noted that the difference in $Si_{1-x}Ge_x$ diffraction peak position is caused only by the difference in Ge content, not by the strain relaxation of the $Si_{1-x}Ge_x$ layer. In addition, we also measured ω-rocking curves for both samples as shown in Fig. 2(b). This result shows that the full width at half maximum (FWHM) values of the $Si_{1-x}Ge_x$ 004 diffraction peaks are very similar, 0.0316° for the DCS/GeH_4 sample and 0.0314° for the Si_2H_6/Ge_2H_6 sample. The similar FWHM values mean that there is no obvious difference in the tilting angle of $Si_{1-x}Ge_x$ (004) lattice planes between the $Si_{1-x}Ge_x$ epitaxial layers.

Figure 3 shows AFM images and surface roughness profiles of $Si_{1-x}Ge_x$ layers grown with DCS/GeH_4 and Si_2H_6/Ge_2H_6 precursor combinations. The scanning area for all

images is 2×2 μm^2. These AFM images and surface profiles show atomically flat and uniform surfaces and do not show any surface imperfections such as stacking faults, dislocation lines, and 3-dimensional island growth for both sets of precursors. The root mean square (RMS) roughness of the $Si_{1-x}Ge_x$ layer prepared with Si_2H_6/Ge_2H_6 was estimated to be 0.11 nm, which is as small as that with DCS/GeH_4 (0.10 nm).

Considering these results of XRD and AFM measurements, despite the reduced temperature, a similar structural quality of the $Si_{1-x}Ge_x$ epitaxial layer is obtained in the sample prepared with Si_2H_6/Ge_2H_6 compared with DCS/GeH_4.

3.2 Electrical defect structure in the $Si_{1-x}Ge_x$ epitaxial layers

In this section, we report the electrically active defect structure of $Si_{1-x}Ge_x$ epitaxial layers characterized by deep-level transient Fourier spectroscopy (DLTFS) to compare the electrical properties between two samples prepared with DCS/GeH_4 and Si_2H_6/Ge_2H_6 precursor combinations.

For all $Si_{1-x}Ge_x$/Si samples, a sampling period (T_w) of 5.12 ms and a pulse width (T_p) of 1 ms were used at a bias pulse with a reverse bias (V_R) of −1 V and a filling bias (V_P) of 0 V. Here, assuming that the defect density (N_T) is lower than about 10% of the dopant concentration (N_D) in $Si_{1-x}Ge_x$ layers, we can estimate the N_T from the DLTS results as[27)]

$$N_T = \frac{2\Delta C}{C_R} N_D, \qquad (1)$$

where ΔC and C_R are the capacitance change upon filling the deep levels in the depletion region with electrons and the capacitance at V_R, respectively.

Figures 4(a) and 4(b) show the defect density in the $Si_{1-x}Ge_x$ layers extracted from the DLTS signals as a function of the measurement temperature for the $Si_{0.76}Ge_{0.24}$/Si sample prepared with DCS/GeH_4 and the $Si_{0.74}Ge_{0.26}$/Si sample with Si_2H_6/Ge_2H_6, respectively. The depletion layer widths at the bias pulse (V_P=0 V, V_R=−1 V) were estimated from *C*-*V* characteristics to be 60−80 nm and 55−70 nm for samples with DCS/GeH_4 and Si_2H_6/Ge_2H_6, respectively. Those values are smaller than the thickness of the $Si_{1-x}Ge_x$ layers. In other words, the probed depth in these DLTS results is almost in the same region within both $Si_{1-x}Ge_x$ layers. No DLTS peak is observed for the DCS/GeH_4 sample as shown in Fig. 4(a). In contrast, 2 positive peaks are clearly observed at around 180 and 250 K (labeled E1 and E2, respectively) for the Si_2H_6/Ge_2H_6 sample as shown in Fig. 4(b). In DLTS measurement, a positive peak generally corresponds to a signal associated with an electron trap in the n-type epitaxial layer.

To estimate the energy level of a defect from DLTS measurements, the following

equation was used[27]:

$$\tau = \frac{1}{\sigma_n v_n N_c} \exp\left(\frac{E_t}{kT}\right), \qquad (2)$$

where τ, E_t, k, T, σ_n, v_n, and N_c are the time constant expressed as the inverse of an electron emission rate, the energy level measured from the conduction band minimum, the Boltzmann constant, the measurement temperature, the capture cross section of a defect for electrons, the thermal velocity of electrons, and the effective density of states in the conduction band, respectively. Here, considering that v_n and N_c are proportional to $T^{\frac{1}{2}}$ and $T^{\frac{3}{2}}$, respectively, the slope in the plot of $\ln(\tau T^2)$ as a function of inverse T gives the activation energy of E_t.

Figure 5 shows Arrhenius plots of τT^2 values for E1 and E2 observed in Fig. 4(b). The activation energies and capture cross sections for E1 and E2 extracted from the slope and intercept of the Arrhenius plots were estimated to be E_c−0.33 eV and 9.7×10^{-18} cm^2, E_c−0.54 eV and 2.5×10^{-13} cm^2, respectively.

Figure 6 shows the summary of energy levels of observed defects in the as-grown $Si_{0.74}Ge_{0.26}$/Si sample prepared with the Si_2H_6/Ge_2H_6 precursor combination. Various point defect structures reported previously are also shown for reference.[28-31]

The energy levels of the observed peaks in this study are deeper than those typically found for interstitial-related defect complexes. Thus, it is considered that the observed defects in the as-grown $Si_{1-x}Ge_x$ epitaxial layer with Si_2H_6/Ge_2H_6 consist mainly of vacancy-related complexes. Considering that these defects are not observed in the $Si_{1-x}Ge_x$/Si sample prepared with the DCS/GeH_4 precursor combination, we considered that the defects are introduced during RP-CVD growth owing to the low growth temperature.

Next, we also investigated the impact of PDA on these deep-level traps in the $Si_{1-x}Ge_x$ layer prepared with the Si_2H_6/Ge_2H_6 precursor combination. Note that any change in Ge content and the strain relaxation of the $Si_{1-x}Ge_x$ layer were hardly observed by XRD measurements in the sample even after PDA up to 500 °C. Figure 7 shows the deep-level defect density extracted DLTS signals as a function of the measurement temperature for as-grown and 200 °C- and 500 °C-annealed $Si_{0.74}Ge_{0.26}$/Si samples. In the $Si_{1-x}Ge_x$/Si sample annealed at 200 °C, the defect density markedly decreased to a value less than the lower detection limit of about 1×10^{14} cm^{-3} under the DLTS measurement conditions in this study. No remarkable DLTS peaks were also observed for the 500 °C-annealed samples.

Here, we discuss the thermal annealing effects on the vacancy defects in the $Si_{1-x}Ge_x$/Si samples. According to the previous report[32], vacancy-related defects can be dissociated at

temperatures as low as 50 °C for Ge-V in the relaxed $Si_{0.95}Ge_{0.05}$/Si and 180 and 250 °C for E-centers (group-V impurity-vacancy pair) in n-type Si and relaxed-$Si_{0.75}Ge_{0.25}$, respectively. In addition, taking into account the vacancy diffusion coefficient in a Ge sample reported in Ref. 33, the diffusion length is estimated to be 140 nm for the PDA condition at 200 °C for 10 min. We suggest that markedly decreasing the defect density after PDA at temperatures as low as 200 °C can be interpreted in terms of the thermal dissociation of vacancy-related complexes and the vacancy diffusion in the $Si_{1-x}Ge_x$ layers during PDA. Even though as-grown $Si_{1-x}Ge_x$ epitaxial layers with Si_2H_6/Ge_2H_6 are electrically defective layers, these DLTS results indicate that the PDA process at 200 °C, which is far below the growth temperature, is effective for reducing the deep-level trap density in $Si_{1-x}Ge_x$ to that of DCS/GeH_4 at least less than about 1×10^{14} cm^{-3}.

4. Conclusions

We investigated the crystalline and electrical properties of n-type doped epitaxial $Si_{1-x}Ge_x$ layers (x=24−26%) grown by the RP-CVD method with each precursor combination of DCS/GeH_4 and Si_2H_6/Ge_2H_6. XRD and AFM results revealed that $Si_{1-x}Ge_x$ epitaxial growth using high-order silane and germane even at a low temperature of 550 °C enables us to obtain a similar structural quality, as well as the sample with conventional precursors at a higher temperature of 615 °C. In terms of electrical properties, even though we found that vacancy-related defects are present in the as-grown $Si_{1-x}Ge_x$ epitaxial layer prepared with Si_2H_6/Ge_2H_6 by DLTS measurement, PDA treatment at a low temperature of 200 °C effectively reduces the defect density to as low as that of DCS/GeH_4, which is below the DLTS detection limit of about 1×10^{14} cm^{-3}. The advantages of high-order precursors, which achieve both high throughput and low thermal budget, aid the epitaxial growth technology for future group-IV-based CMOS scaling.

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Figure Captions

Fig. 1. (Color online) XRD-2DRSM results around the Si reciprocal lattice point of $Si_{1-x}Ge_x$ epitaxial layers grown with (a) DCS/GeH_4 and (b) Si_2H_6/Ge_2H_6.

Fig. 2. (Color online) (a) XRD ω-2θ profiles and (b) XRD ω-rocking curves for $Si_{0.76}Ge_{0.24}$/Si (DCS/GeH_4) and $Si_{0.74}Ge_{0.26}$/Si (Si_2H_6/Ge_2H_6).

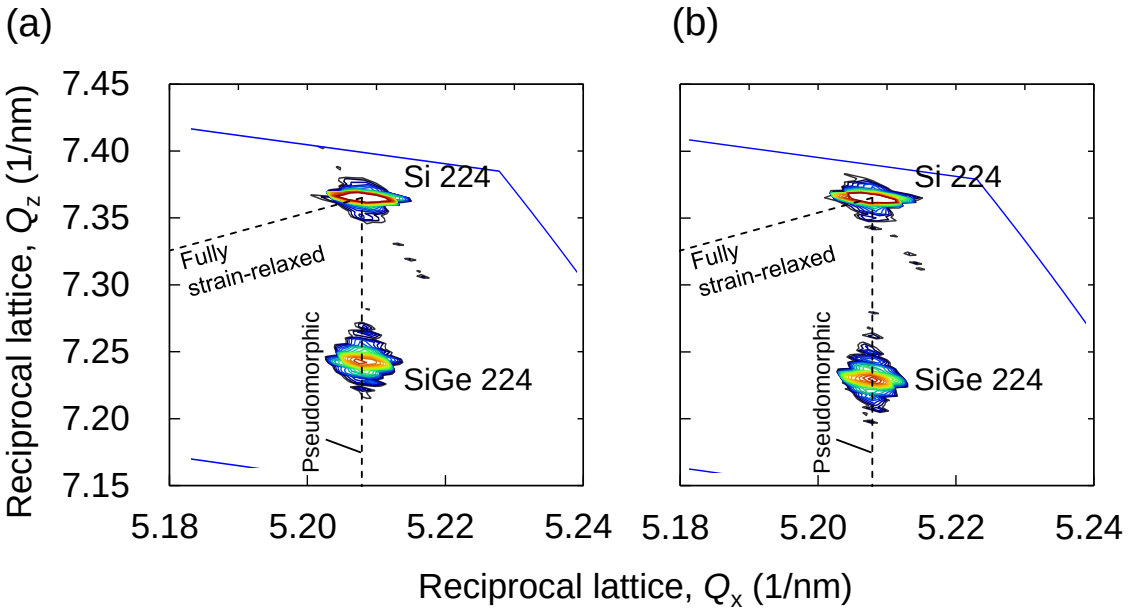
Fig. 3. (Color online) AFM images and surface roughness profiles of (a) $Si_{0.76}Ge_{0.24}$ (DCS/GeH_4) and (b) $Si_{0.74}Ge_{0.26}$ (Si_2H_6/Ge_2H_6).

Fig. 4. (Color online) Deep-level defect density extracted from the DLTS signals as a function of measurement temperature for (a) $Si_{0.76}Ge_{0.24}$ with DCS/GeH_4 and (b) $Si_{0.74}Ge_{0.26}$ with Si_2H_6/Ge_2H_6.

Fig. 5. (Color online) Arrhenius plots of τT^2 for the observed peaks in Fig. 4(b).

Fig. 6. (Color online) Energy levels of observed defects for as-grown $Si_{0.74}Ge_{0.26}$ layer with Si_2H_6/Ge_2H_6 and various point defect structures reported in literature.

Fig. 7. (Color online) Deep-level defect density extracted from the DLTS signals as a function of measurement temperature for as-grown and 200 °C- and 500 °C-annealed $Si_{0.74}Ge_{0.26}$ samples prepared with Si_2H_6/Ge_2H_6.



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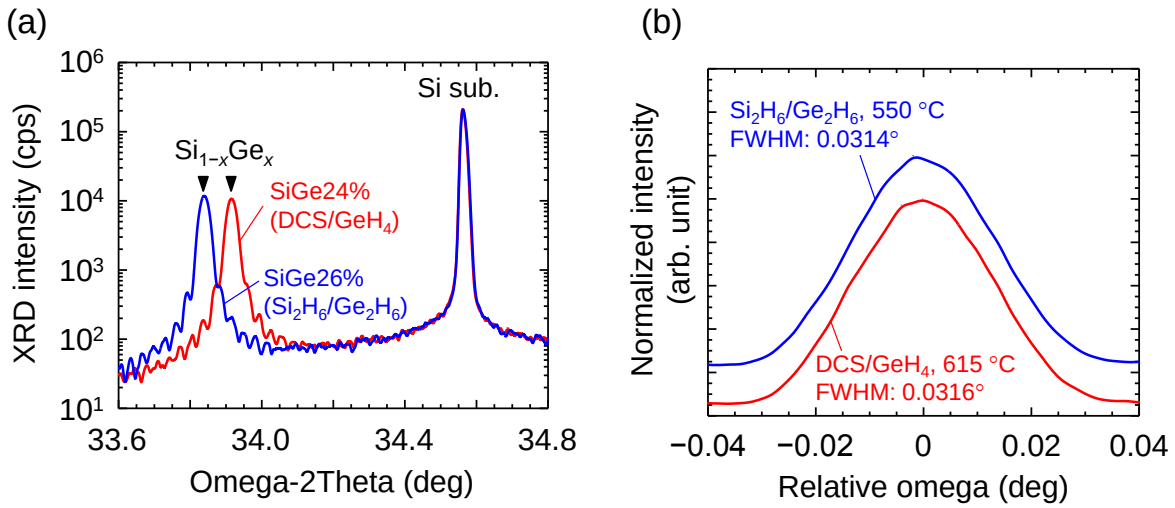

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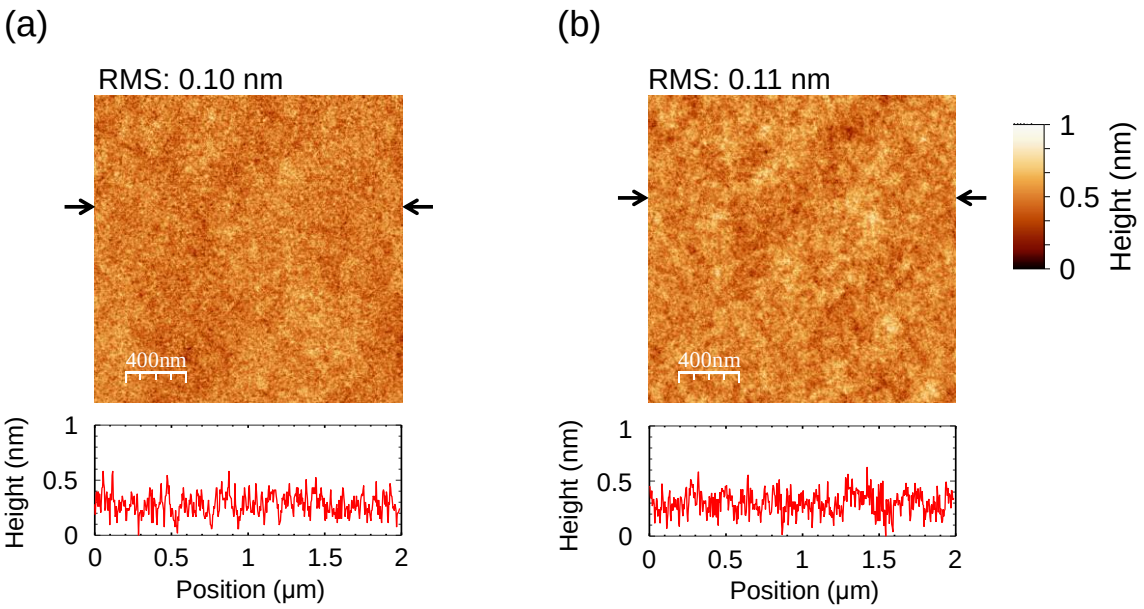

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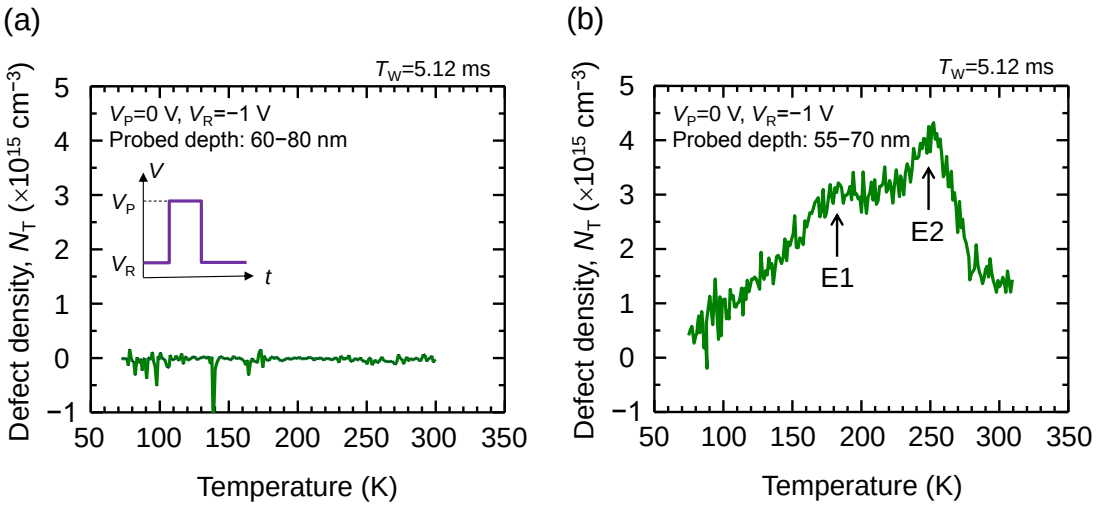

Fig. 4. (Color online) Deep-level defect density extracted from the DLTS signals as a function of measurement temperature for (a) $Si_{0.76}Ge_{0.24}$ with DCS/GeH_4 and (b) $Si_{0.74}Ge_{0.26}$ with Si_2H_6/Ge_2H_6.

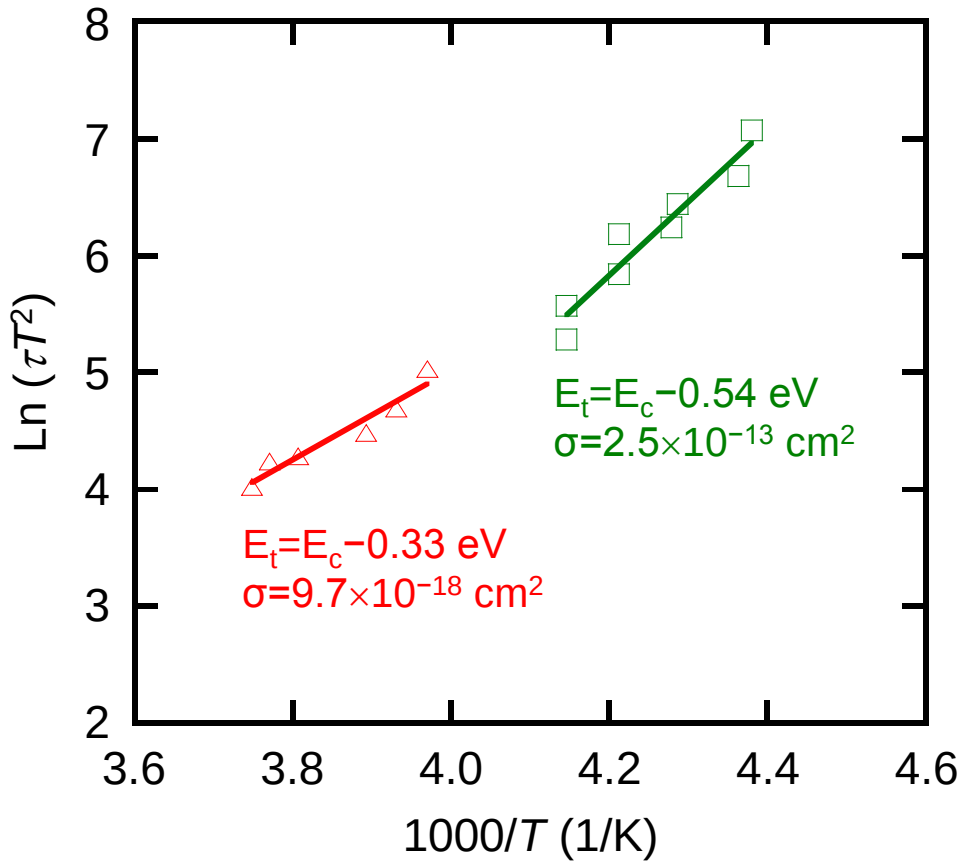

Fig. 5. (Color online) Arrhenius plots of τT^2 for the observed peaks in Fig. 4(b).

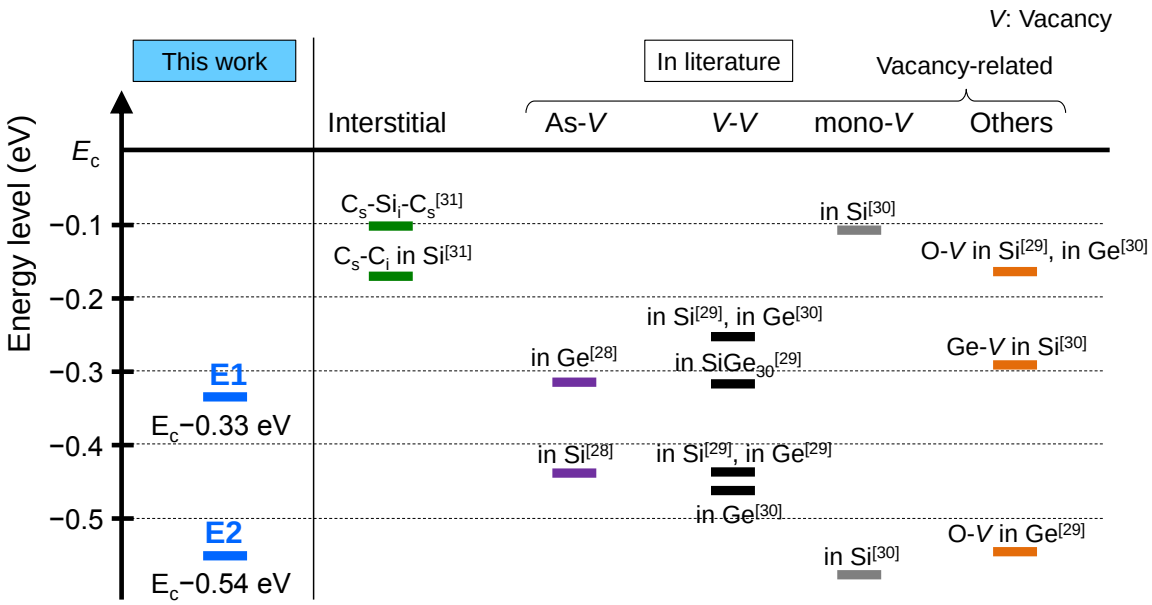

Fig. 6. (Color online) Energy levels of observed defects for as-grown $Si_{0.74}Ge_{0.26}$ layer with Si_2H_6/Ge_2H_6 and various point defect structures reported in literature.

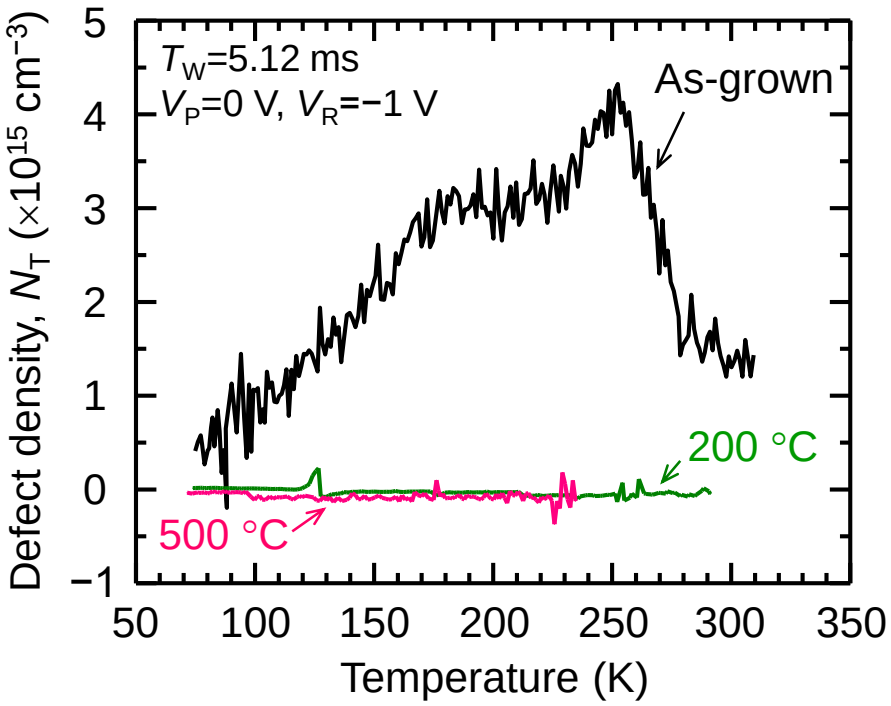

Fig. 7. (Color online) Deep-level defect density extracted from the DLTS signals as a function of measurement temperature for as-grown and 200 °C- and 500 °C-annealed $Si_{0.74}Ge_{0.26}$ samples prepared with Si_2H_6/Ge_2H_6.