Template for APEX (Jan. 2014)

Vertical GaN p-n diode with deeply etched mesa and capability of avalanche breakdown

Hayata Fukushima[1], Shigeyoshi Usami[1], Masaya Ogura[1], Yuto Ando[1], Atsushi Tanaka[2,5], Manato Deki[2], Maki Kushimoto[1], Shugo Nitta[2], Yoshio Honda[2], and Hiroshi Amano[2,3,4,5]

[1] *Graduate School of Engineering, Nagoya University, Nagoya 464-8603, Japan*

[2] *Institute of Materials and Systems for Sustainability, Nagoya University, Nagoya 464-8601, Japan*

[3] *Akasaki Research Center, Nagoya University, Nagoya 464-8603, Japan*

[4] *Venture Business Laboratory, Nagoya University, Nagoya 464-8603, Japan*

[5] *National Institute for Materials Science, Tsukuba 305-0044, Japan*

E-mail: h_fukusi@echo.nuee.nagoya-u.ac.jp

A simple structure with high breakdown voltage and low leakage current of a vertical GaN p-n diode on a GaN free-standing substrate is demonstrated. We describe a vertical p-n diode with a simple edge termination that has a drift layer etched deeply and vertically. A device simulation revealed that the electric field was more relaxed at the device edge and applied uniformly in the entire device with increasing etching depth. We fabricated the simulated structure and succeeded in reducing the leakage current and improving the breakdown voltage. With this structure, a stable avalanche breakdown can be observed.

GaN is a promising material for next-generation semiconductor power devices owing to its wide band gap, high breakdown electric field, and high electron mobility. As new power devices have started to replace silicon power devices, which have reached the physical limits of silicon, lateral devices using GaN, typified by high-electron-mobility transistors, have been researched and commercialized. However, GaN power devices such as these lateral devices are normally grown on foreign substrates including sapphire, Si, and SiC substrates, and thus the dislocation density can reach approximately 10^8 to 10^{10} cm^{-2} owing to lattice mismatch. Although GaN power devices should potentially have a higher breakdown voltage than SiC power devices, owing to their higher dislocation density, GaN power devices could not exceed the performance of SiC devices.[1-5] Recently, there has been significant progress in improving the quality of GaN free-standing substrates, and the dislocation density of commercially available GaN free-standing substrates is currently 10^4 to 10^7 cm^{-2}. As a result, research on vertical GaN power devices with high breakdown voltage is progressing dramatically.[6-11] However, GaN vertical power devices are still under development because of an unsatisfactory edge termination structure or a leakage current generation at dislocations.[12-15] The unsatisfactory termination structure causes not only the leakage current owing to electric field concentration but also destructive breakdown and early avalanche breakdown at the device edge. Because of this problem, the impact ionization coefficient essential for predicting the breakdown field of GaN is still unknown. To reveal this physical property, it is necessary to realize a power device with high breakdown voltage and the capability of relaxing the electric field at the device edge and stable avalanche breakdown.[16] To realize edge termination in GaN p-n diodes, a bevel mesa structure, a field plate structure, a guard ring structure, ion implantation, and other structures have been reported.[17-24] In this letter, we report vertical GaN p-n diodes with simple edge termination structure that can obtain a uniform electric field to the entire device and a large electric field relaxation simply by deep and vertical mesa etching, and their capability of stable avalanche breakdown.

Figure 1 (a) shows a schematic diagram of the p-n diode structure used for device simulation. A p-n diode comprising a 10 μm n-type GaN drift layer (N_d: 2×10^{16} cm^{-3}), a 500 nm p-type GaN layer (N_a: 2×10^{19} cm^{-3}), and a 30 nm p^+-GaN contact layer (N_a: 2×10^{20} cm^{-3}) on an n-type GaN free-standing substrate with a donor concentration of 2×10^{18} cm^{-3} and a deposited contact electrode was reproduced by a Silvaco ATLAS device simulator. Using this structure, the electric field distribution was simulated with the device simulator while varying the mesa depth. Figures. 1 (b)-(f) show the images of the electric field distribution

obtained by the simulation when a high reverse bias of -800 V was applied. The simulation shows that the electric field at the device edge becomes more relaxed and is applied more uniformly as the mesa is vertically etched to a greater depth. These results indicate that the dielectric breakdown at the device edge can be suppressed by etching the mesa to a greater depth than the depletion layer width at the designed breakdown voltage with a non-punch-through condition.

Figure 2 (a) shows a schematic diagram of the p-n diode structure that we fabricated. A p-n diode structure similar to that used in the simulation was epitaxially grown by metal-organic vapor phase epitaxy on an n-type GaN free-standing substrate. The GaN substrate was fabricated by hydride vapor phase epitaxy and had a threading dislocation density of 3.4×10^{6} cm^{-2}, measured by the wafer providers. Figure 3 shows secondary ion mass spectrometry profile of the growth layer. In the n-GaN drift layer, the density of silicon was 2.41×10^{16} cm^{-3} and the density of carbon was 1.52×10^{16} cm^{-3}. The depth profile obtained by C-V measurement showed that N_d-N_a was 1.95×10^{16} cm^{-3}. The device fabrication process was as follows. The growth layer was etched by inductively coupled plasma-reactive ion etching (ICP-RIE) with pure Cl_2 gas. ICP-RIE, which enables directional etching, was adopted to realize a vertical mesa structure. As an etching mask, Ni/Ti/Ni/Ti/Ni (50 nm/25 nm/100 nm/25 nm/100 nm) was deposited by electron beam (EB) vapor deposition and the mask was formed by a lift-off process. When only a thick Ni mask was deposited, the stress applied by Ni generated cracks in the photoresist and caused the failure of the lift-off process. The etching by ICP-RIE (CE-S, ULVAC) was performed at an antenna power of 150 W, a bias power of 15 W, and a Cl_2 flow rate of 30 sccm. The etching rate of GaN under these conditions was approximately 1.5 nm/s. The etching time was adjusted so that the etching depth of each device was 1 μm, 2.5 μm, 7.5 μm, and 10 μm. The measured etching depths are 1.13 μm, 2.29 μm, 7.80 μm, and 10.8 μm. The mesa diameters were 100-500 μm for each device. The p-type GaN layer was activated by rapid thermal annealing (RTA) in a nitrogen atmosphere at 700 ℃ for 5 min. A Ni/Au (20 nm/200 nm) anode was deposited by EB vapor deposition and formed by the lift-off process. Sintering annealing was performed in an oxygen atmosphere at 525 ℃ for 5 min by RTA. Subsequently, a 3.5-μm-thick polyimide layer was coated to protect the side wall from a discharge in air. Patterning was performed by photolithography to form contact holes in polyimide. Finally, a bottom ohmic electrode was formed by depositing 200 nm Al by sputtering. Figures 2 (b) and (c) show the cross-sectional scanning electron microscopy (SEM) images of devices with the above structure fabricated by the same process. The side walls of these devices were passivated by alumina.

By using the Ni/Ti layered etching mask, it was possible to realize a mesa structure having a vertical side-wall angle of 90°±1°. This indicates that the structure used in the simulation was reproduced by the fabricated devices.

The forward J-V characteristics of the devices with the mesa diameter of 200 μm are shown in Figure 4 (a). Regardless of the mesa depth, the specific on-resistance was 0.8 mΩ cm^2 and the ideality factor was 2.2. This indicates that all devices were undamaged by deep etching. The reverse J-V characteristics are shown in Figure 4 (b). In the devices with mesa depths of 1.13 μm and 2.29 μm, the leakage current was large and the breakdown voltage was as low as -450 V to -600 V. The breakdown was destructive in these devices. These devices had a large variation in their characteristics. Therefore, it is considered that the electric field relaxation at the device edge was insufficient. On the other hand, the leakage current was reduced by about four orders of magnitude in the devices with a mesa depth of 7.80 μm. The breakdown voltage was improved to -880 V for almost all devices, and the variation of the characteristics was small. In the devices with a mesa depth of 10.8 μm, the breakdown voltage was not improved (-880 V), but the leakage current was further reduced by about one order of magnitude and the variation was smaller. A nondestructive voltage breakdown was confirmed in these devices with mesa depths of 7.80 μm and 10.8 μm. In addition, it was confirmed that the breakdown voltage was the same value in devices with the mesa diameters of 100 μm, 200 μm, 340 μm, and 500 μm.

The temperature dependence of the reverse J-V characteristics was measured using a device with the mesa depth of 10.8 μm and the mesa diameter of 200 μm to confirm that the nondestructive breakdown was an avalanche breakdown. If the voltage breakdown upon applying a high voltage is an avalanche breakdown, the leakage current will increase owing to the increase in the number of carriers and the avalanche breakdown voltage will increase owing to greater scattering with increasing temperature.[12,14,21] Figure 5 shows the reverse J-V characteristics for device temperatures of 25 ℃ to 150 ℃ in 25 ℃ increments. The temperature dependence of the reverse J-V characteristics confirmed the occurrence of avalanche breakdown in the device with the mesa depth of 10.8 μm.

The breakdown field was calculated to be 2.48 MV/cm using the avalanche breakdown voltage and the doping density obtained by C-V measurement. This is less than the theoretical value for GaN, 3.24 MV/cm.[25,26] To investigate the factors causing the degradation of the breakdown field, the current amplification point was confirmed by emission microscopy (PHEMOS-1000, Hamamatsu Photonics). This microscopy can accurately specify the position of light emission by superimposing an emission topography

image and a device optical image. This technology has already been used for SiC and GaN devices.[27,28] By using this microscopy, it was possible to capture the emission due to the current when a reverse high voltage was applied and determine the point where the current was intensified. Figure 6 (a) shows the emission microscopy image at the avalanche breakdown voltage of the device with the mesa depth of 10.8 μm and the mesa diameter of 340 μm. Sparse emission was observed throughout the inside of the device. The emission was also observed at the mesa edge because the internal emission was extracted from the deeply etched side wall. In fact, no emission was observed before avalanche breakdown from the device edge. It has been reported that the emission due to the leakage current from dislocations is dotlike.[27] Therefore, this emission pattern was not caused by the dislocations. The emission pattern at avalanche breakdown was consistent with the step bunching observed by optical microscopy [Figs. 6 (a), (b)]. It is considered that the sparse emission at avalanche breakdown reflected the internal compensation of carbon and nonuniformity of silicon incorporated in bunched step edge.[29-31]

In summary, we greatly reduced the leakage current and improved the breakdown voltage of a GaN p-n diode using a vertically and deeply etched mesa structure. We also succeeded in observing a stable nondestructive voltage breakdown and obtained evidence by the evaluation of the temperature dependence that this phenomenon was an avalanche breakdown. The measured breakdown field in this study was 2.48 MV/cm. It is considered that the cause of the degradation of the breakdown field was the fluctuation of the doping density due to step bunching. It is expected that the essential physical properties can be derived by applying the structure in this paper to a device with a uniformly doped epitaxial layer.

Acknowledgments

This work was supported by MEXT “Program for research and development of next-generation semiconductor to realize energy-saving society.”

References

1) J. K. Sheu, M. L. Lee, and W. C. Lai, Appl. Phys. Lett. **86**, 052103 (2005).
2) X. A. Cao, H. Lu, S. F. LeBoeuf, C. Cowen, and S. D. Arthur, Appl. Phys. Lett. **87**, 053503 (2005).
3) Y. Yoshizumi, S. Hashimoto, T. Tanabe, and M. Kiyama, J. Cryst. Growth **298**, 875, (2007).
4) C. Gupta, Y. Enatsu, G. Gupta, S. Keller, and U. K. Mishra, Phys. Status Solidi A **213**, 878, (2016).
5) F. Roccaforte, P. Fiorenza, G. Greco, R. L. Nigro, F. Giannazzo, A. Patti, and M. Saggio, Phys. Status Solidi A **211**, 2063 (2014).
6) K. Motoki, T. Okahisa, R. Hirota, S. Nakahata, K. Uematsu, and N. Matsumoto, J. Cryst. Growth **305**, 377, (2007).
7) T. Yoshida, Y. Oshima, T. Eri, K. Ikeda, S. Yamamoto, K. Watanabe, M. Shibata, and T. Mishima, J. Cryst. Growth **310**, 5, (2008).
8) R. Dwiliński, R. Doradziński, J. Garczyński, L. Sierzputowski, R. Kucharski, M. Zając, M. Rudziński, R. Kudrawiec, J. Serafińczuk, and W. Strupiński, J. Cryst. Growth **312**, 2499 (2010).
9) H. Geng, H. Sunakawa, N. Sumi, K. Yamamoto, A. A. Yamaguchi, and A. Usui, J. Cryst. Growth **350**, 44 (2012).
10) X. Ke, W. Jian-Feng, and R. Guo-Qiang, Chin. Phys. B **24**, 066105 (2015).
11) I. C. Kizilyalli, P. Bui-Quanga, D. Disney, H. Bhatia, and O. Aktas, Microelectron. Reliab. **55**, 1654 (2015).
12) D. Disney, H. Nie, A. Edwards, D. Bour, H. Shah, and I. C. Kizilyalli, Proc. *Int. Symp. Power Semicond. Devices ICs*, Kanazawa, Japan, 59 (2013).
13) I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, IEEE Trans. Electron Devices **62**, 414 (2015).
14) K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, IEEE Electron Device Lett. **37**, 161 (2016).
15) T. Kachi and T. Uesugi, Sens. Mater. **25**, 219 (2013).
16) T. P. Chow, V. Khemka, J. Fedison, N. Ramungul, K. Matocha, Y. Tang, and R. J. Gutmann, Solid-State Electron. **44**, 277 (2000).
17) K. Nomoto, Y. Hatakeyama, H. Katayose, N. Kaneda, T. Mishima, and T. Nakamura, Phys. Status Solidi A **208**, 1535 (2011).
18) Y. Hatakeyama, K. Nomoto, N. Kaneda, T. Kawano, T. Mishima, and T. Nakamura, IEEE Electron Device Lett. **32**, 1674 (2011).

19) Y. Hatakeyama, K. Nomoto, A. Terano, N. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, Jpn. J. Appl. Phys. **52**, 028007, (2013).

20) H. Ohta. K. Hayashi, F. Horikiri, M. Yoshino, T. Nakamura, and T. Mishima, Jpn. J. Appl. Phys. **57**, 04FG09 (2018).

21) I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, and D. Bour, IEEE Trans. Electron Devices **60**, 3067–3070 (2013).

22) J. R. Dickerson, A. A. Allerman, B. N. Bryant, A. J. Fischer, M. P. King, M. W. Moseley, A. M. Armstrong, R. J. Kaplar, I. C. Kisilyalli, O. Aktas, and J. J. Wierer, Jr., IEEE Trans. Electron Devices **63**, 419 (2016).

23) J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, and P. Fay, Appl. Phys. Lett., **113**, 023502 (2018).

24) H. Fu, K. Fu, X. Huang, H. Chen, I. Baranowski, T. Yang, J. Montes, and Y. Zhao, IEEE Electron Device Lett., **39**, 1018 (2018).

25) B. J. Baliga, Semicond. Sci. Technol. **28**, 074011 (2013).

26) J. Kolník, İ. H. Oğuzman, K. F. Brennan, R. Wang, and P. P. Ruden, J. Appl. Phys. **81**, 726 (1997).

27) S. Usami, Y. Ando, A. Tanaka, K. Nagamatsu, M. Deki, M. Kushimoto, S. Nitta, Y. Honda, H. Amano, Y. Sugawara, Y. Yao, and Y. Ishikawa, Appl. Phys. Lett. **112** 182106 (2018).

28) H. Fujiwara, H. Naruoka, M. Konishi, K. Hamada, T. Katsuno, T. Ishikawa, Y. Watanabe, and T. Endo, Appl. Phys. Lett. **101**, 042104 (2012).

29) H. Fujikura, K. Hayashi, F. Horikiri, Y. Narita, T. Konno, T. Yoshida, H. Ohta, and T. Mishima, Appl. Phys. Express **11**, 045502 (2018).

30) T. Tanaka, N. Kaneda, T. Mishima, Y. Kihara, T. Aoki, and K. Shiojima, Jpn. J. Appl. Phys. **54**, 041002 (2015).

31) K. Shiojima, T. Hashizume, F. Horikiri, T. Tanaka, and T. Mishima, Phys. Status Solidi B **255**, 1700480 (2018).

Figure Captions

Fig. 1. (a) Schematic cross section of the vertical GaN p-n diode used for simulation. (b) Simulated electric field distributions of the p-n diodes when a reverse bias of -800 V was applied for mesa depths of 1 μm, (c) 2.5 μm, (d) 4 μm, (e) 5 μm, and (f) 10 μm.

Fig. 2. (a) Schematic cross section of the vertical GaN p-n diode with polyimide passivation. The bottom electrode has a window under the mesa to observe the emission. (b) Cross-sectional SEM images of the vertical GaN p-n diode with alumina passivation and mesa depths of 6.71 μm, and (c) 8.43 μm.

Fig. 3. SIMS profile of the growth layer of the vertical GaN p-n diode.

Fig. 4. Forward and reverse J-V characteristics of the vertical GaN p-n diode with polyimide passivation.

Fig. 5. Temperature dependence of reverse J-V characteristics of a vertical GaN p-n diode with a mesa depth of 10.8 μm.

Fig. 6. (a) Emission microscopy image of p-n diode with high reverse bias of -879 V applied. (b) Optical microscopy image.

Template for APEX (Jan. 2014)

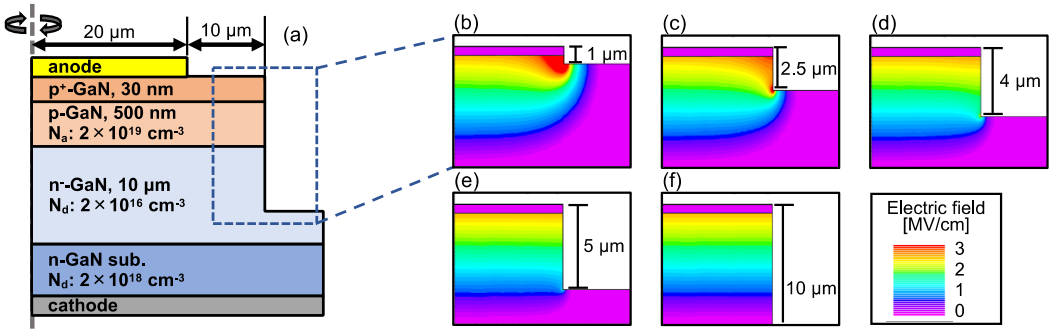

Fig.1.

Template for APEX (Jan. 2014)

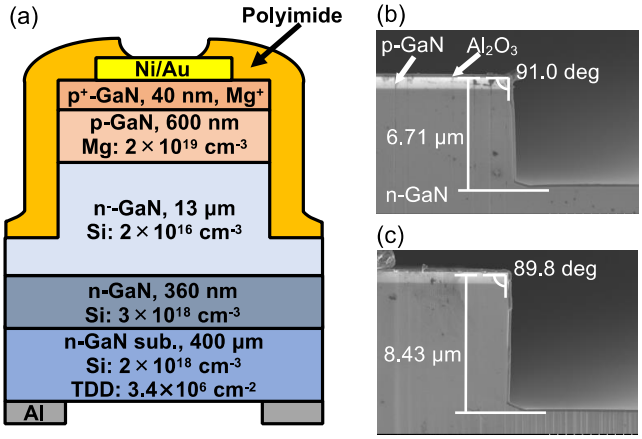

Fig. 2.

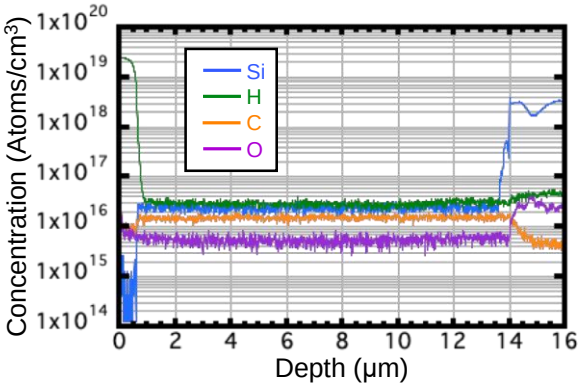
Concentration (Atoms/cm³)
1x10²⁰
1x10¹⁹
1x10¹⁸
1x10¹⁷
1x10¹⁶
1x10¹⁵
1x10¹⁴
Si
H
C
O
0
2
4
6
8
10
12
14
16
Depth (μm)

Fig. 3.

Template for APEX (Jan. 2014)

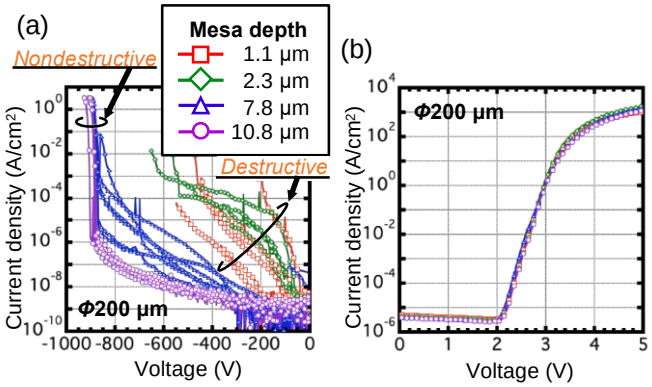

Fig. 4.

Template for APEX (Jan. 2014)

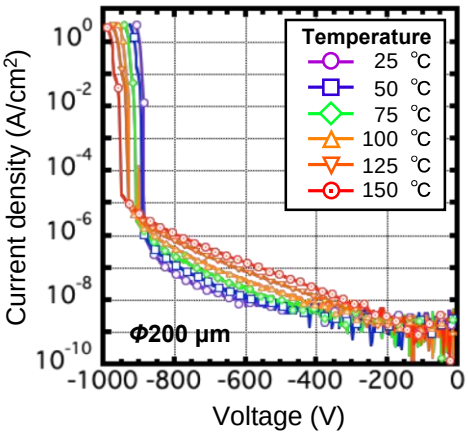

Fig. 5.

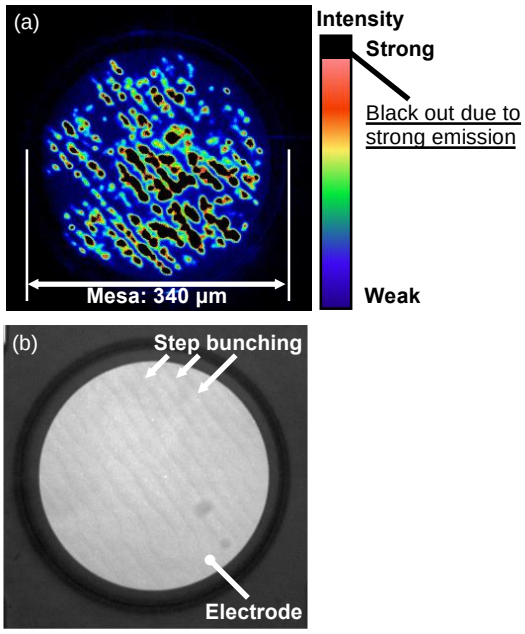
(a)
Intensity
Strong
Black out due to strong emission
Weak
Mesa: 340 μm
(b)
Step bunching
Electrode

Fig. 6.