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Dual-gate field-effect transistors of octathio[8]circulene thin-films with ionic liquid and SiO_2 gate dielectrics

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Dual-gate organic thin-film transistors (OTFTs) of octathio[8]circulene (1) with ionic liquid and SiO_2 gate dielectrics lead to good transistor performance with a high on/off ratio ($\sim 10^5$), a low threshold voltage (~ -5 V), a low subthreshold slope (~ 150 mV/decade), and low power operation, thus surpassing the performance of the single-gate OTFTs of 1. This operation is a promising method for improving the carrier concentrations in OTFTs and for realizing high-performance OTFTs. © *2010 American Institute of Physics*. [doi:10.1063/1.3491807]

Organic thin-film transistors (OTFTs) have attracted much attention due to their numerous advantages, including their flexibility, processability, and low cost.[1] It is notable that the OTFT performance depends on the dielectric layer between the gate electrode and the organic semiconductor. Since conventional SiO_2 layers suffer from low carrier accumulation due to their low capacitance,[2] various attempts have been made to replace this inorganic material with high-capacitance organic polymers or electrolyte solutions.[3,4] For instance, Iwasa and coworkers[5] have reported electrochemical field-effect transistors in which high-density carrier accumulations have been achieved through the electric double layers (EDLs) formed on the surfaces of semiconductors in the gate electrolyte solutions. In the EDL-OTFTs, ionic liquids have been utilized as gate electrolytes due to their stability in air and their nonvolatility even under high vacuum; they bring about a fast response to applied voltage in addition to a high-density carrier accumulation.[6] However, the ionic-liquid-gate OTFTs suffer from a significant drawback, namely, the surface damage that occurs under high applied voltages.

In addition to the conventional single-gate structure, dual-gate field effect transistors have been developed. These transistors are advantageous, as independent control of the two gate biases can optimize the device performance and each bias voltage can be very low.[7] While this operation mechanism is promising for improving the performance of OTFTs and for elucidating the charge accumulation and the carrier transport in them, its application to organic transistors has been very limited.[8,9]

Diverse organic semiconductors with characteristic features such as extended π conjugations, sulfur–sulfur contacts, polymer frameworks, etc., have been examined for OTFTs.[10] Among them, a fully fused oligothiophene, octathio[8]circulene (1), called "sulflower" [see Fig. 1(a)], is a new material, possessing dense three-dimensional close packing in its crystals and chemical stability.[11–13] Perepichka and coworkers[14] have fabricated an OTFT of 1 with Au electrodes and an SiO_2 gate dielectric layer, and have obtained a hole mobility of 9×10^{-3} cm^2/V s and a relatively high threshold gate voltage of -45 V. In our previous works, we have revealed the electrochemical oxidation process of the thin film of octathio[8]circulene in an ionic liquid, *N*, *N*-diethyl-*N*-methyl (2-methoxyethyl) ammonium bis(trifluoromethylsulfonyl)imide {abbreviated as DEME-TFSI [see Fig. 1(a)]},[15] which is stable in air/water and has a wide potential window (approximately 4 V). We also fabricated a single-gate EDL-OTFT of octathio[8]circulene with this ionic liquid, taking advantage of the persistency of 1 in ionic liquids. The EDL-OTFTs of 1 exhibited a stable transistor performance with a rather high mobility of 0.02 cm^2/V s, a high carrier accumulation of 3.4×10^{12} cm^{-2}, and a very

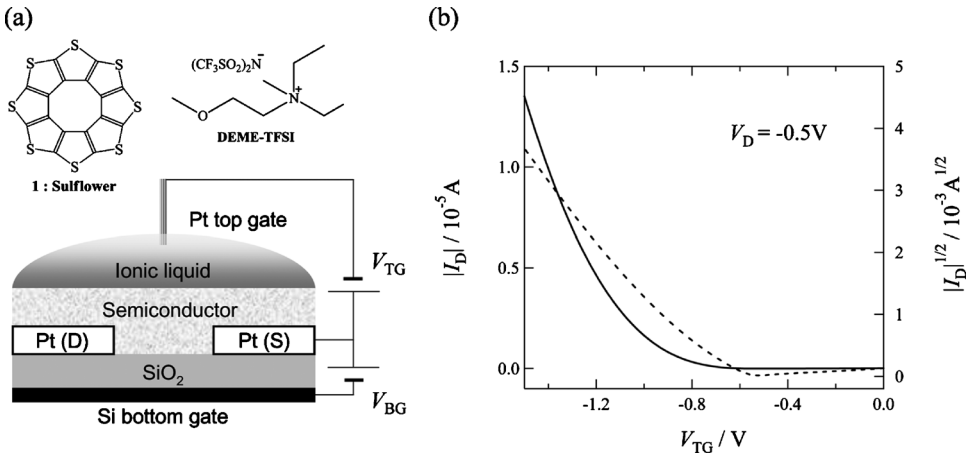

FIG. 1. (a) Dual-gate EDL-OTFT, consisting of an organic semiconductor 1 and an ionic liquid DEME-TFSI. (b) Transfer characteristics of the EDL-OTFT of 1 when the bottom-gate circuit is open. The solid and broken curves represent the $|I_D|$ vs V_{TG} and $|I_D|^{1/2}$ vs V_{TG} plots, respectively.

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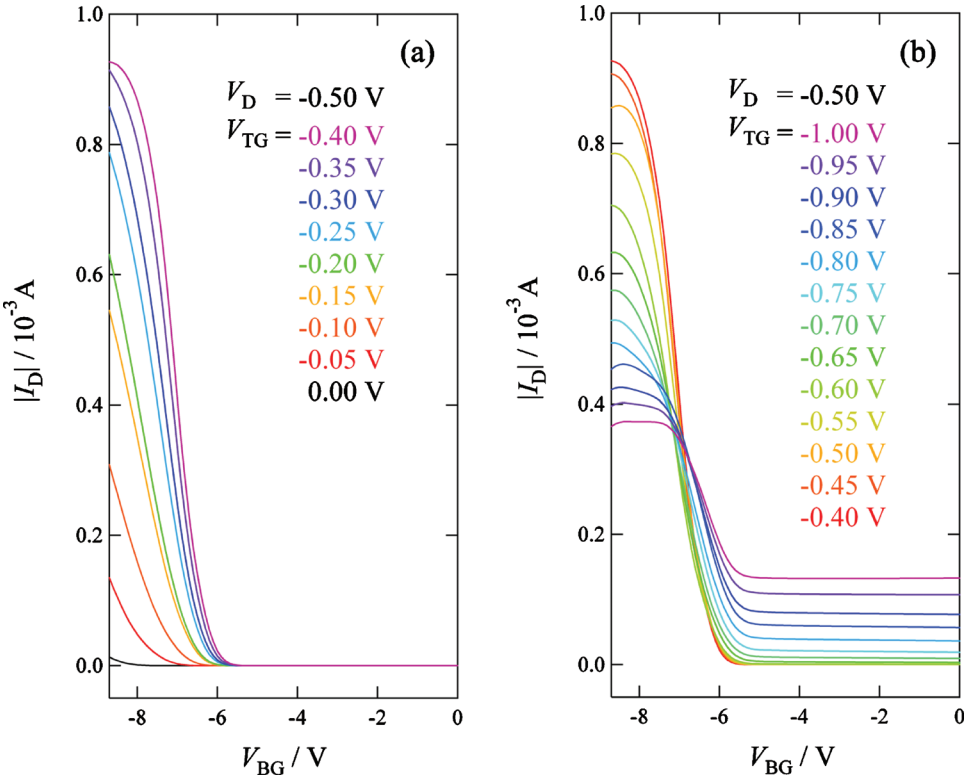

FIG. 2. (Color) V_{TG} dependence of the transfer characteristics of the dual-gate OTFT of octathio[8]circulene, operated by the bottom-gate voltage V_{BG}, in the range of (a) V_{TG}=0.0～−0.4 V and (b) −0.4～−1.0 V.

low-power operation with a threshold gate voltage of −0.5 V (versus the Ag/AgCl reference electrode).[16] In the present study, we fabricated a dual-gate OTFT of 1 with DEME-TFSI and SiO_2 as top- and bottom-gate dielectric materials, respectively. We will report the OTFT performance of this dual-gate system and compare it with that of the previous single-gate OTFTs of 1.[14,16] While dual-gate OTFTs with solid-state gate dielectrics have been reported previously,[7] the combination of the ionic liquid- and SiO_2-gate dielectrics will result in very good transistor performance because the SiO_2-gate voltage can keep the operation voltage at the ionic liquid gate low enough to avoid surface damage.

Figure 1(a) illustrates the structure of the dual-gate EDL-OTFT of 1. The material 1 was prepared by the method described in the literature.[11] The thin films of 1 with a thickness of 30 nm were prepared on the interdigitated array electrodes (Pt), in which the channel dimensions were w=100 cm in width and L=2 μm in length, and which were separated from the bottom-gate electrode (Si) by a SiO_2 layer of 300 nm, by vacuum vapor-deposition at 400 °C under 3×10^{-4} Pa at a rate of 1–3 nm min^{-1}, using a ULVAC VPC-260FN. The film thickness was monitored during deposition by a quartz crystal microbalance located adjacent to the sample position within the bell jar. In our previous studies, we revealed thin films of 1 in which the molecular planes were parallel to the substrates.[12] The electrolyte was of reagent grade and was used without further purification. The top-gate was prepared with a droplet of DEME-TFSI that covered the whole area of the thin film of 1, and a Pt wire that was inserted into the ionic liquid. Dual-gate OTFT performance tests were carried out by using an ADVANTEST R6246 dual-channel source meter at room temperature under dark and vacuum conditions in DEME-TFSI electrolytes [see Fig. 1(a).

Figure 1(b) shows the EDL-OTFT performance, namely, the source-drain current $|I_D|$ versus top-gate voltage V_{TG} plots, when the bottom-gate circuit is open. Note that the gate leakage current through the electrolytes is smaller than 0.2 μA. The values of $|I_D|$ drastically increase below a threshold gate voltage of V_{TG}^{th*}=−0.5 V, where * indicates that the SiO_2 bottom-gate is open. This behavior indicates that effective carrier doping takes place through the EDLs, when $V_{TG}<-0.5$ V. The obtained performance is nearly the same as that of the single-gate EDL-OTFTs of 1 with DEME-TFSI, as reported previously.[16]

Figure 2(a) shows the transfer characteristic, operated by the bottom-gate voltage V_{BG}, namely, $|I_D|$ versus V_{BG} plots, under a constant V_{TG} in the range from 0.0 to −0.4 V at a source-drain voltage of V_D=−0.5 V. At V_{TG}=0.0 V, the curve exhibits OTFT performance with a threshold voltage of V_{BG}^{th}=−7.8 V. When a negative V_{TG} was loaded, we observed a significant improvement in the transistor performance, even when $V_{TG}>V_{TG}^{th*}$ (=−0.5 V); the value of V_{BG}^{th} exhibited a significant increase with a decrease in V_{TG}. These results indicate that V_{TG} produces an effective field at the interface of the SiO_2 bottom gate dielectrics and assists with carrier doping from this gate. Figure 2(b) shows the $|I_D|$ versus V_{BG} plots in the range of $-0.4>V_{TG}>-1.0$ V at V_D=−0.5 V. When $V_{TG}<V_{TG}^{th*}$, the transistor performance is observed, but V_{TG} gradually increases the off current while it remains negligibly small in the range of $V_{TG}>V_{TG}^{th*}$.

Figure 3(a) shows the V_{TG} dependence of the on-off current ratio. It can be seen that high ratios of more than 10^4 are maintained in the range of $0.0>V_{TG}>-0.5$ V, while below −0.5 V, they show a quick decrease to approximately one at V_{TG}=−1.0 V. Figure 3(b) shows the V_{TG} dependencies of the subthreshold slope $\partial V_{BG}/\partial \log I_D$. In the range of $0.0>V_{TG}>-0.5$ V, the values of $\partial V_{BG}/\partial \log I_D$ are constantly low (<0.3 V/decade), while below −0.5 V, they show a gradual increase to approximately 3 V/decade at V_{TG}=−1.0 V. It is notable that the V_{TG}^{th*} value in Fig. 1(b)

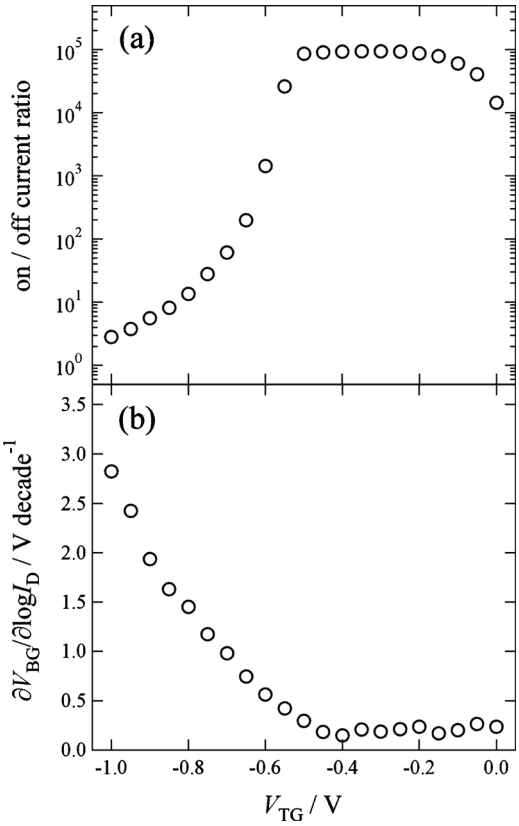

FIG. 3. (a) V_{TG} dependence of the on-off current ratio and (b) the subthreshold slope.

roughly agrees with the critical V_{TG} value (−0.5 V) in the dependencies shown in Figs. 3(a) and 3(b). The surface condition of the thin film of 1 is considered to be significantly changed when $V_{TG}<-0.5$ V. This phenomenon is probably caused by penetration or/and adsorption of the counter ions to the thin film surface, which brings about a significant increase in the off-current, thus spoiling the transistor performance.

Figure 4 shows the dependence of V_{BG}^{th} on V_{TG}, which is extracted from Fig. 2. There is a linear relation between them with a slope of −3.2. In general, the dual-gate transistors show a relation between V_{BG}^{th} and V_{TG}, which is expressed by

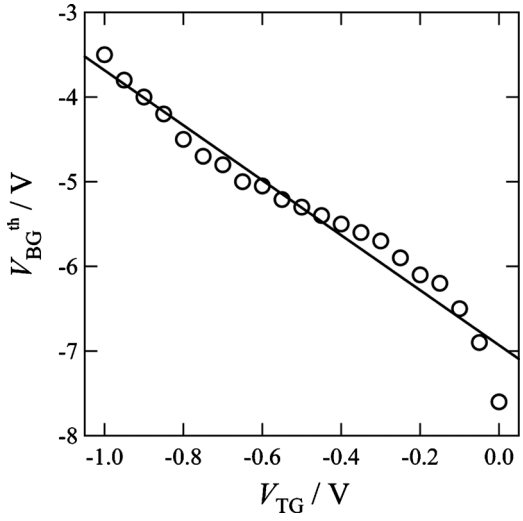

FIG. 4. V_{TG} dependence of the threshold bottom-gate voltage V_{BG}^{th}.

$$\frac{\partial V_{BG}^{th}}{\partial V_{TG}} = -\frac{CC_{TG}}{C_{BG}(C+C_{TG})}, \quad (1)$$

where C_{TG}, C_{BG}, and C are the capacitances of the top- and bottom-gate dielectrics and the semiconductor, respectively.[17] Therefore, the symmetric dual-gate OTFTs, composed of the same gate dielectrics, should exhibit a $\partial V_{BG}^{th}/\partial V_{TG}$ value of approximately –0.5.[8] In contrast, the values of C_{BG} and C_{TG} in the present dual-gate OTFT are 1.1×10^{-8} F/cm^2 and 1.1×10^{-6} F/cm^2, respectively.[18] Since C of the organic layer is estimated at 10^{-7} F/cm^2, the $\partial V_{BG}^{th}/\partial V_{TG}$ value would be on the order of tens, which can semiquantitatively explain the observed value.

In summary, we have fabricated a dual-gate OTFT of 1 with DEME-TFSI and SiO_2 gate dielectrics. The dual-gate operation led to very good transistor performance with a high on/off ratio, a low threshold voltage, a low subthreshold slope, and low power operation, all of which surpassed those of the single-gate OTFTs of octathio[8]circulene. The dual-gate operation using ionic liquid is a promising method for improving the carrier concentrations in OTFTs and for realizing high-performance OTFTs.

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[1] J. Zaumseil and H. Sirringhaus, Chem. Rev. (Washington, D.C.) **107**, 1296 (2007).
[2] J. Veres, S. Ogier, and G. Lloyd, Chem. Mater. **16**, 4543 (2004).
[3] V. Podzorov, V. M. Pudalov, and M. E. Gershenson, Appl. Phys. Lett. **82**, 1739 (2003).
[4] J. Lee, M. J. Panzer, Y. He, T. P. Lodge, and C. D. Frisbie, J. Am. Chem. Soc. **129**, 4532 (2007).
[5] K. Ueno, S. Nakamura, H. Shimotani, A. Ohtomo, N. Kimura, T. Nojima, H. Aoki, Y. Iwasa, and M. Kawasaki, Nature Mater. **7**, 855 (2008).
[6] S. Ono, S. Seki, R. Hirahara, Y. Tominari, and J. Takeya, Appl. Phys. Lett. **92**, 103313 (2008).
[7] Y. Kaneko, K. Tsutsui, and T. Tsukada, J. Non-Cryst. Solids **149**, 264 (1992).
[8] J. B. Koo, K. S. Suh, I. K. You, and S. H. Kim, Jpn. J. Appl. Phys., Part 1 **46**, 5062 (2007).
[9] F. Maddalena, M. Spijkman, J. J. Brondijk, P. Fonteijn, F. Brouwer, J. C. Hummelen, D. M. de Leeuw, P. W. M. Blom, and B. de Boer, Org. Electron. **9**, 839 (2008).
[10] A. Fukazawa and S. Yamaguchi, Asian J. Chem. **4**, 1386 (2009).
[11] K. Y. Chernichenko, V. V. Sumerin, R. V. Shpanchenko, E. S. Balenkova, and V. G. Nenajdenko, Angew. Chem., Int. Ed. **45**, 7367 (2006).
[12] T. Fujimoto, R. Suizu, H. Yoshikawa, and K. Awaga, Chem.-Eur. J. **14**, 6053 (2008).
[13] S. S. Bukalov, L. A. Leites, K. A. Lyssenko, R. R. Aysin, A. A. Korlyukov, J. V. Zubavichus, K. Y. Chernichenko, E. S. Balenkova, V. G. Nenajdenko, and M. Y. Antipin, J. Phys. Chem. A **112**, 10949 (2008).
[14] A. Dadvand, F. Cicoira, K. Y. Chernichenko, E. S. Balenkova, R. M. Osuna, F. Rosei, V. G. Nenajdenko, and D. F. Perepichka, Chem. Commun. (Cambridge) **2008**, 5354.
[15] T. Fujimoto, M. M. Matsushita, H. Yoshikawa, and K. Awaga, J. Am. Chem. Soc. **130**, 15790 (2008).
[16] T. Fujimoto, M. M. Matsushita, and K. Awaga, Chem. Phys. Lett. **483**, 81 (2009).
[17] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, IEEE Trans. Electron Devices **50**, 830 (2003).
[18] Y. J. Kim, Y. Matsuzawa, S. Ozaki, K. C. Park, C. Kim, M. Endo, H. Yoshida, G. Masuda, T. Sato, and M. S. Dresselhaus, J. Electrochem. Soc. **152**, A710 (2005).