A simple gate driver design for GaN-based switching devices with improved surge voltage and switching loss at 1-MHz operation

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In power electronics, the impedance of reactance components increases proportionally with frequency; therefore, the sizes of reactance components can be reduced by increasing the switching frequency. Gallium nitride (GaN)-based devices have received significant attention in high-frequency applications because the figure-of-merit of GaN is superior to that of silicon (Si). However, for high-frequency operation, a trade-off relationship between the surge voltage induced by parasitic inductances, and the switching loss becomes significant. Therefore, in this study, we propose a gate driver that improves the trade-off relationship. This gate driver was obtained via the addition of simple logic circuits and capacitors to a conventional gate driver. The effectiveness of our proposed circuit was verified via SPICE simulations with Cadence Spectre using 180-nm CMOS technology. The simulation results show that by operating at 1 MHz, this circuit can help reduce the surge voltage by 12.2% and the switching loss by 14.3%.

1. Introduction

In power electronics devices such as electric vehicles and household appliances, more compact circuits can be achieved by increasing the switching frequency of switching devices.[1-3] Contemporary developments in gallium nitride (GaN)-based power switching devices contribute to the increase of the switching frequency because the semiconductor properties of GaN are superior to those of silicon (Si).[4-8] Table I summarizes the properties of Si and GaN. The figure of merit of GaN is greater than that of Si, indicating that GaN-based devices are more suitable than Si-based devices for use as high-speed switching devices. Thus, over the last decade, Si-based devices have been gradually replaced with GaN-based devices in high-frequency applications. Using GaN-based devices as switching components is an effective way to increase the switching frequency; however, the commercialization of gate drivers for GaN-based devices has not progressed compared with gate drivers for Si-based devices. One reason for this drawback is that the surge voltage is inversely proportional to the switching transient time. Although GaN-based devices enable very short switching transient owing to their low gate charge, the effect of the surge voltage in GaN-based devices is more significant than that in Si-based devices. The surge voltage is explained in detail below.

Figures 1(a) and 1(b) show the conventional gate driver and transient waveforms of the gate-source voltage, drain-source voltage, and drain current of power devices. A gate resistor R_G is used to adjust the switching transient time and surge voltage. A low gate resistance causes rapid switching and a high surge voltage. Meanwhile, a high gate resistance results in slow switching and a low surge voltage. Therefore, a trade-off relationship between the switching loss, which is proportional to switching transient time, and the surge voltage is essential.

The switching loss is expressed by Eq. (1), where V_{DS} and I_D are the drain-source

voltage and drain current of the switching device, respectively, and f_{sw} is the switching frequency.

$$E_{switching} = \left\{\int_{t1}^{t3} V_{DS} \cdot I_D dt + \int_{t6}^{t8} V_{DS} \cdot I_D dt\right\} \cdot f_{sw} \quad (1)$$

Equation (1) shows that the switching loss can be reduced by reducing the switching transient time. Additionally, the switching loss increases proportionally with the switching frequency.[9)]

The surge voltage needs to be controlled; otherwise, it may damage the switching device permanently. The surge voltage is expressed by Eq. (2), where V_{DD} is a supply voltage, and L_d and L_s are the parasitic inductances at the drain and source nodes, respectively. Moreover, $\frac{di}{dt}$ is the rate of current that flows to the output capacitance of the switching device, and it changes over time.

$$V_{surge} = -(L_d + L_s) \cdot \frac{di}{dt} + V_{DD} \quad (2)$$

The surge voltage occurs because the parasitic inductance, the loop resister and output capacitor of the switching device form a series loop and resonate at a resonant frequency. [10)] Completely eliminating the parasitic inductance is not possible although various studies have been reported.[11-14)] The following explanation mainly applies to the turn-off transient because parasitic components affect the circuit operation strongly during the turn-off transient as compared to the turn-on transient.[15)]

The current that flows to the output capacitance of the switching device during the turn-off transient is expressed by Eq. (3), where C is the output capacitance of the switching device.

$$I = C \cdot \frac{dV_{DS}}{dt} \quad (3)$$

Therefore, attenuating $\frac{dV_{DS}}{dt}$ during the turn-off transient is necessary to ensure that the surge voltage does not exceed the rated voltage of the switching device.

Various gate drivers have been studied to improve the trade-off relationship between the surge voltage and switching loss.[16-32)] The majority of the reported gate drivers weaken the drive strength at the Miller Plateau period (t6-t7) to achieve both rapid switching and device protection against surge voltage.

However, most of these reported gate drivers require a complicated analog or digital control system, because of which the size and cost of the entire circuit increase.

Accordingly, this study proposes a simple gate driver obtained via the addition of simple

logic circuits and capacitors to a conventional gate driver. The simulation results show that this proposed gate driver can effectively improve the trade-off relation. The remainder of this paper is organized as follows. Section 2 describes the operating principle of the proposed gate driver. Section 3 verifies the validity of the methodology through simulation results. Finally, Section 4 presents the conclusions of the study.

2. Principle of proposed gate driver

Figure 2 shows the block diagram of the proposed gate driver. This gate driver uses simple circuits, such as inverters with different gate-threshold voltages, to improve the trade-off relationship between the surge voltage and switching loss. The added circuit weakens the drive strength at the Miller Plateau period during the turn-off transient to attenuate $\frac{dV_{DS}}{dt}$. It should be noted that high and low output voltages represent 5 V and 0 V, respectively.

2.1 Effect of two inverters and XNOR

Figures 3(a) and 3(b) show the topology of inverter1 and inverter2 illustrated in Fig. 2, respectively. The two inverters have the same topologies, but different parameters that affect the DC voltage transfer characteristic, β_n and β_p that are expressed by Eqs. (4) and (5), respectively.

$$\beta_n = \frac{W_n}{L_n} \cdot \mu_n C_{ox} \tag{4}$$

$$\beta_p = \frac{W_p}{L_p} \cdot \mu_p C_{ox} \tag{5}$$

where W_n, L_n and μ_n are the gate width, gate length and mobility of NMOS of the inverter, respectively; W_p, L_p and μ_p are the PMOS counterparts; and C_{ox} is the capacitance per unit area of the oxide layer. Herein, μ_n is approximately 2.5 times μ_p. These inverters have different gate-threshold voltages V_{TH}, as shown in Fig. 4, because the gate-threshold voltage depends on the ratio of β_n to β_p. The ratio of β_n to β_p of inverter1 is about 1 : 1, and that of inverter2 is about 3.6 : 1. The gate-threshold voltage is the voltage wherein the input and output voltages are equal, and it can be shifted by adjusting the ratio of β_n to β_p. While the gate-threshold voltage of inverter1 in Fig. 2 is approximately $\frac{V_{DD}}{2}$, that of inverter2 falls below $\frac{V_{DD}}{2}$; therefore, the output of inverter1

becomes high before the output of inverter2 during the turn-off transient. The output of XNOR can be changed to low at the Miller Plateau period by adjusting β_n and β_p. As a result, the entire pull-down strength of the gate driver is reduced at the Miller Plateau period.

Additionally, the times at which the outputs of two inverters become low are different during the turn-on transient. However, the added circuit has no effect on the gate driver during the turn-on transient because the time when the outputs of the inverters are different is too small for XNOR and is therefore negligible.

2.2 Effect of external capacitors

The pull-down strength may not be weakened only in the Miller Plateau period owing to the dispersion of characteristics. Circuit designers should address this since contemporary technology cannot be used to manufacture a circuit with exactly the same characteristics as the simulated circuit. It is possible to match the period when PMOS1 is kept on in the Miller Plateau period because of external capacitors even after the circuit is implemented. For instance, in the case when the timing of turning on the PMOS is earlier than the start of the Miller Plateau period, as shown in Fig.5 (a), that problem can be addressed by increasing the capacity values accordingly, as shown in Fig.5 (b). The rise time of inverters can be controlled by changing the capacity values of external capacitors. Control parameters that can be adjusted after implementation is an advantage of this circuit.

2.3 Operation of proposed gate driver

Figure 6 shows the simplified steady-state control waveforms for gate-source voltage, inverters, XNOR, V_{DS} and gate current. Figures 7(a), 7(b) and 7(c) show operating phases of the proposed gate driver.

P0: The switching device is discharged by the buffer that has a strong pull-down strength to turn the device off during this phase as illustrated in Fig. 7(a). PMOS1 is kept off during this phase because the outputs of inverter1 and inverter2 are kept low.

P1: The output of inverter1 becomes high at the start of this phase, while that of inverter2 is kept low; therefore, the output of XNOR becomes low. As a result, the pull-down strength is weakened during this phase because PMOS1 is turned on in this phase as illustrated in Fig.7 (b). Therefore, $\frac{dV_{DS}}{dt}$ decreases and the surge voltage can be suppressed. Additionally,

PMOS1 is operated in the linear region because the voltages at the source and drain nodes of PMOS1 are almost constant at approximately 5 V and 2 V, respectively, during the Miller plateau period. The voltage at the source node is generated by the DC supply voltage, whereas the voltage at the drain node is almost the same as the gate-source voltage of the GaN-based device, as illustrated in Fig. 2. It should be noted that the voltage at the drain node is constant at approximately 2 V because the gate-source voltage of the GaN-based device used in this study is constant at approximately 2 V during the Miller plateau period, and PMOS1 is turned on during this period.[33)]

P2: The output of inverter2 becomes high at the start of this phase, and that of inverter1 is kept high. As a result, the switching device is completely turned off by the buffer at the end of this phase. In addition, PMOS1 is turned off because the output of XNOR is high during this phase.

3. Simulation results

Figure 8 shows the schematic of the SPICE simulation, where the GaN FET is modeled using the EPC2020 SPICE model and parasitic inductances are included. The proposed gate driver consists the conventional gate driver with low gate resistance and logic circuits. The pulse test is used to verify the effectiveness of the proposed gate driver in SPICE simulation compared with the conventional gate driver. The design specifications and the simulation conditions are shown in Table II. Figures 9(a) and 9(b) show the gate-source and drain-source voltages of the GaN FET, respectively, during the turn-on transient, whilst Figs. 10(a) and 10(b) show the corresponding values during the turn-off transient.

Although the gate-source voltage of the GaN FET resonates because of the parasitic inductance of the gate node, the input capacitance of the GaN FET and gate resistance, the resonance has little effect on the whole operation during the turn-on transient, as illustrated in Figs. 9(a) and 9(b). Moreover, the logic circuits of the proposed gate driver have no effect on the operation as mentioned above.

During the turn-off transient, the proposed gate driver and conventional gate driver with low gate resistance have the same pull-down strengths until the start of the Miller Plateau period. While the pull-down strength of the conventional gate driver does not change in the Miller Plateau period, that of the proposed gate driver is weakened. After the Miller Plateau

period, both of the fall down speed becomes equal because PMOS1 of the proposed gate driver is kept off. The switching transient time of the conventional gate driver with a large gate resistance increases although the surge voltage reduces because of the large gate resistance. As a result, both the surge voltage and switching transient time are reduced compared with those in conventional gate drivers, as shown in Fig. 10(b). The curve with blue dots shows the trade-off relationship between the switching loss and surge voltage in the conventional gate driver. The red triangle indicates that the proposed gate driver can reduce the surge voltage and switching loss by 12.2% and by 14.3%, respectively.

Table III shows the comparison table of this study and an LMG1020 released by Texas Instruments Inc. The surge voltage and switching loss of the LMG1020 were obtained using the SPICE model of the LMG1020, and the simulation was performed under the same conditions as specified in Table II. The LMG1020 is a gate driver for driving GaN-based devices in high-speed applications and is mainly composed of a buffer circuit similar to that in conventional gate drivers. As loss reduction is required for high-frequency applications, the LMG1020 with a conventional configuration cannot meet the market demand. Overall, the proposed gate driver is more useful than an LMG1020 for improving the trade-off relationship between the surge voltage and switching loss, as shown in Table III.

4. Conclusions

In this study, we propose a simple gate driver added to simple logic circuits for GaN-based devices operating at 1-MHz. The proposed gate driver can weaken the drive strength during the Miller Plateau period to improve the trade-off relationship between the switching loss and surge voltage. The proposed gate driver presents two remarkable advantages;

1. The control parameters can be adjusted after implementation although the proposed gate driver does not have a digital control system.
2. Since the proposed gate driver can be obtained via the addition of only simple logic circuits to the conventional gate driver, it can be easily implemented.

The simulation results show that at 1-MHz operation, this circuit can reduce the surge voltage by 12.2% and the switching loss by 14.3% when compared with the conventional gate driver. Moreover, the proposed gate driver is more useful than an LMG1020 for improving the trade-off relationship between the surge voltage and switching loss.

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Figure Captions

Fig. 1. (a) Conventional gate driver. (b) Transient waveforms of gate-source and drain-source voltages and drain current of power devices.

Fig. 2. Block diagram of the proposed gate driver.

Fig. 3. (a) Topology of inverter1. (b) Topology of Inverter2

Fig. 4. DC voltage transfer characteristics of inverter1 and inverter2.

Fig. 5. (a) Transient waveform of added circuits without external capacitors (b) Transient waveform of added circuits with external capacitors.

Fig. 6. Simplified steady-state control waveforms for gate-source voltage, inverters, XNOR, V_{DS} and gate current.

Fig. 7. (a) Operating phase P_0. (b) Operating phase P_1. (c) Operating phase P_2.

Fig. 8. Schematic of the SPICE simulation.

Fig. 9. (a) Gate-source voltage of the GaN FET during the turn-on transient. (b) drain-source voltage of the GaN FET during the turn-on transient.

Fig. 10. (a) Gate-source voltage of the GaN FET during the turn-off transient. (b) drain-source voltage of the GaN FET during the turn-off transient.

Fig. 11. Switching loss vs. surge voltage during the turn-off period at 50V switching for the GaN FET.

Tables

Table I. Material properties.

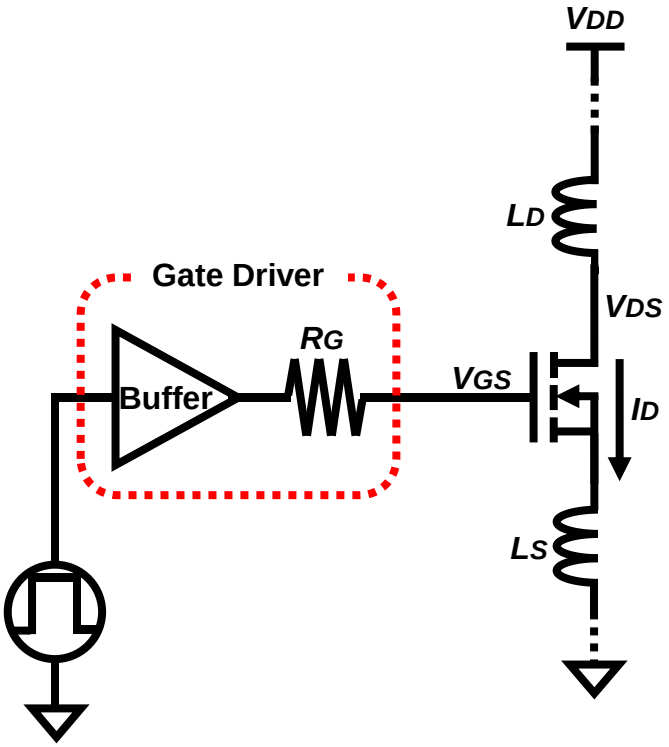
Material	Si	GaN
Bandgap [eV]	1.1	3.4
Electron mobility [cm^2/Vs]	1350	1500
Electric field for breakdown [MV/cm]	0.3	3.3
Figure of merit [$\varepsilon\mu_e E_c^3$]	1	1130

Table II. Design specifications and simulation conditions.

Pramater	Value
R_{ON} [Ω], PMOS1	3.5
Output impedance [Ω], Buffer	161
Typical C_{iss} [pF], EPC2020	1780
Typical C_{oss} [pF], EPC2020	1410
Low R_G [Ω]	1.5
Large R_G [Ω]	30
Operation frequency [MHz]	1
Supply voltage [V], GaNFET	50
Supply voltage [V], Gate driver	5

Table III. Comparison table of this study and LMG1020.

	LMG1020	This study
Surge voltage [V]	12.1	12
Switching loss [W]	3.6	2.8
UVLO	included	not included
Switching device	GaN device	GaN device



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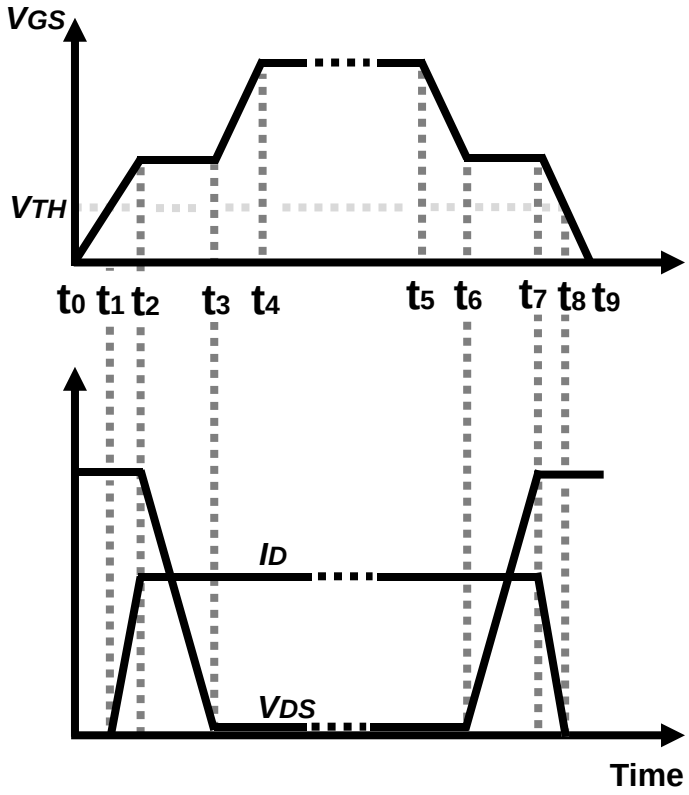


(b)

Fig. 1.

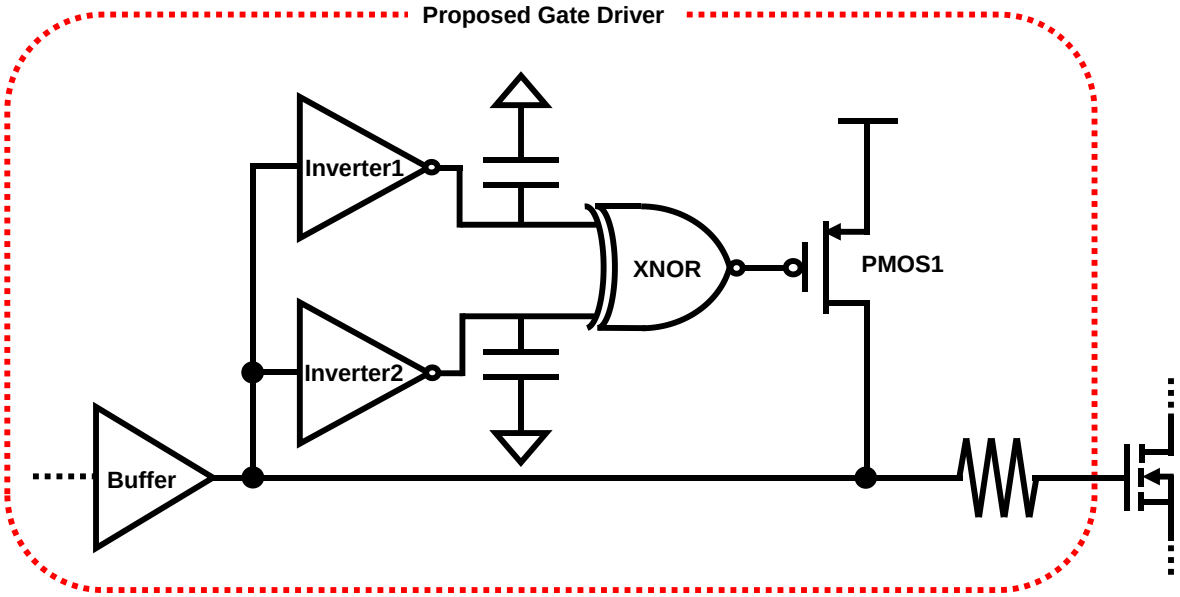
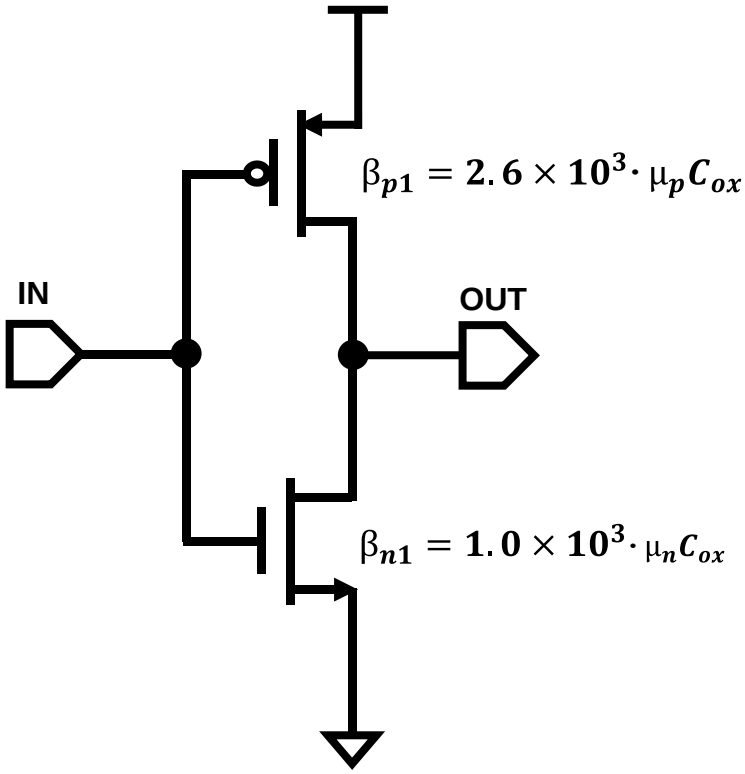
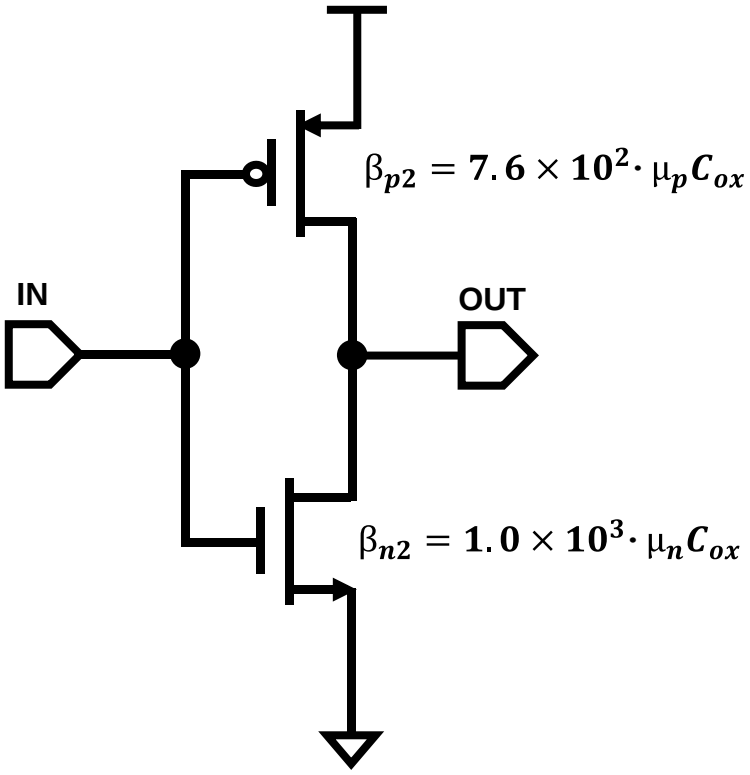

Proposed Gate Driver
Inverter1
Inverter2
Buffer
XNOR
PMOS1

Fig. 2.


$\beta_{p1} = 2.6 \times 10^3 \cdot \mu_p C_{ox}$
IN
OUT
$\beta_{n1} = 1.0 \times 10^3 \cdot \mu_n C_{ox}$

(a)


$\beta_{p2} = 7.6 \times 10^2 \cdot \mu_p C_{ox}$
IN
OUT
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(b)

Fig. 3.

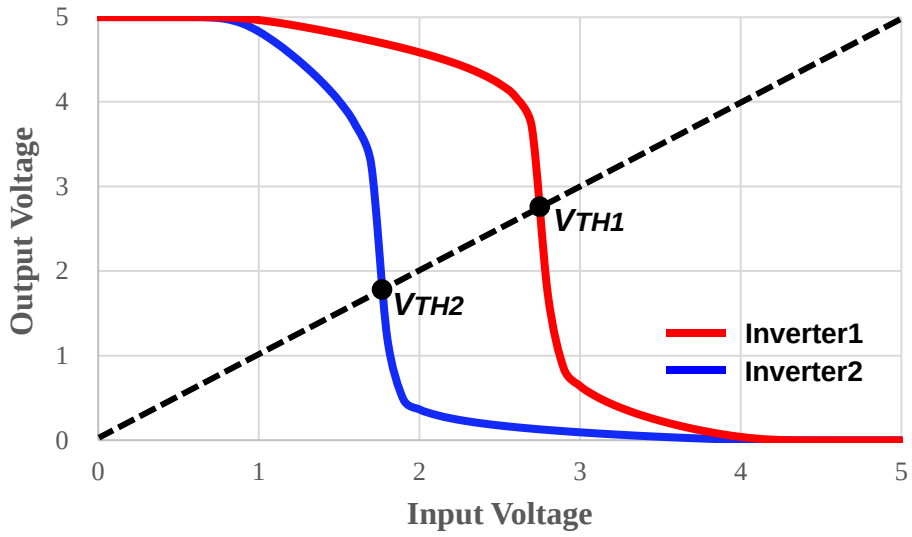
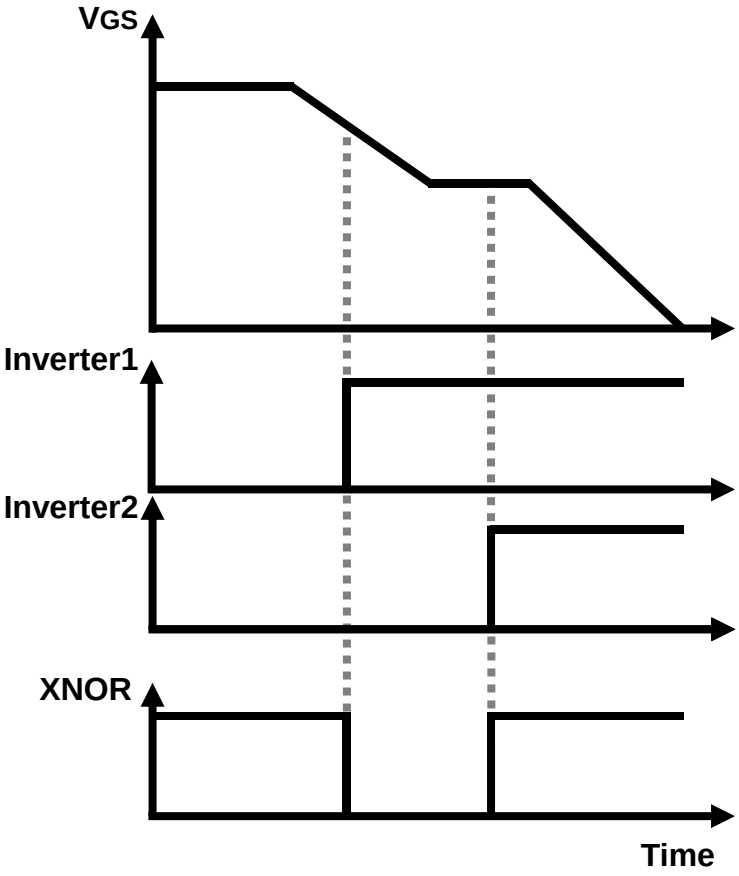

Output Voltage
Input Voltage
0
1
2
3
4
5
VTH1
VTH2
Inverter1
Inverter2

Fig. 4.



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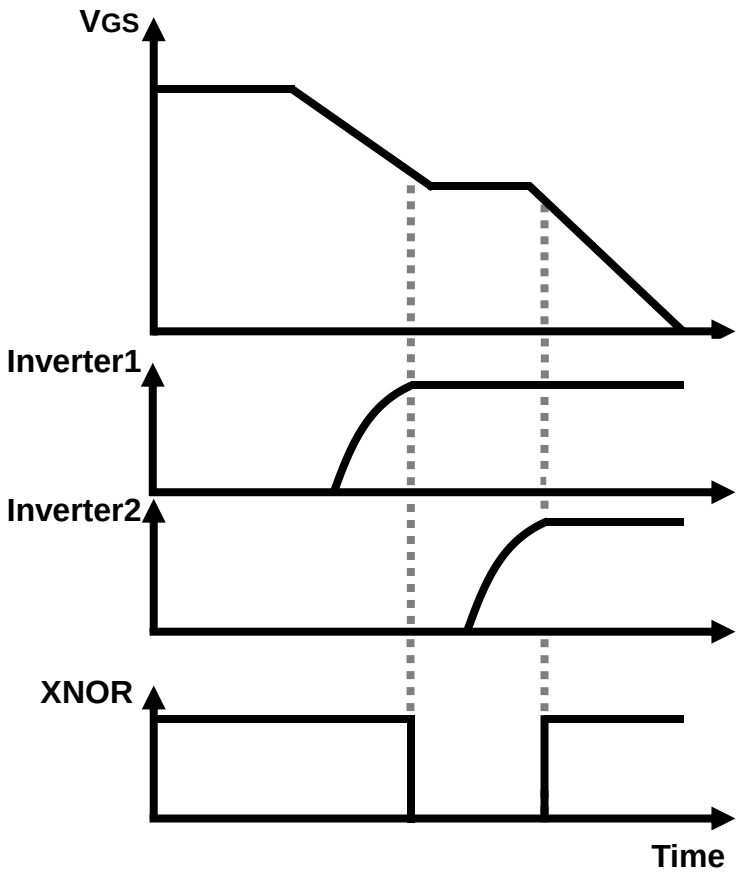


(b)

Fig. 5.

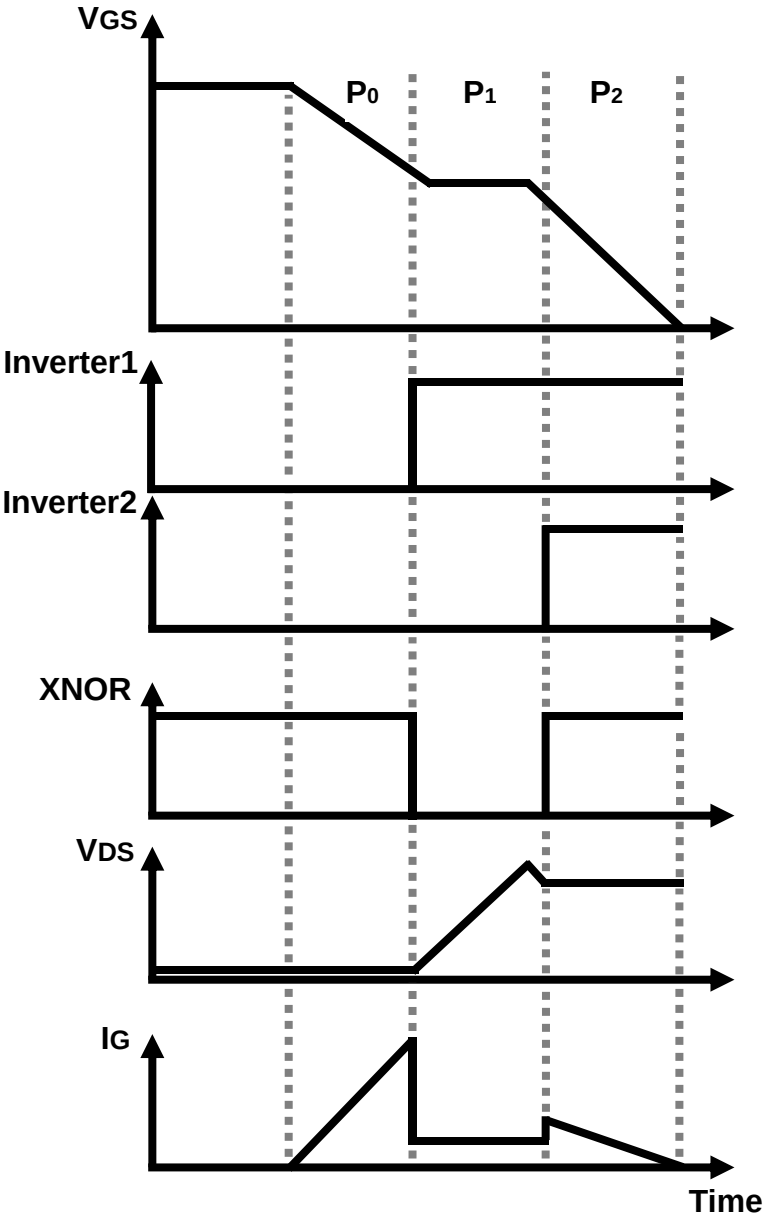
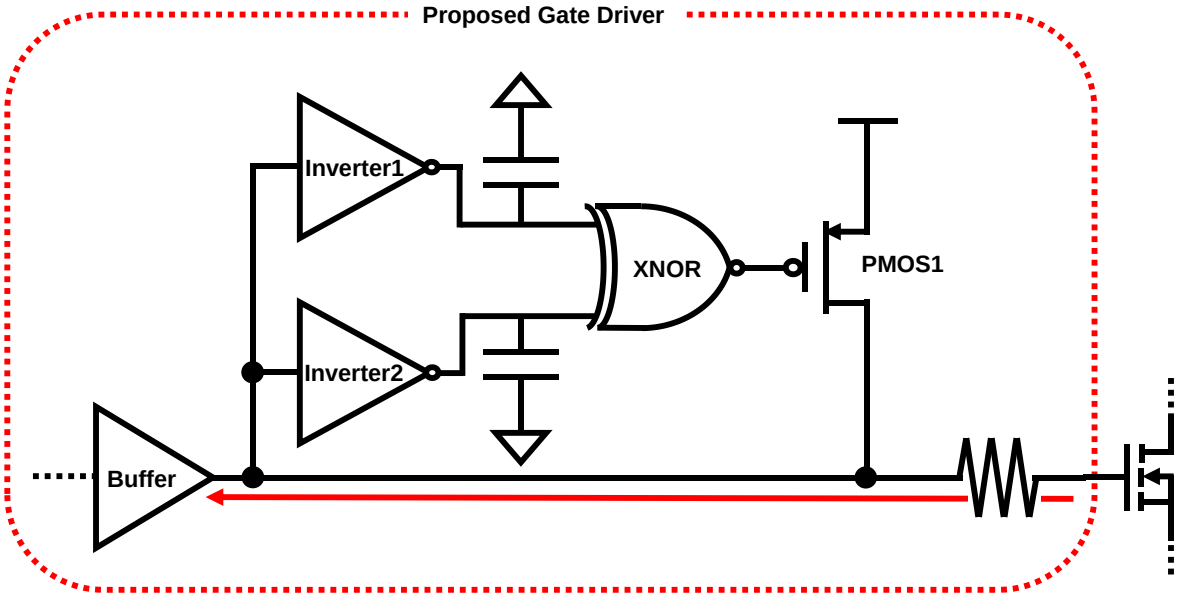
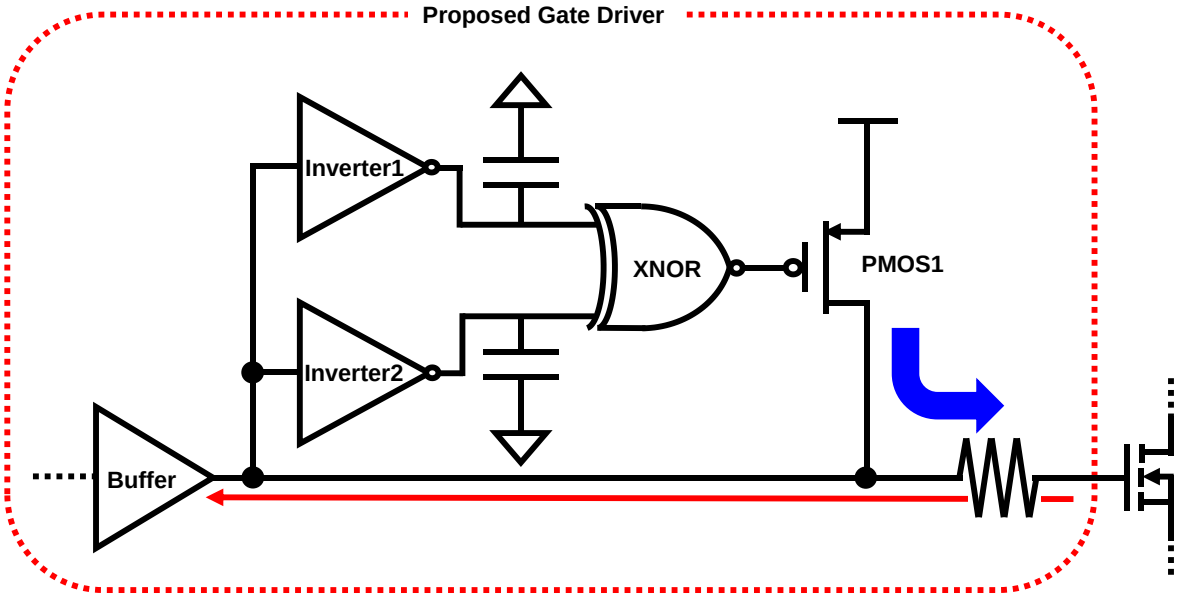


Fig. 6.


Proposed Gate Driver
Inverter1
Inverter2
XNOR
PMOS1
Buffer

(a)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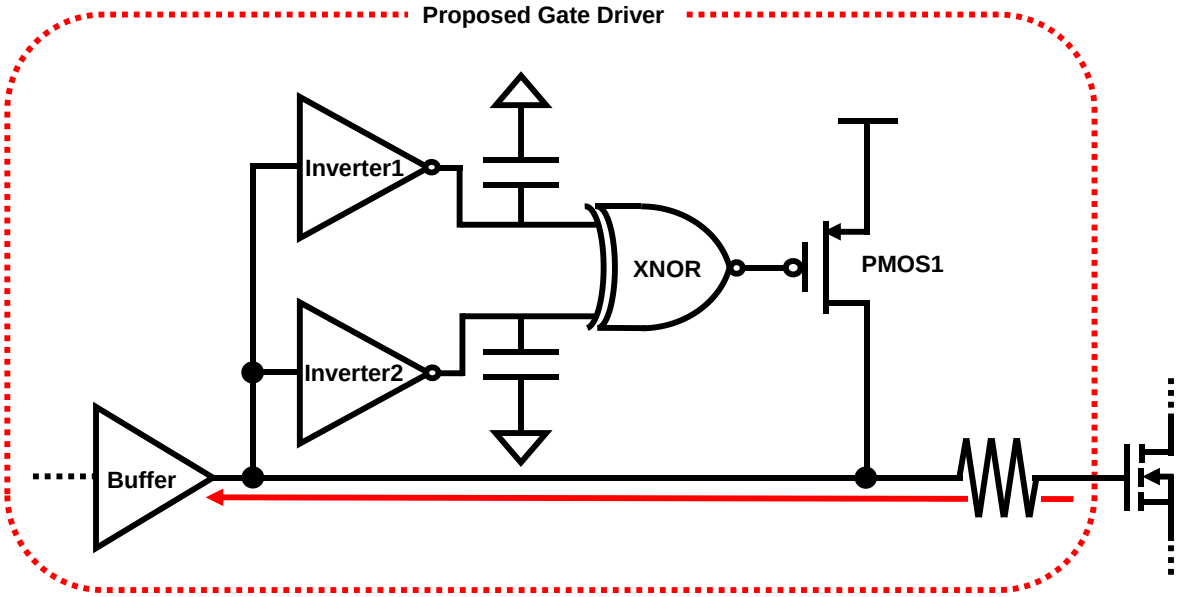
Inverter2
XNOR
PMOS1
Buffer

(b)


Proposed Gate Driver
Inverter1
Inverter2
XNOR
PMOS1
Buffer

(c)

Fig. 7.

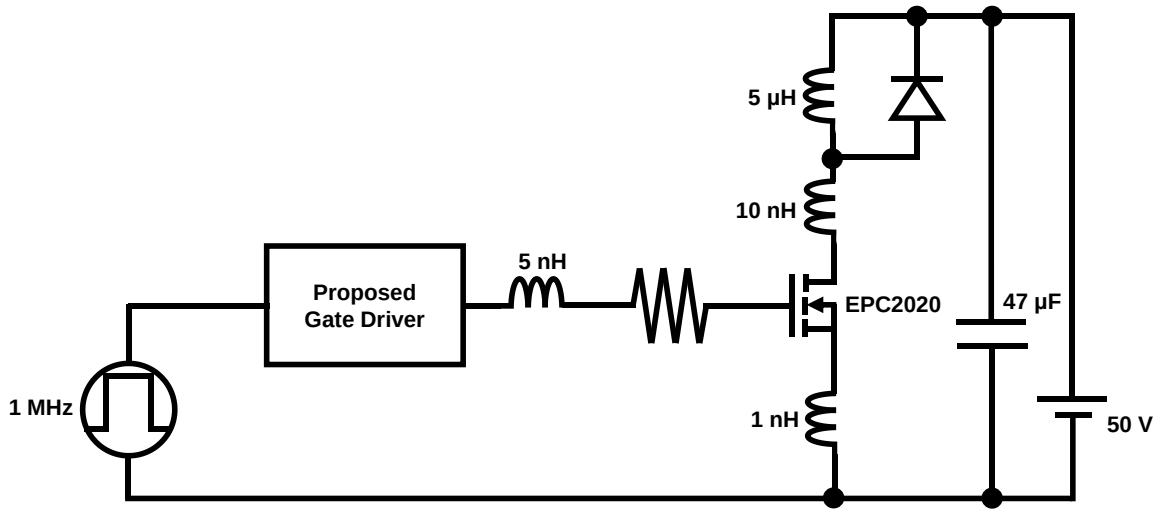
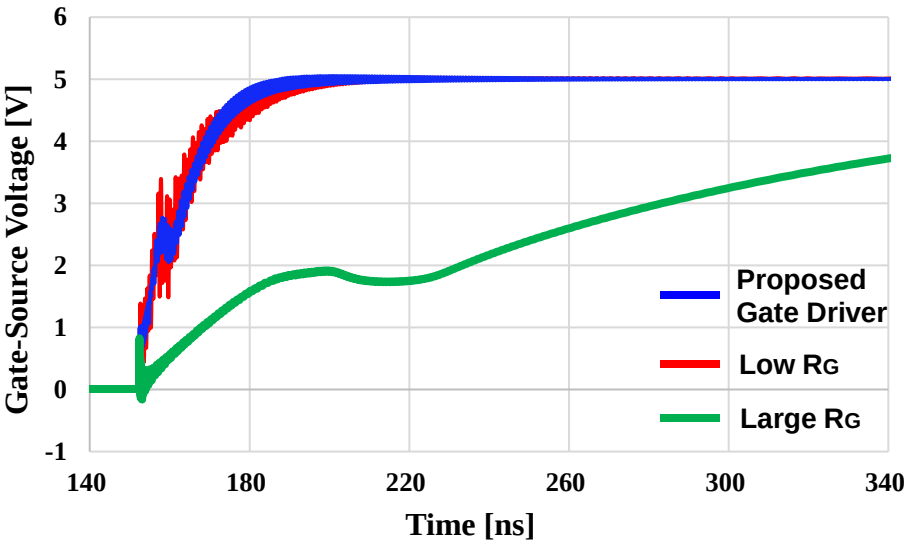
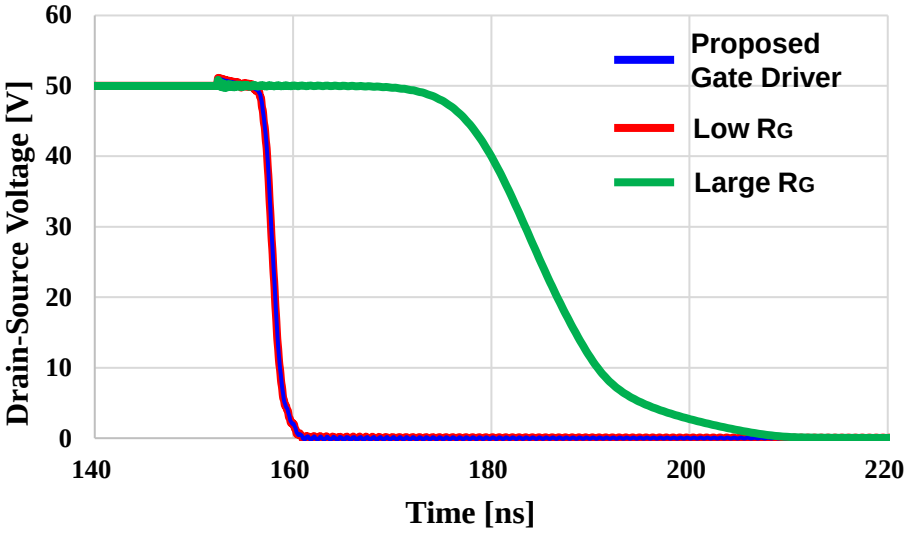


Fig. 8.

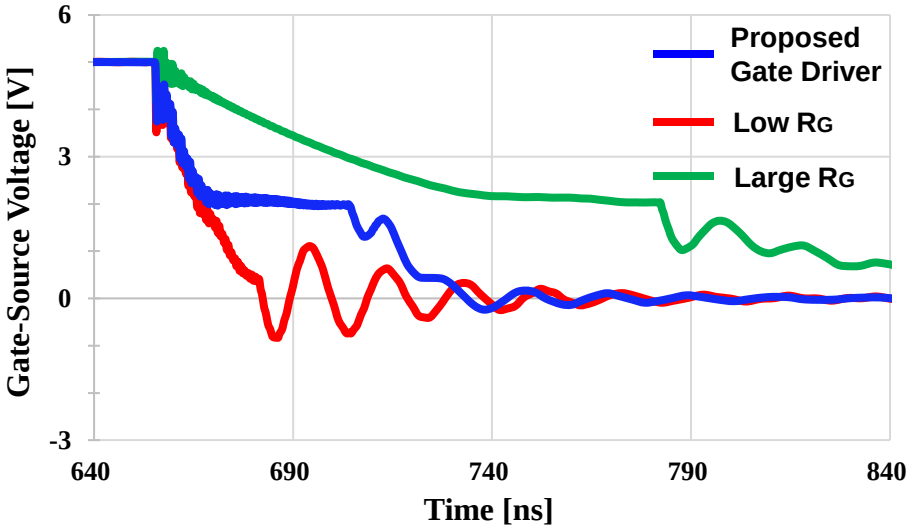

Gate-Source Voltage [V]
6
5
4
3
2
1
0
-1
140
180
220
260
300
340
Time [ns]
Proposed Gate Driver
Low RG
Large RG

(a)

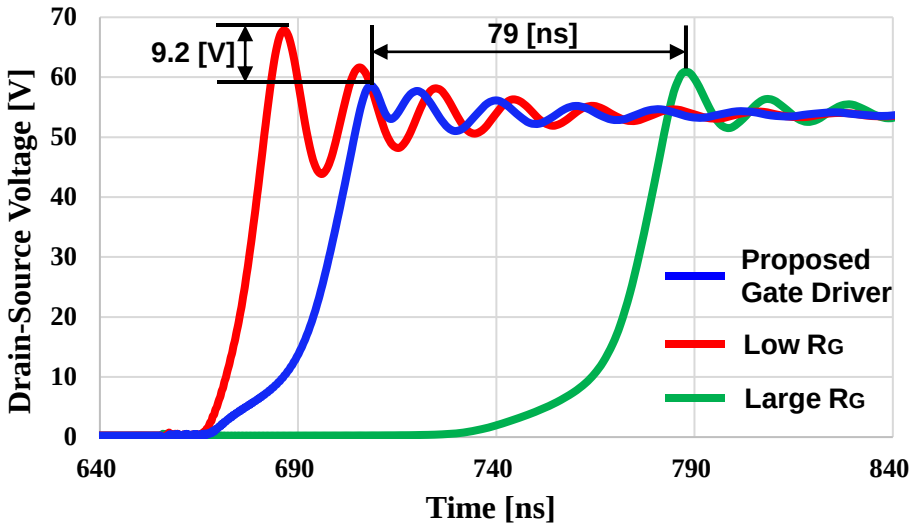

Drain-Source Voltage [V]
60
50
40
30
20
10
0
140
160
180
200
220
Time [ns]
Proposed Gate Driver
Low RG
Large RG

(b)

Fig. 9.


6
3
0
-3
640
690
740
790
840
Gate-Source Voltage [V]
Time [ns]
Proposed Gate Driver
Low RG
Large RG

(a)


9.2 [V]
79 [ns]
Drain-Source Voltage [V]
70
60
50
40
30
20
10
0
640
690
740
790
840
Time [ns]
Proposed Gate Driver
Low RG
Large RG

(b)

Fig. 10.

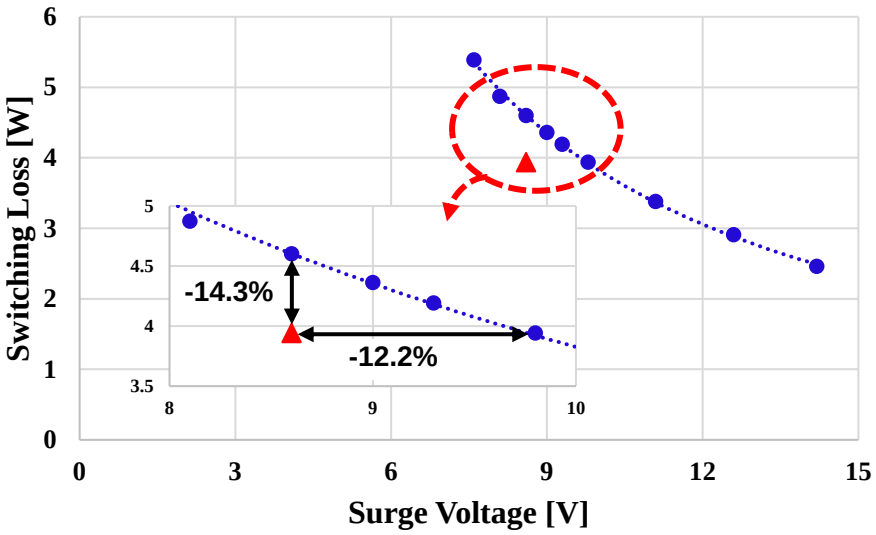

Switching Loss [W]
Surge Voltage [V]
0
1
2
3
4
5
6
0
3
6
9
12
15
-14.3%
-12.2%
3.5
4
4.5
5
8
9
10

Fig. 11.