# Low interface state densities at $Al_2O_3$/GaN interfaces formed on vicinal polar and non-polar surfaces

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## Abstract

Ni/$Al_2O_3$/GaN structures with vicinal GaN surfaces from *c*- or *m*-plane were formed. Then, electrical interface properties of the structures were systematically investigated. It was found that interface state density ($D_{it}$) at the $Al_2O_3$/GaN interface for *c*-plane are higher than that for *m*-plane, and post-metallization annealing (PMA) is quite effective to reduce $D_{it}$ for both *c*- and *m*-planes. As a result, the low $D_{it}$ value of ~ $3\times10^{10}$ $eV^{-1}$ $cm^{-2}$ was demonstrated for both planes.

## Article

Gallium Nitride (GaN) has attracted much attentions for next generation power switching devices due to its superior material properties such as wide band gap, high critical electric field strength and high electron saturation velocity [1]. A metal-insulator-semiconductor field effect transistor (MISFET) is one of sophisticated and useful devices to achieve the low gate leakage current during switching operation. Therefore, recently, researches related to GaN MISFETs have been reported [2, 3, 4, 5, 6, 7, 8, 9, 10]. For high power switching devices, a vertical device structure with a top source region and a bottom drain region through a conductive substrate has some advantages such as small device size and high breakdown voltage. A Ga-polar *c*-plane GaN substrate is mainly used in the reported devices with the vertical device structure [11, 12, 13, 14, 15, 16]. This could be owing to a controllability of impurity incorporation into epitaxial grown layer on the substrates.

In the vertical trench- or fin-type MISFETs fabricated on a *c*-plane GaN substrate, MIS channels will be formed on a lattice plane which is perpendicular or inclined to the *c*-plane. Since Ga and N atoms are bonded by covalent and ionic bonds [17], the polarity depends on the surface orientation of GaN. Also, the areal bond density and the bond

angles on the top GaN surface depends on the surface orientation [18]. Therefore, the MIS interface properties could strongly be impacted by the surface orientations. Then, investigation for MIS structure fabricated on *c*-plane will give us an indirect information of the channel. However, because of difficulties of epitaxial growth, there are few reports on MIS structure fabricated on other planes. For example, there are reports on *m*-plane GaN MIS capacitors which were formed directly on substrate without epitaxial grown layer [19, 20, 21]. These results show distorted capacitance-voltage (*C*-*V*) curves compared with an ideal *C*-*V* curve and large frequency dispersion in *C*-*V* curves, which indicates poor interface properties.

As discussed in ref. 12, *m*-plane GaN is considered to be a suitable plane orientation to form the MIS channel due to an ease of smooth surface formation by wet etching with basal chemicals. Recently, our group reported well-controlled impurity concentrations in the *m*-plane GaN layer grown by metal-organic vaper phase epitaxy (MOVPE) on vicinal surfaces from *m*-plane [22]. Also, the good electrical properties of Schottky diodes formed on the *m*-plane has been reported [23]. These results indicate that the *m*-plane itself has a possibility to be used as a surface to fabricate a vertical device on it. Either *c*- or *m*-plane will be used to fabricate the device on it, plane orientation dependence of MIS interface properties will be quite informative for both planer and three dimensional MISFET structures. In this study, thus, we systematically investigated the interface properties of MIS structures with an $Al_2O_3$ layer formed on *c*- or *m*-plane epitaxial grown layer.

Fig. 1 shows the device structure fabricated in this study. A GaN substrate with a Ga-polar *c*-plane (0001) or *m*-plane ($10\bar{1}0$) surface orientations was used. Both substrates were prepared by slicing from ingot grown along [0001] direction by halide vapor phase

epitaxy. The surfaces of the substrates have misorientations from the crystallographic surface orientations of (0001) or $(10\bar{1}0)$. The misorientation angle and direction of the *c*-plane substrates is 0.4° toward $[\bar{1}\,2\,\bar{1}\,0]$. For *m*-plane, the substrate with 5° of misorientation toward $[000\bar{1}]$ was used. Donor concentrations of the substrates are $2\times10^{18}$ $cm^{-3}$ and $2\times10^{17}$ $cm^{-3}$ for *c*- and *m*-plane, respectively. Then a 5-μm-thick GaN layer with a Si dopant was epitaxially grown on the substrates by MOVPE. Growth pressure, temperature and V/III ratio are 1000hPa, 1100℃, and 1019, respectively. Effective donor concentration of the epitaxial GaN layers was around $4\times10^{16}$ $cm^{-3}$ for all samples. As discussed in ref. 22, the concentrations of unintentionally incorporated impurities into the MOVPE layer grown on this substrate was suppressed to the order of $10^{15}$ $cm^{-3}$. The wafers were cleaned with a sulfuric acid solution mixed with hydrogen peroxide, a diluted HF solution, an ammonium hydroxide solution mixed with hydrogen peroxide and hydrochloric acid mixed with hydrogen peroxide in turn and rinsed with ultrapure water. Then, an $Al_2O_3$ layer with a thickness of 50 nm was deposited on GaN layers at a substrate temperature of 260℃ by the atomic layer deposition using trimethylalminum and $H_2O$ as precursors. Ni/Au gate metals were deposited using an electron beam (EB) evaporation and patterned to circular shape with a diameter of 200 μm using a metal shadow mask on the surfaces of the $Al_2O_3$ layers. Also, Ti/Al/Ti/Au Ohmic contacts were formed on the backside of the GaN substrates. Finally, post metallization annealing (PMA) was performed at 400℃ in a nitrogen ambient for 1hour.

Electrical interface properties were characterized by the *C*-*V*, conductance-voltage (*G*-*V*) techniques and the conductance method at room temperature.

As mentioned in the introduction part, the crystallographic surface difference between *c*- and *m*-planes could induce defect states with different energy levels and density after formation of a gate insulator layer. The difference could be detected in a *C*-*V* shift, stretched-out of a *C*-*V* curve and an energy distribution of $D_{it}$. Furthermore, *C*-*V* curves measured at various frequencies quickly gives us some information related to MIS interface properties. This is because the ac response related to interaction between free carriers and interface states located inside the bandgap is often observed in the depletion bias condition as a frequency dispersion. Therefore, the frequency dispersion of the *C*-*V* curves is a good indicator for existence of the interface states. Figures 2 (a) and 2 (b) show the *C*-*V* curves of the capacitors without PMA for the *c*- and *m*-planes, respectively. Here, the measurement frequencies are in a range from 1 kHz to 1MHz. Also, the dotted line indicates an ideal *C*-*V* curve assuming the work function of 5.15 eV for the Ni gate measured by ultraviolet photoelectron spectroscopy [24]. The lateral thin solid lines indicate capacitances at the flat-band conditions of GaN ($C_{FB}$), which means that the gate voltage range with the capacitance values lower than $C_{FB}$ is in the depletion condition. In Fig. 2 (a), the frequency dispersion was observed at the gate voltage range from −3.5 to −2.5 V. Here, the inset show the magnified *C*-*V* curves in the bias range. Also, the small frequency dispersion was observed in the gate voltage range from −2.5 to −1.0 V in Fig. 2 (b) as well as Fig. 2 (a). Furthermore, the measured *C*-*V* curves are well overlapped to the ideal *C*-*V* curve (not shown here), which means no distortion due to the *C*-*V* stretched-out and no hump due to the ac response related to the interface states. These results are inconsistent with the reported results for the *C*-*V* curves for the MIS structures fabricated directly on *m*-plane GaN substrate without epitaxial grown layer [19, 20, 21]. The inconsistency is attributable to the damage less surface of the epitaxial GaN layer formed

on the vicinal surface and the suitable surface treatment performed by wet chemicals in this study.

In general, in order to improve MIS interface properties, PMA is performed at around 400°C. Recently, in an MIS structure fabricated on *c*-plane GaN, effectiveness of PMA has been reported [25]. On the other hand, the effectiveness for the case of the *m*-plane has not been investigated yet. Figures 3 (a) and 3 (b) show the *C*-*V* curves of the capacitors with PMA for the *c*- and *m*-planes, respectively. Also, the inset shows the magnified *C*-*V* curves in the gate bias range for the depletion condition. It should be noted that, in both cases, the frequency dispersions are reduced by PMA compared with Figs. 2 (a) and 2 (b). This result strongly indicates that PMA is quite effective for improving the interface properties of the *m*-plane as well as *c*-plane. Furthermore, in Fig. 3 (b), the frequency dispersion is negligibly small, suggesting that interface state density ($D_{it}$) is quite low. Furthermore, an impact of PMA was observed in the accumulation bias condition. The accumulation capacitances in Figs. 3(a) and 3(b) are slightly lower than those in Figs. 2 (a) and 2 (b). Jiang *et al.* have already reported that PMA at a temperature range from 300°C to 500°C oxidizes the GaN surface, resulting in an obvious thickness increment of a Ga-oxide interfacial layer at 500°C [26]. Judging from the results, the reduction of the accumulation capacitances in this study is attributable to the thickness increment of the Ga-oxide interfacial layer between the $Al_2O_3$ layer and the GaN surfaces.

While the capacitance is not sensitive for detection of the interface states due to influence of the oxide and semiconductor capacitances, *G*-*V* characteristics is more sensitive due to a direct measurement of ac current regarding capture of free carriers to the interface states if a series resistance is small enough. Figure 4 shows the *G*-*V* curves for the capacitors with PMA for the *c*- and *m*-planes. Here, the measurement frequency

was 10 kHz. Peaks associated with the ac response are clearly observed at the gate voltage around 0 V and 0.8 V for the *c*- and *m*-planes, respectively. This indicates existence of the interface states and that $D_{it}$ is still in a measurable range. Moreover, the peak height for the *m*-plane is lower than that for the *c*-plane, which means that there is a possibility that $D_{it}$ for the *m*-plane is lower than that for the *c*-plane. On the other hand, the peak heights in the *G*-*V* curves depend on $D_{it}$, the measurement frequency, and the series resistance. Therefore, an accurate evaluation of $D_{it}$ using the conductance method including the surface potential fluctuation has an important meaning. Figure 5 shows energy distributions of $D_{it}$ for the capacitors. Here, the $D_{it}$ values were evaluated by the conductance method including the surface potential fluctuation [27]. The $D_{it}$ values for the *c*-plane without PMA (open black circles) is about two times higher than those for the *m*-plane without PMA (open blue circles). On the other hand, the $D_{it}$ values for the *c*- and *m*-planes with PMA (solid black and blue circles) are much smaller than those without PMA, and the $D_{it}$ distribution for the *c*-plane with PMA is well overlapped on the distribution for the *m*-plane with PMA. As a result, the $D_{it}$ value for the both capacitors with PMA is around $3\times10^{10}$ $eV^{-1}$ $cm^{-2}$ at 0.3 eV below the conduction band minimum ($E_C$). The $D_{it}$ value for the *c*-plane is almost the same values reported in Ref. [25, 28], in which GaN-on-GaN and GaN-on-sapphire structures were used. On the other hand, the $D_{it}$ value for the *m*-plane could be currently the lowest value although some reports have not evaluated the $D_{it}$ values yet [19, 20, 21].

According to a theoretical calculation [29], Ga dangling bonds form states near $E_C$ in both planes. In the case of the capacitors without PMA, the estimated $D_{it}$ for the *c*-plane was 2 times higher than that for the *m*-plane. Interestingly, this difference corresponds to the Ga bond densities for both planes. Therefore, the Ga dangling bond could be a

candidate for the interface states. As mentioned before, PMA induces the oxidation of the GaN surfaces. As a result, Ga dangling bonds were well passivated after PMA, resulting in the low $D_{it}$ values for both planes. In this case, the physical origin of the interface states could be no longer Ga dangling bonds. Fluctuations of bond length and bond angle of Ga-N bonding generate band tailing from the conduction and valence bands to the bandgap. Therefore, the interface states observed after PMA could be originated from the band tailing. The band-tailing state density does not depend on the bond areal density. As a result, the overlapped $D_{it}$ distributions after PMA was observed as shown in Fig. 5. These results indicate that the formation of the $Al_2O_3$/*m*-plane GaN interface with low $D_{it}$ is possible as well as the case of the *c*-plane. This is quite informative for realizing the vertical GaN MISFETs.

Fixed oxide charges inside the $Al_2O_3$ layers and/or the $Al_2O_3$/GaN interfaces are also of importance as well as $D_{it}$ because the fixed oxide charges are one of origins degrading the carrier transport properties. The effective density of the fixed oxide charges ($N_F$) can be evaluated from the horizontal shift of *C*-*V* curve from the ideal curve and an assumption that the fixed oxide charges are located at the $Al_2O_3$/GaN interface. The *C*-*V* curves for both *c*- and *m*-planes without PMA shown in Figs. 2 (a) and 2 (b) are negatively shifted compared with the ideal *C*-*V* curves. The flatband voltages ($V_{FB}$) are −2.3 and −1.2 V for the *c*- and *m*-planes, respectively. This indicates existence of positive fixed charges in both structures and its density $N_F$ for the *c*- and *m*-planes are $3.6\times10^{12}$ $cm^{-2}$ and $2.3\times10^{12}$ $cm^{-2}$, respectively. After PMA, the *C*-*V* curves are shifted toward the positive bias direction compared with the *C*-*V* curves for without PMA. As a result, both *C*-*V* curves are located near the ideal *C*-*V* curves. $V_{FB}$ after PMA are 0.4 and 1.4 V for the *c*- and *m*-

planes, respectively. The values of $N_F$ for the *c*- and *m*-planes with PMA are $+5.8\times10^{11}$ $cm^{-2}$ and $-3.6\times10^{11}$ $cm^{-2}$, respectively.

Reason for the reductions of $N_F$ by PMA should be considered. In general, from a *C*-*V* shift toward the positive direction, it is impossible to judge whether the positive charges dominantly decrease or the negative charges dominantly increase. In GaN MISFETs formed on the *c*- and *m*-planes, PMA obviously improves mobility at low carrier concentration in the channel for both planes [30]. This means that total interface charges were reduced by PMA. Taking into the reduction of the interface charges and the existence of the negative fixed charges in the *m*-plane account, it is a reasonable phenomenon that the positive charges dominantly decrease and the negative charges slightly increase at the same time. Then, an origin of the positive charges is considered. As mentioned before, during PMA, the Ga oxidation occurs. Before the oxidation, ionized Ga atoms (for example, interstitial Ga atoms in the Ga-oxide interfacial layer and/or the GaN surface) exist near the $Al_2O_3$/GaN interface [31], which are positively charged due to lack of electrons. The oxidation by PMA passivates the ionized Ga atoms with oxygen atoms. Therefore, the positive charges were reduced by PMA. On the other hand, during the oxidation, dissociated nitrogen atoms diffuse into the $Al_2O_3$ layer. A part of the dissociated nitrogen atoms substitutes the oxygen atoms in the $Al_2O_3$ layer. The substituted nitrogen atoms ($N_O$) form energy states around midgap of GaN which has a (0/-1) nature [32]. Due to the deep energy level of $N_O$, captured electron cannot communicate with the conduction band edge, which means $N_O$ works as a fixed negative charge.

Interestingly, the $V_{FB}$ difference between the *c*- and *m*-planes is around 1V without depending on performing PMA. This could indicate that difference of the surface

orientations and the related polarization charges generate the $V_{FB}$ difference, resulting in the positive and negative signs for the fixed charges.

In summary, we demonstrated the low $D_{it}$ values less than $1\times10^{11}$ $eV^{-1}$ $cm^{-2}$ for the GaN MIS capacitors fabricated on the *m*-plane with the vicinal GaN surface. Effectiveness of PMA for both *m*- and *c*-planes was also proved for reducing $D_{it}$ and $N_F$. As a result, by applying PMA, the $D_{it}$ values of ~ $3\times10^{10}$ $eV^{-1}$ $cm^{-2}$ at the energy level of $E-E_C$ =−0.3 eV and the $N_F$ values in the order of $10^{11}$ $cm^{-2}$ were observed for both planes. These could be acceptable level for actual vertical n-channel GaN MISFETs with high performance.

Acknowledgment

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Data Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## References

[1] T. P. Chow, Microelectronic Engineering **83**, 112 (2006).

[2] Y. Irokawa, Y. Nakano, M. Ishiko, T. Kachi, J. Kim, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abemathy, S. J. Pearton, C.-C. Pan, G.-T. Chen, and J.-I. Chyi, Appl. Phys. Lett. **84**, 2919 (2004).

[3] K. Matocha, T. P. Chow, and R. J. Gutmann, IEEE Trans. Electron Devices **52**, 6 (2005).

[4] W. Huang, T. Khan, and T. P. Chow, IEEE Electron Device Lett. **27**, 796 (2006).

[5] H. Otake, S. Egami, H. Ohta, Y. Nanishi and H. Takasu, Jpn. J. Appl. Phys. **46**, L599(2007).

[6] S. Gu, H. Katayose, K. Nomoto, T. Nakamura, A. Ohoka, K. Lee, W. Lu, and P. M. Asbeck, Phys. Status Solidi C **10**, 820 (2013).

[7] S. Takashima, K. Ueno, H. Matsuyama, T. Inamoto, M. Edo, T. Takahashi, M. Shimizu, and K. Nakagawa, Appl. Phys. Express **10**, 121004 (2017).

[8] R. Tanaka, S. Takashima, K. Ueno, H. Matsuyama, M. Edo, and K. Nakagawa, Appl. Phys. Express **12**, 054001 (2019).

[9] H. Ogawa, T. Okazaki, H. Kasai, K. Hara, Y. Notani, Y. Yamamoto, and T. Nakamura, Phys. Status Solidi C **11**, 302 (2014).

[10] H. Ogawa, H. Kasai, K. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, Phys. Status Solidi C **11**, 918 (2014).

[11] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, Appl. Phys. Express **1**, 011105 (2008).

[12] M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, Appl. Phys. Express **1**, 021104 (2008).

[13] T. Oka, T. Ina, Y. Ueno, and J. Nishii, Appl. Phys. Express **8**, 054101 (2015).

[14] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, 2017 IEEE International Electron Devices Meeting, 9.2.1 (2017).

[15] M. Yoshino, Y. Ando, M. Deki, T. Toyabe, K. Kuriyama, Y. Honda, T. Nishimura, H. Amano, T. Kachi, and T. Nakamura, Materials **12**, 689 (2019).

[16] R. Tanaka, S. Takashima, K. Ueno, H. Matsuyama, and M. Edo, Jpn. J. Appl. Phys. **59**, SGGD02 (2020).

[17] J. Nord, K. Albe, P. Erhart, and K. Nordlund, J. Phys.: Condens. Matter **15**, 5649 (2003).

[18] F. Yu, S. Yao, F. Romer, B. Witzigmann, T. Schimpke, M. Strassburg, A. Bakin, H. W. Schumacher, E. Peiner, and H. S. Wasisto, Nanotechnology **28**, 095206 (2017).

[19] K. Matocha, V. Tilak, and G. Dunne, Appl. Phys. Lett. **90**, 123511 (2007).

[20] Y. Jia, J. S. Wallace, E. Echeverria, J. A. Gardella, and U. Singisetti, Phys. Stat. Solidi B **254**, 1600681 (2017).

[21] Y. Jia, K. Zeng, and U. Singisetti, J. Appl. Phys. **122**, 154104 (2017).

[22] A. Tanaka, Y. Ando, K. Nagamatsu, M. Deki, H. Cheong, B. Ousmane, M. Kushimoto, S. Nitta, Y. Honda, and H. Amano, Phys. Status Solidi A **215**, 1700645 (2018).

[23] H. Yamada, H. Chonan, T. Takahashi, and M. Shimizu, Appl. Phys. Express **10**, 041001 (2017).

[24] D. E. Eastman, Phy. Rev. B, **2**, 1 (1970).

[25] T. Hashizume, S. Kaneki, T. Oyobiki, Y. Ando, S. Sasaki, and K. Nishiguchi, Appl. Phys. Express **11**, 124102 (2018).

[26] H. Jiang, X. Lu, C. Liu, Q. Li, and K. M. Lau, Phys. Status Solidi A **213**, 868 (2016).

[27] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).

[28] T. Marron, S. Takashima, Z. Li, and T. P. Chow, Phys. Status Solidi C **9**, 907 (2012).

[29] S. Gu, E. A. Chagarov, J. Min, S. Madisetti, S. Novak, S. Oktyabrsky, A. J. Kerr, T. Kaufman-Osborn, A. C. Kummel, and P. M. Asbeck, Appl. Surface Sci. **317**, 1022

(2014).

[30] Y. Ando, K. Nagamatsu, M. Deki, N. Taoka, A. Tanaka, S. Nitta, Y. Honda, T. Nakamura, and H. Amano, to be submitted.

[31] R. Therrien, G. Lucovsky, and R. Davis, Appl. Surface Sci. **166**, 513 (2000).

[32] M. Choi, J. L. Lyons, A. Janotti, and C. G. Van de Walle, Appl. Phys. Lett. **102**, 142902 (2013).

## Figure captions

Fig. 1 : (Color online) Structure of MIS capacitors fabricated in this study.

Fig. 2 : (Color online) *C*-*V* curves of the capacitors without PMA for (a) *c*- and (b) *m*-planes. The dotted line indicates an ideal *C*-*V* curve. The insets show the magnified *C*-*V* curves in the depletion bias conditions.

Fig. 3 : (Color online) *C*-*V* curves of the capacitors with PMA for (a) *c*- and (b) *m*-planes. The insets show the magnified *C*-*V* curves in the depletion bias conditions.

Fig. 4 : (Color online) *G*-*V* curves for the capacitors with PMA for the *c*- and *m*-planes.

Fig. 5 : (Color online) Energy distributions of $D_{it}$ for the capacitors.

## Figures

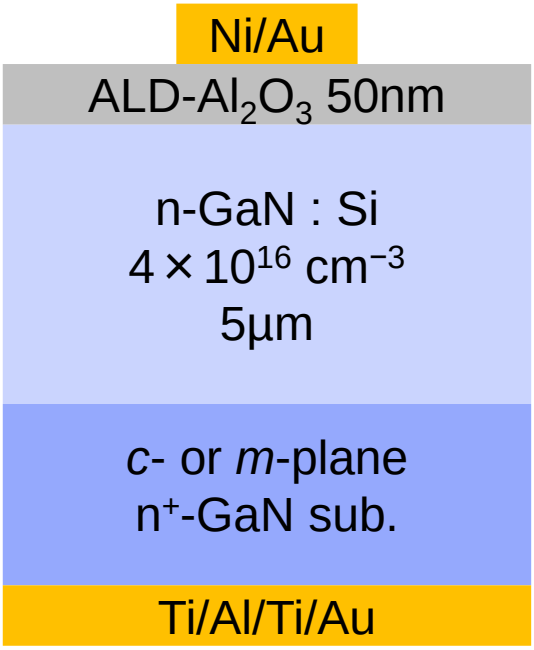


Fig. 2

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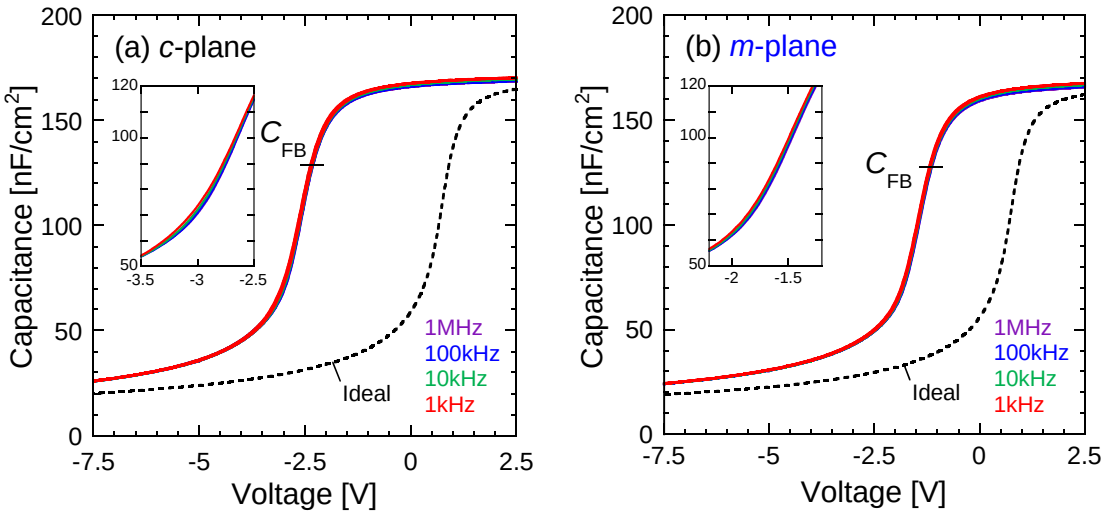


Fig. 3

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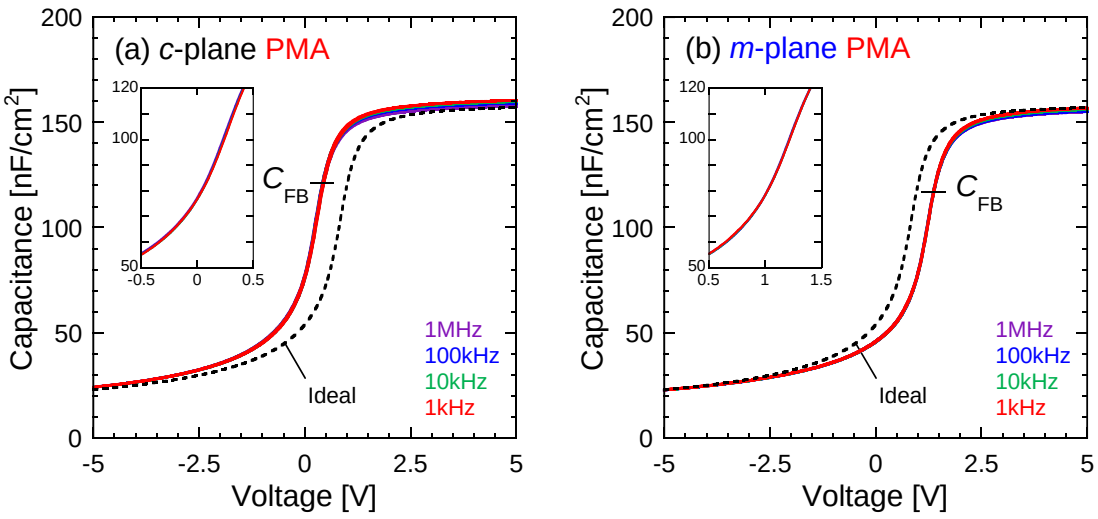


Fig. 4

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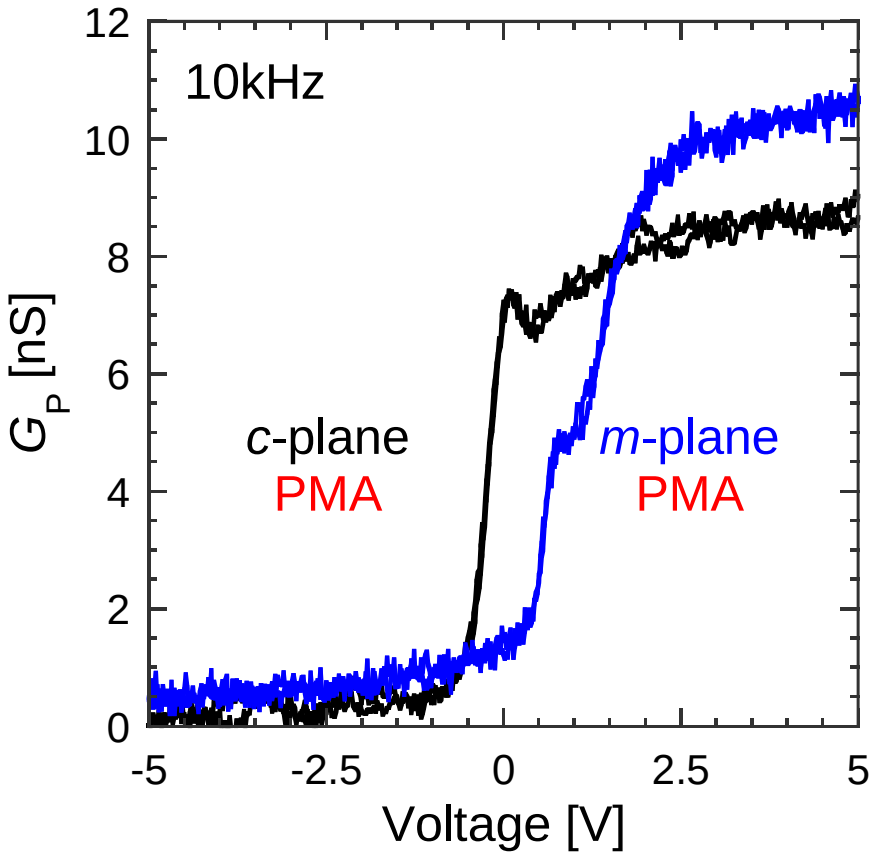


Fig. 5

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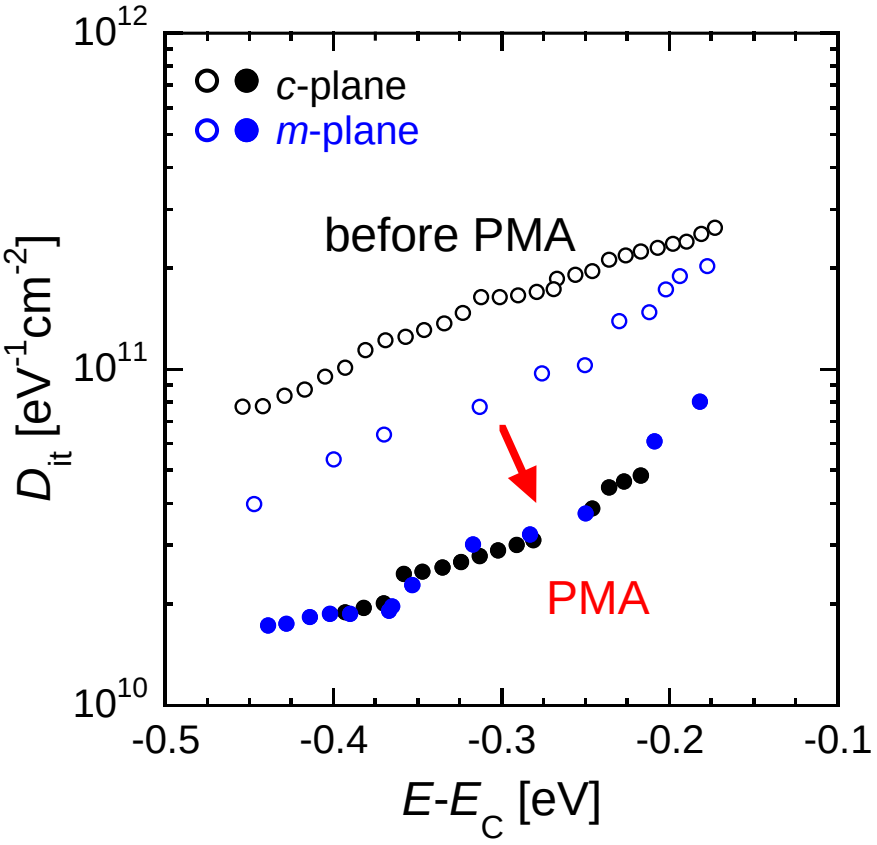


Fig. 6

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